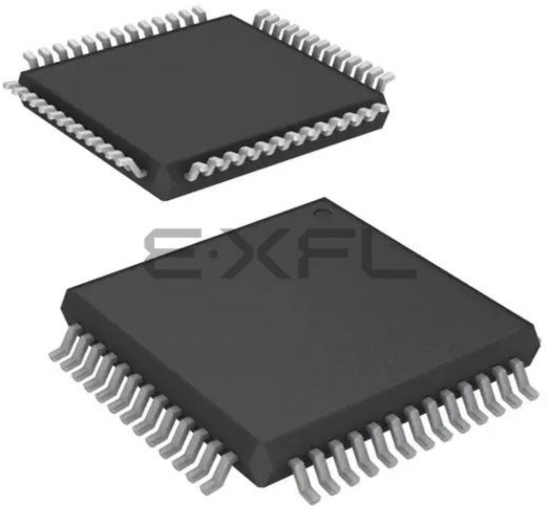

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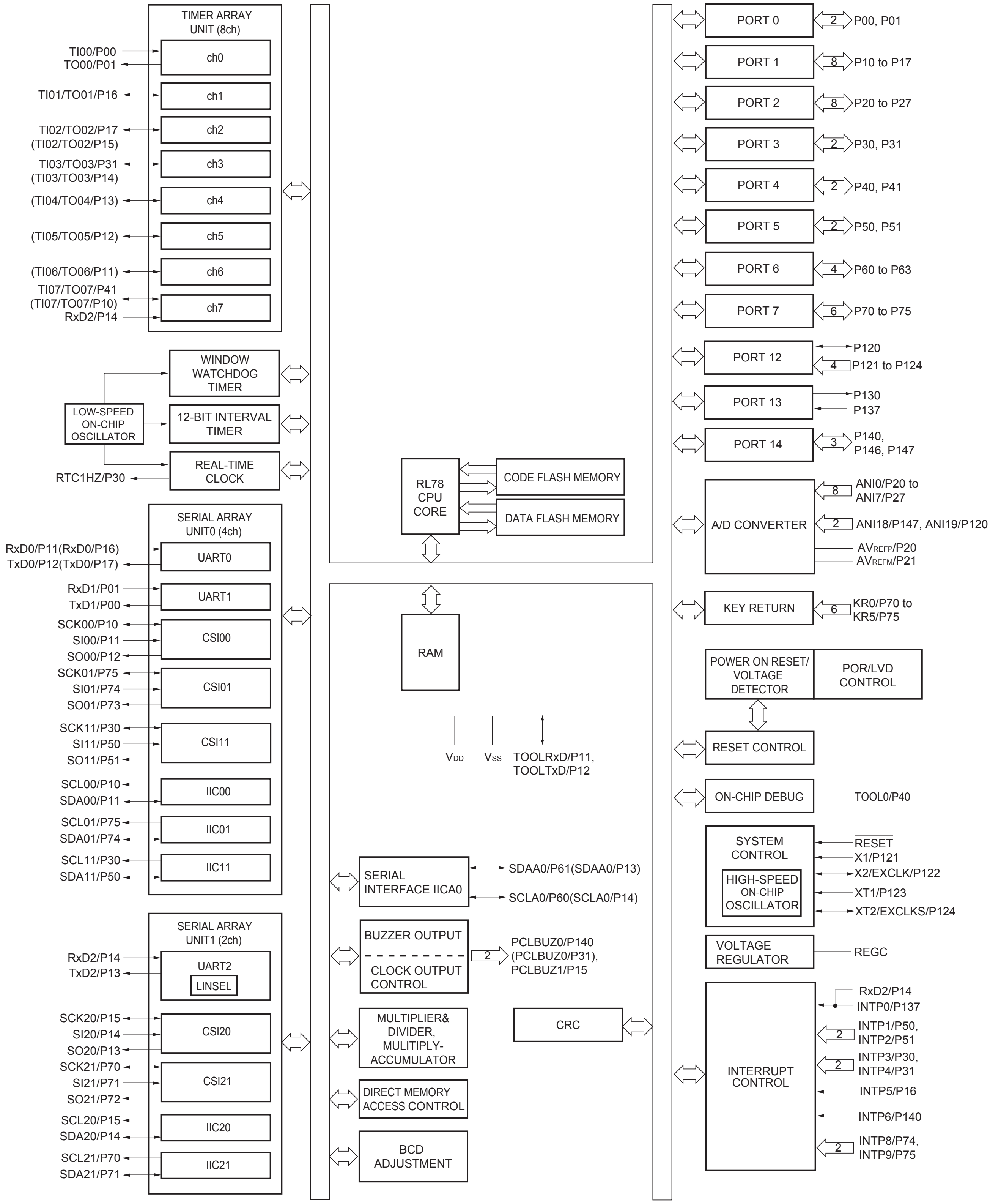
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | 52-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101jjafa-v0 |

### 1.5.9 48-pin products




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | $I_{DD1}$ | Operating mode | HS (high-speed main) mode [Note 5] | $f_{IH}$ = 32 MHz [Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 6.1 | 9.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 6.1 | 9.5 | mA |
| | | | | $f_{IH}$ = 24 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 7.4 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 7.4 | mA |
| | | | | $f_{IH}$ = 16 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 3.5 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.5 | 5.3 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{IH}$ = 8 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.3 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.3 | mA |
| | | | LV (low-voltage main) mode [Note 5] | $f_{IH}$ = 4 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.0 | mA |
| | | | HS (high-speed main) mode [Note 5] | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = –40°C | Normal operation | Square wave input | | 5.4 | 6.5 | μA |
| | | | | | | Resonator connection | | 5.5 | 6.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +25°C | Normal operation | Square wave input | | 5.5 | 6.5 | μA |
| | | | | | | Resonator connection | | 5.6 | 6.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +50°C | Normal operation | Square wave input | | 5.6 | 9.4 | μA |
| | | | | | | Resonator connection | | 5.7 | 9.5 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 12.0 | μA |
| | | | | | | Resonator connection | | 6.0 | 12.1 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +85°C | Normal operation | Square wave input | | 6.6 | 16.3 | μA |
| | | | | | | Resonator connection | | 6.7 | 16.4 | μA |

(**Notes** and **Remarks** are listed on the next page.)

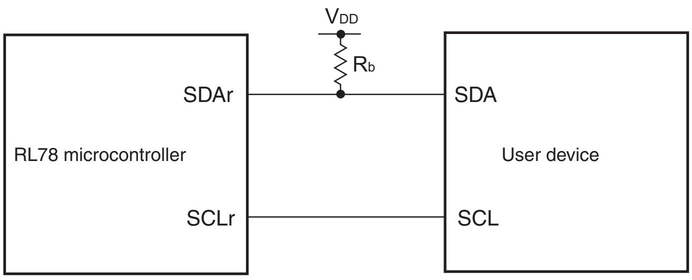
**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**
**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode MIN. | HS (high-speed main) Mode MAX. | LS (low-speed main) Mode MIN. | LS (low-speed main) Mode MAX. | LV (low-voltage main) Mode MIN. | LV (low-voltage main) Mode MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 38 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | — | | 25 | | 25 | ns |

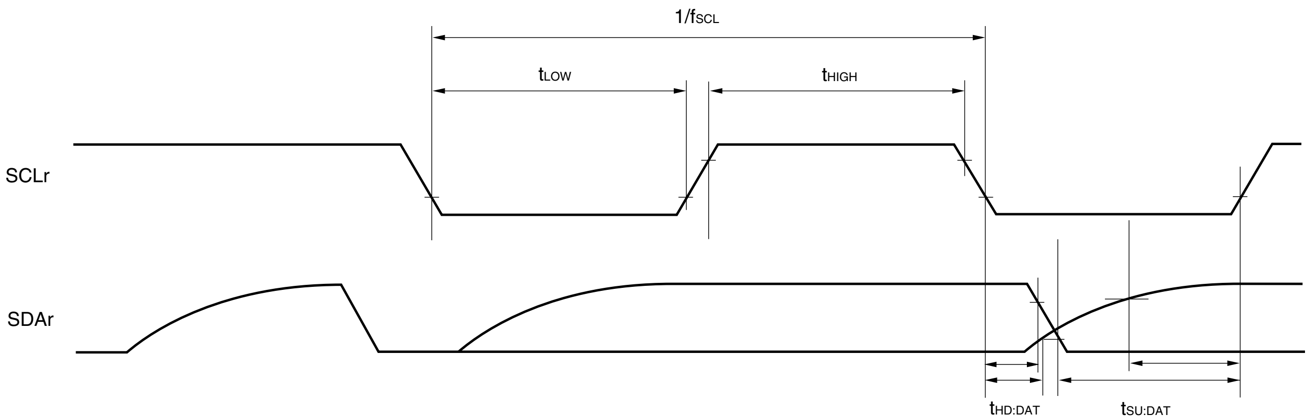
**Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Simplified I²C mode mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

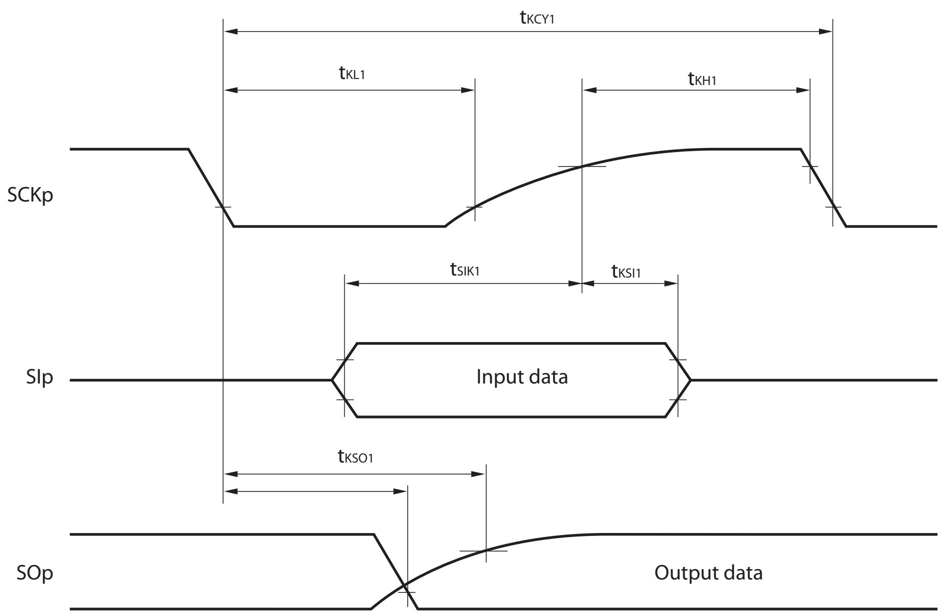
**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

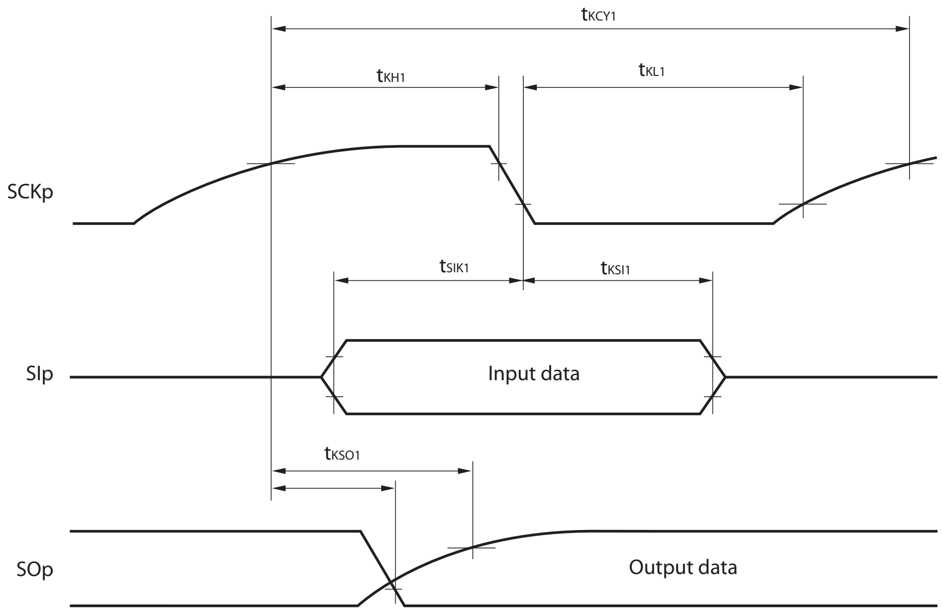
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI14 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI26 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | – |

**(1) When reference voltage (+)= $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 4] | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 4] | | | ±0.50 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V [Note 4] | | | ±0.50 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 4] | | | ±5.0 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 4] | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | | $V_{BGR}$ [Note 5] | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | | $V_{TMPS25}$ [Note 5] | | V |

(**Notes** are listed on the next page.)

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | 1.2 | ±8.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin : ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution<br>$EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±6.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution<br>$EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI26 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**5.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ [Note 3], Reference voltage (–) = $AV_{REFM}$ = 0 V [Note 4], HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error [Notes 1, 2] | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error [Note 1] | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error [Note 1] | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ [Note 3] | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### LVD Detection Voltage of Interrupt & Reset Mode

**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

### 2.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

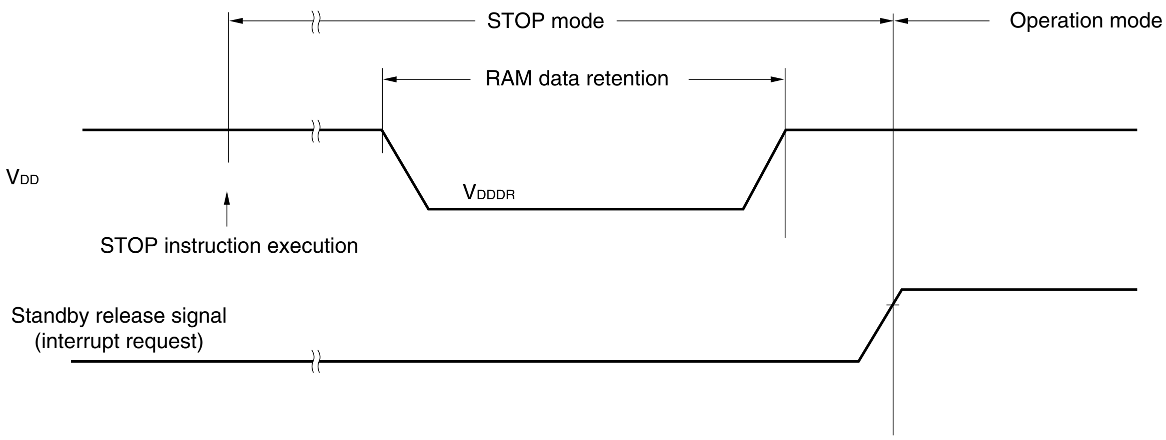
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

## 2.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46[Note] | | 5.5 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{DD0}$ | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I = V_{DD}$ | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I = V_{DD}$, In input port or external clock input | | | 1 | μA |
| | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{SS0}$ | | | −1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I = V_{SS}$ | | | −1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I = V_{SS}$, In input port or external clock input | | | −1 | μA |
| | | | In resonator connection | | | −10 | μA |
| On-chip pll-up resistance | $R_U$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{SS0}$, In input port | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

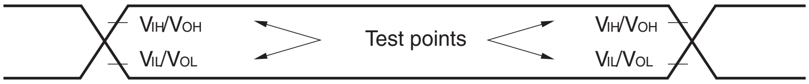
**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

## 3.5 Peripheral Functions Characteristics

**AC Timing Test Points**




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

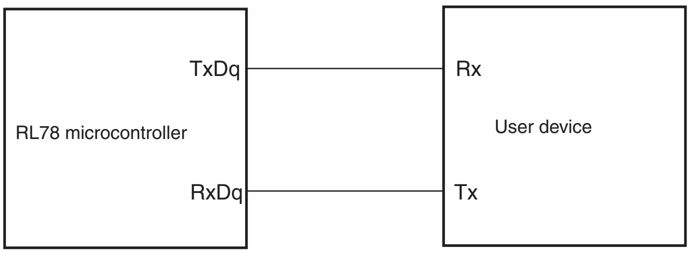
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate [Note 1] | | | | $f_{MCK}/12$ [Note 2] | bps |
| | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

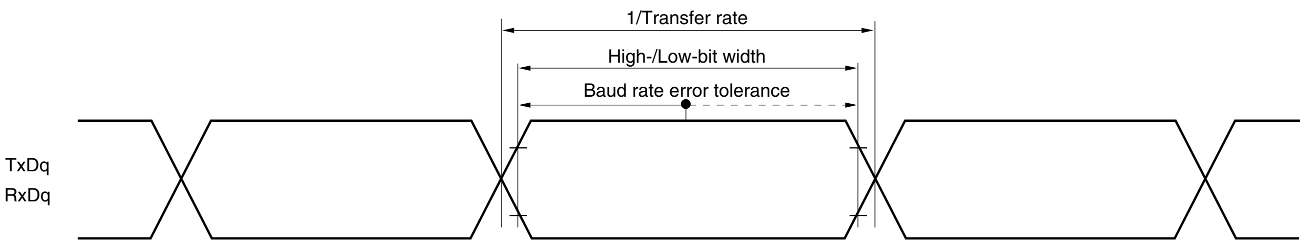
**2.** The following conditions are required for low voltage interface when $E_{VDD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (simplified I²C mode)**
**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 220 Note2 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | $1/f_{MCK}$ + 580 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.
**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**
**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 340 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 340 Note 2 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | $1/f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | $1/f_{MCK}$ + 570 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}/4$.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error [Note 1] | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin : ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error [Notes 1, 2] | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error [Notes 1, 2] | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error [Note 1] | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI26 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

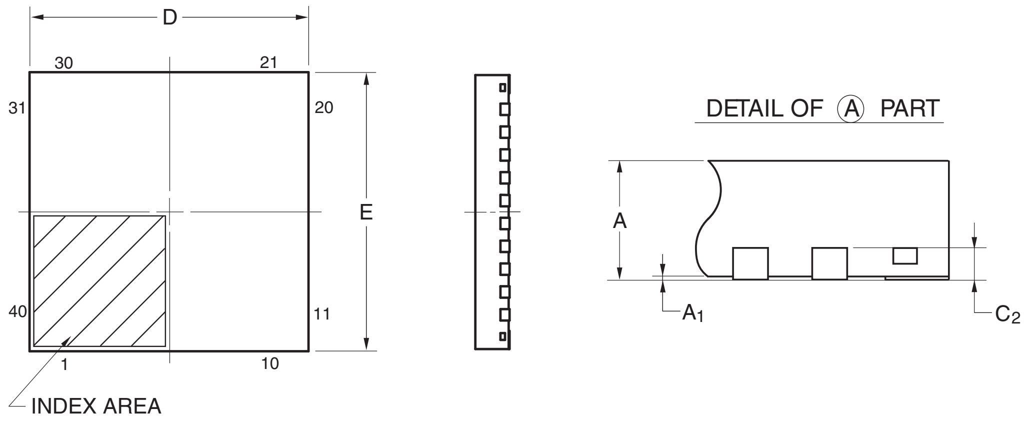
**3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

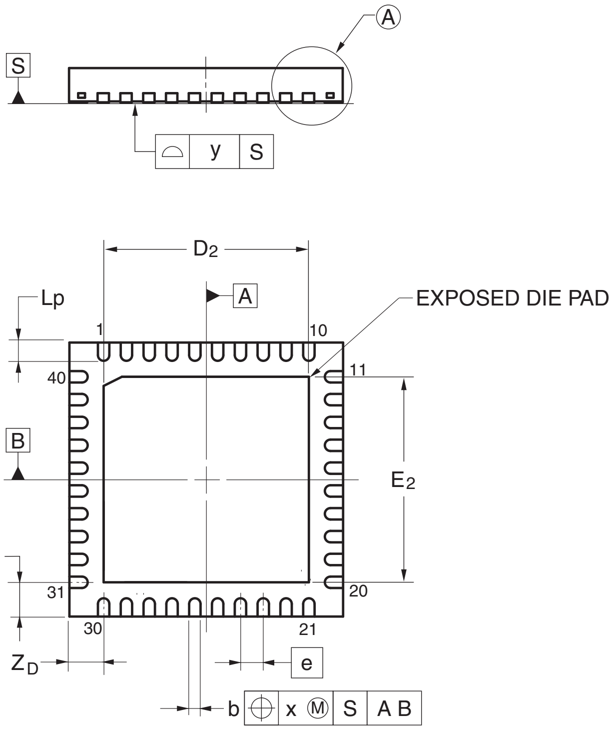
**4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

## 4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA
R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA
R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA, R5F100EHGNA

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-5 | 0.09 |




| Referance Symbol | Dimension in Millimeters Min | Nom | Max |
|---|---|---|---|
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 4.50 | — |
| $E_2$ | — | 4.50 | — |

## NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.