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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lcdfa-v0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application	Ordering Part Number
			Note	
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A G	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CAALA#W0, R5F100CAALA#W0, R5F100CEALA#W0, R5F100CGALA#W0 R5F100CAGLA#W0, R5F100CAGLA#U0, R5F100CAGLA#U0, R5F100CAGLA#U0, R5F100CAGLA#U0, R5F100CAGLA#U0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0, R5F100CAGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CAALA#W0, R5F10AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
				R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0
				R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0
			D	R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0
				R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0
			G	R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0,
				R5F100EDGNA#W0, R5F100ECGNA#W0,
				R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	А	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0,
		mounted		R5F101EEANA#00, R5F101EFANA#00, R5F101EGANA#00, R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0
			D	R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EFDNA#W0, R5F101EDNA#W0, R5F101EFDNA#W0,
				R5F101EGDNA#W0, R5F101EHDNA#W0

Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



Table 1-1. List of Ordering Part Numbers

(11/12)

Pin count	Package	Data flash	Fields of Application	Ordering Part Number
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	Mounted	А	R5F100PFAFB#V0, R5F100PGAFB#V0, R5F100PHAFB#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFB#X0, R5F100PHAFB#X0,
	min, 0.5 min pitch)			R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0
			D	R5F100PFDFB#V0, R5F100PGDFB#V0, R5F100PHDFB#V0,
				R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0
				R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0,
				R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0
			G	R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0,
				R5F100PJGFB#V0
				R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0,
				R5F100PJGFB#X0
		Not	Α	R5F101PFAFB#V0, R5F101PGAFB#V0, R5F101PHAFB#V0,
		mounted		R5F101PJAFB#V0, R5F101PKAFB#V0, R5F101PLAFB#V0
				R5F101PFAFB#X0, R5F101PGAFB#X0, R5F101PHAFB#X0,
				R5F101PJAFB#X0, R5F101PKAFB#X0, R5F101PLAFB#X0
			D	R5F101PFDFB#V0, R5F101PGDFB#V0, R5F101PHDFB#V0,
				R5F101PJDFB#V0, R5F101PKDFB#V0, R5F101PLDFB#V0
				R5F101PFDFB#X0, R5F101PGDFB#X0, R5F101PHDFB#X0,
				R5F101PJDFB#X0, R5F101PKDFB#X0, R5F101PLDFB#X0
	100-pin plastic	Mounted	Α	R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0,
	LQFP (14 × 20 mm,			R5F100PJAFA#V0, R5F100PKAFA#V0, R5F100PLAFA#V0
	0.65 mm pitch)			R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0,
				R5F100PJAFA#X0, R5F100PKAFA#X0, R5F100PLAFA#X0
			D	R5F100PFDFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0,
				R5F100PJDFA#V0, R5F100PKDFA#V0, R5F100PLDFA#V0
				R5F100PFDFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0,
				R5F100PJDFA#X0, R5F100PKDFA#X0, R5F100PLDFA#X0
			G	R5F100PFGFA#V0, R5F100PGGFA#V0, R5F100PHGFA#V0,
				R5F100PJGFA#V0
				R5F100PFGFA#X0, R5F100PGGFA#X0, R5F100PHGFA#X0,
				R5F100PJGFA#X0
		Not	Α	R5F101PFAFA#V0, R5F101PGAFA#V0, R5F101PHAFA#V0,
		mounted		R5F101PJAFA#V0, R5F101PKAFA#V0, R5F101PLAFA#V0
				R5F101PFAFA#X0, R5F101PGAFA#X0, R5F101PHAFA#X0,
				R5F101PJAFA#X0, R5F101PKAFA#X0, R5F101PLAFA#X0
			D	R5F101PFDFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0,
				R5F101PJDFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0
				R5F101PFDFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0,
				R5F101PJDFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0

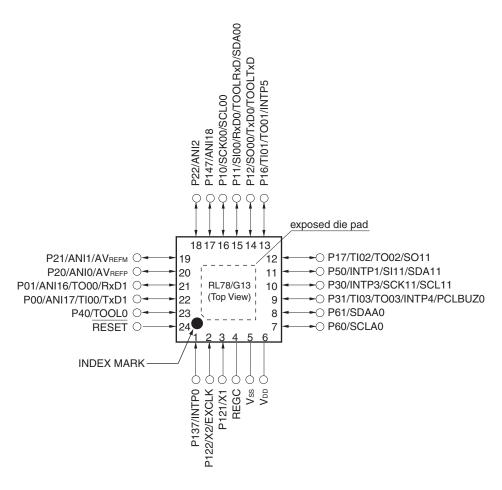
Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



1.3.2 24-pin products

• 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

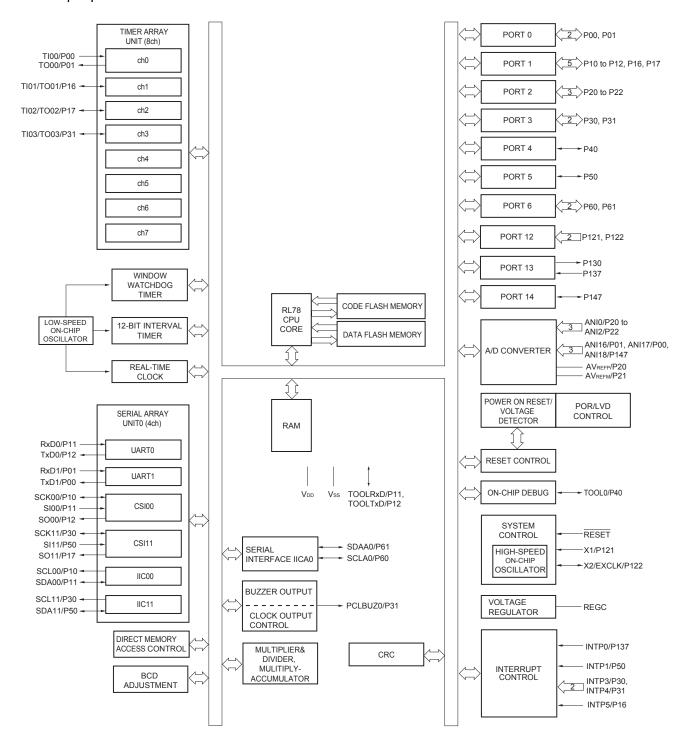


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

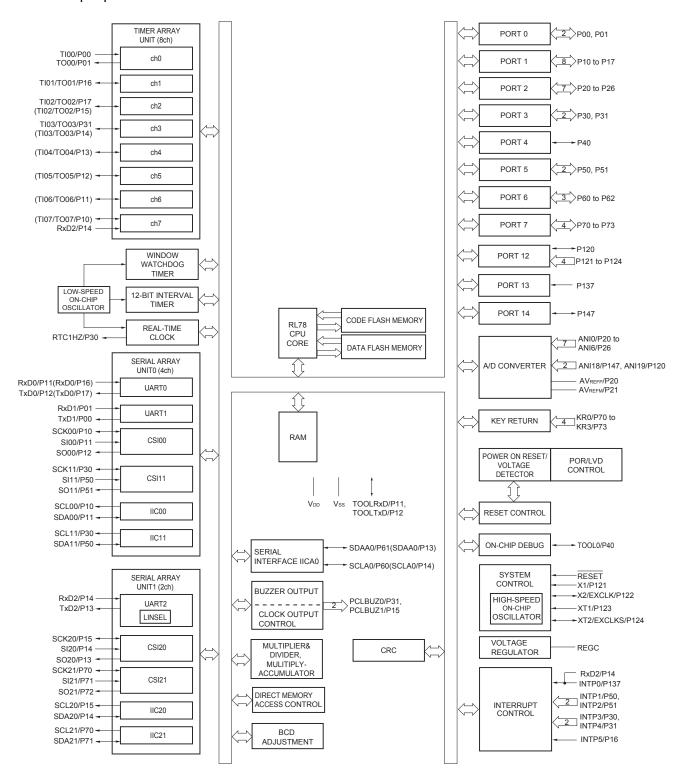
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. It is recommended to connect an exposed die pad to $V_{\mbox{\scriptsize ss}}.$

1.5.3 25-pin products



1.5.7 40-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.

Absolute Maximum Ratings (TA = 25°C) (2/2)

Parameter	Symbols		Conditions	Ratings	Unit
Output current, high	Іон1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	І ОН2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	lo _{L1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	lo _{L2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient	TA	In normal operati	on mode	-40 to +85	°C
temperature		In flash memory	programming mode		
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V) (5/5)

Items	Symbol	Conditio	ns		MIN.	TYP.	MAX.	Unit
Input leakage current, high	Іинт	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	VI = EVDDO				1	μΑ
	ILIH2	P20 to P27, P1 <u>37,</u> P150 to P156, RESET	$V_{I} = V_{DD}$				1	μΑ
	Ішнз	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VDD	In input port or external clock input			1	μΑ
				In resonator connection			10	μΑ
Input leakage current, low	lut1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Vı = EVsso				-1	μΑ
	ILIL2	P20 to P27, P137, P150 to P156, RESET	Vı = Vss				-1	μΑ
	Ішз	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	Vı = Vss	In input port or external clock input			-1	μΑ
				In resonator connection			-10	μΑ
On-chip pll-up resistance	R∪	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Vı = EVsso	, In input port	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes 1. Total current flowing into VDD, EVDDO, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDO, and EVDD1, or Vss, EVSSO, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. During HALT instruction execution by flash memory.
 - 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 4. When high-speed system clock and subsystem clock are stopped.
 - **5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - **7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz to } 32 \text{ MHz}$ $2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz to } 16 \text{ MHz}$ LS (low-speed main) mode: $1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz to } 8 \text{ MHz}$ LV (low-voltage main) mode: $1.6 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz to } 4 \text{ MHz}$

- **8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - **4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(Ta = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Items	Symbol		Conditions	·	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum	Тсч	Main	HS (high-	$2.7V\!\leq\!V_{DD}\!\leq\!5.5V$	0.03125		1	μS
instruction execution time)		system clock (fmain)	speed main) mode	$2.4 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	0.0625		1	μS
		operation	LS (low-speed main) mode	$1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}$	0.125		1	μS
			LV (low- voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μS
		Subsystem of	clock (fsuв)	1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μS
		operation						
		In the self	HS (high-	$2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}$	0.03125		1	μS
		programming mode	speed main) mode	$2.4 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	0.0625		1	μS
			LS (low-speed main) mode	$1.8 V \le V_{DD} \le 5.5 V$	0.125		1	μS
			LV (low- voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μS
External system clock	fex	2.7 V ≤ V _{DD} ≤	≤ 5.5 V		1.0		20.0	MHz
frequency		2.4 V ≤ V _{DD} <			1.0		16.0	MHz
		1.8 V ≤ V _{DD} <	< 2.4 V		1.0		8.0	MHz
		1.6 V ≤ V _{DD} <			1.0		4.0	MHz
	fexs				32		35	kHz
External system clock input	texh, texl	2.7 V ≤ V _{DD} ≤	≤ 5.5 V		24			ns
nigh-level width, low-level width		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} <	< 1.8 V		120			ns
	texhs, texhs				13.7			μS
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	tтін, tтіL				1/fмск+10			ns ^{Note}
TO00 to TO07, TO10 to TO17	fто	HS (high-spe	eed 4.0 V	≤ EV _{DD0} ≤ 5.5 V			16	MHz
output frequency		main) mode	2.7 V	≤ EV _{DD0} < 4.0 V			8	MHz
			1.8 V	≤ EV _{DD0} < 2.7 V			4	MHz
			1.6 V	≤ EV _{DD0} < 1.8 V			2	MHz
		LS (low-spec	ed 1.8 V	$\leq EV_{DD0} \leq 5.5 V$			4	MHz
		main) mode	1.6 V	≤ EV _{DD0} < 1.8 V			2	MHz
		LV (low-volta main) mode	age 1.6 V	\leq EV _{DD0} \leq 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output	fpcL	HS (high-spe	eed 4.0 V	$\leq EV_{DD0} \leq 5.5 V$			16	MHz
frequency		main) mode		≤ EV _{DD0} < 4.0 V			8	MHz
				≤ EV _{DD0} < 2.7 V			4	MHz
				≤ EV _{DD0} < 1.8 V			2	MHz
		LS (low-spec		\leq EV _{DD0} \leq 5.5 V			4	MHz
		main) mode	_	≤ EV _{DD0} < 1.8 V			2	MHz
		LV (low-volta main) mode		\leq EV _{DD0} \leq 5.5 V \leq EV _{DD0} $<$ 1.8 V			2	MHz MHz
Interrupt input high-level width,	tinth,	INTP0		≤ V _{DD} ≤ 5.5 V	1		=	μS
low-level width	tintl	INTP1 to INT		≤ EV _{DD0} ≤ 5.5 V	1			μS
Karrintanının tianın tarınlarınl	tkr	KR0 to KR7		≤ EV _{DD0} ≤ 5.5 V	250			ns
Key interrupt input low-level					1		1	
Key interrupt input low-level width			1.6 V	≤ EV _{DD0} < 1.8 V	1			μS

(Note and Remark are listed on the next page.)



(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Parameter	Symbo		Conditions	HS (high main)		LS (low-sp Mo	,	LV (low-vol		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	tsık2	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1/fмск+2 0		1/fмск+30		1/fмск+30		ns
		1.8 V ≤ E	$EV_{DD0} \le 5.5 \text{ V}$	1/fмск+3 0		1/fмск+30		1/fмск+30		ns
		1.7 V ≤ E	$EV_{DD0} \le 5.5 \text{ V}$	1/fмск+4 0		1/fмск+40		1/fмск+40		ns
		1.6 V ≤	EV _{DD0} ≤ 5.5 V	_		1/fмск+40		1/fмск+40		ns
Slp hold time (from SCKp↑)	tksi2	1.8 V ≤ E	EV _{DD0} ≤ 5.5 V	1/fмск+3 1		1/fмск+31		1/fмск+31		ns
Note 2		1.7 V ≤ E	7 V ≤ EV _{DD0} ≤ 5.5 V			1/fмск+ 250		1/fмск+ 250		ns
		1.6 V ≤	$EV_{DD0} \le 5.5 V$	_		1/fмск+ 250		1/fмск+ 250		ns
Delay time from SCKp↓ to	tkso2	C = 30 pF Note 4	$2.7~V \leq EV_{DD0} \leq 5.5$ V		2/f _{MCK+} 44		2/f _{MCK+} 110		2/f _{MCK+} 110	ns
SOp output Note			$2.4~V \le EV_{DD0} \le 5.5$ V		2/fмск+ 75		2/fмск+ 110		2/fмск+ 110	ns
			$1.8~V \le EV_{DD0} \le 5.5$ V		2/fмск+ 110		2/fмск+ 110		2/fмск+ 110	ns
		1	1.7 V ≤ EV _{DD0} ≤ 5.5 V		2/fмск+ 220		2/fмск+ 220		2/fмск+ 220	ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V		_		2/fмск+ 220		2/fмск+ 220	ns

- **Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 4. C is the load capacitance of the SOp output lines.
 - 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- **Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 - 2. fmck: Serial array unit operation clock frequency

 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

 n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Parameter	Symbol		Conditions		speed	high- I main) ode		/-speed Mode	voltage	low- e main) ode	Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Recep- tion	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ $2.7 \text{ V} \le \text{V}_{\text{b}} \le 4.0 \text{ V}$			fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
				Theoretical value of the maximum transfer rate fmck = fclk Note 4		5.3		1.3		0.6	Mbps
			$2.7 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V},$ $2.3 \text{ V} \le \text{V}_{\text{b}} \le 2.7 \text{ V}$			fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
				Theoretical value of the maximum transfer rate folk Note 4		5.3		1.3		0.6	Mbps
			$1.8 \ V \le EV_{DD0} < 3.3 \ V,$ $1.6 \ V \le V_b \le 2.0 \ V$			fMCK/6 Notes 1 to 3		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
				Theoretical value of the maximum transfer rate fmck = fclk Note 4		5.3		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

- 2. Use it with EVDD0≥Vb.
- 3. The following conditions are required for low voltage interface when $E_{VDDO} < V_{DD}$.

 $2.4 \text{ V} \le \text{EV}_{\text{DD0}} < 2.7 \text{ V} : \text{MAX. } 2.6 \text{ Mbps}$ $1.8 \text{ V} \le \text{EV}_{\text{DD0}} < 2.4 \text{ V} : \text{MAX. } 1.3 \text{ Mbps}$

4. The maximum operating frequencies of the CPU/peripheral hardware clock (fclk) are:

HS (high-speed main) mode: 32 MHz (2.7 V \leq V_{DD} \leq 5.5 V)

16 MHz (2.4 V \leq V_{DD} \leq 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V \leq V_{DD} \leq 5.5 V) LV (low-voltage main) mode: 4 MHz (1.6 V \leq V_{DD} \leq 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (Vpd tolerance (When 20- to 52-pin products)/EVpd tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For ViH and ViL, see the DC characteristics with TTL input buffer selected.

Remarks 1. $V_b[V]$: Communication line voltage

- 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- 3. fmcκ: Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,n: Channel number (mn = 00 to 03, 10 to 13)
- **4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.7 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Parameter	Symbol	Conditions		h-speed Mode	,	v-speed Mode	•	-voltage Mode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 2	tsıkı	$4.0~V \leq EV_{DD0} \leq 5.5~V,$ $2.7~V \leq V_b \leq 4.0~V,$	23		110		110		ns
		$C_b = 20 \text{ pF}, R_b = 1.4 \text{ k}\Omega$							
		$ 2.7 \ V \leq EV_{DD0} < 4.0 \ V, $ $ 2.3 \ V \leq V_b \leq 2.7 \ V, $	33		110		110		ns
		$C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$							
SIp hold time tksi1 (from SCKp↓) Note 2		$ 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, $ $ 2.7 \ V \leq V_b \leq 4.0 \ V, $	10		10		10		ns
		$C_b = 20 \text{ pF}, R_b = 1.4 \text{ k}\Omega$							
		$2.7 \ V \leq EV_{DD0} < 4.0 \ V,$ $2.3 \ V \leq V_b \leq 2.7 \ V,$	10		10		10		ns
		$C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$							
Delay time from SCKp↑ to	tkso1	$4.0~V \leq EV_{DD0} \leq 5.5~V,$ $2.7~V \leq V_b \leq 4.0~V,$		10		10		10	ns
SOp output Note 2		$C_b = 20 \text{ pF}, R_b = 1.4 \text{ k}\Omega$							
		$2.7 \ V \leq EV_{DD0} < 4.0 \ V,$ $2.3 \ V \leq V_b \leq 2.7 \ V,$		10		10		10	ns
		$C_b = 20 \text{ pF}, R_b = 2.7 \text{ k}\Omega$							

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (When 20- to 52-pin products)/EVDD tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

- **Remarks 1.** $R_b[\Omega]$:Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 - 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
 - 3. fmck: Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,n: Channel number (mn = 00))
 - 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(2) I2C fast mode

(Ta = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Сог	nditions	, ,	h-speed Mode	`	/-speed Mode	`	-voltage Mode	Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fscL	Fast mode:	$2.7~V \leq EV_{DD0} \leq 5.5~V$	0	400	0	400	0	400	kHz
		fc∟κ≥ 3.5 MHz	1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart	tsu:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0.6		0.6		0.6		μS
condition		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0.6		0.6		0.6		μS
Hold time ^{Note 1}	thd:sta	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0.6		0.6		0.6		μS
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0.6		0.6		0.6		μS
Hold time when SCLA0 =	tLOW	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	1.3		1.3		1.3		μS
" <u>L</u> "		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	1.3		1.3		1.3		μS	
Hold time when SCLA0 =	t HIGH	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0.6		0.6		0.6		μS
"H"		1.8 V ≤ EV _{DD0} ≤ 5.8	5 V	0.6		0.6		0.6		μS
Data setup time	tsu:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	100		100		100		μS
(reception)		1.8 V ≤ EV _{DD0} ≤ 5.8	5 V	100		100		100		μS
Data hold time	thd:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0	0.9	0	0.9	0	0.9	μS
(transmission)Note 2		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	0	0.9	0	0.9	0	0.9	μS
Setup time of stop	tsu:sto	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.$	5 V	0.6		0.6		0.6		μS
condition		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.$	1.8 V ≤ EV _{DD0} ≤ 5.5 V			0.6		0.6		μS
Bus-free time	t BUF	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.8$	5 V	1.3		1.3		1.3		μS
		$1.8 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.8$	5 V	1.3		1.3		1.3		μS

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of thd:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IoH1, IoL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b = 320 \text{ pF}, R_b = 1.1 \text{ k}\Omega$

<R>

LVD Detection Voltage of Interrupt & Reset Mode

(Ta = -40 to +85°C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol		Cond	litions	MIN.	TYP.	MAX.	Unit
Interrupt and reset	V _{LVDA0}	V _{POC2} ,	VPOC1, VPOC0 = 0, 0, 0	, falling reset voltage	1.60	1.63	1.66	V
mode	VLVDA1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVDB0}	V _{POC2} ,	VPOC1, VPOC0 = 0, 0, 1	, falling reset voltage	1.80	1.84	1.87	V
	V _{LVDB1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V	
	VLVDB2	LVDB2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V LVDB3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVDC0}	V _{POC2} ,	VPOC1, VPOC0 = 0, 1, 0	, falling reset voltage	2.40	2.45	2.50	V
	VLVDC1		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDC3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVDD0}	V _{POC2} ,	VPOC1, VPOC0 = 0, 1, 1	, falling reset voltage	2.70	2.75	2.81	V
	V _{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	VLVDD3		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V



- Notes 1. Total current flowing into VDD and EVDDO, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDO or Vss, EVsso. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 3. When high-speed system clock and subsystem clock are stopped.
 - **4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - **5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 32 MHz $2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 16 MHz

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fih: High-speed on-chip oscillator clock frequency
 - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - 4. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (Ta = -40 to +105°C, 2.4 V \leq EVDD0 \leq VDD \leq 5.5 V, Vss = EVss0 = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	I _{DD2}	HALT	HS (high-	fih = 32 MHz Note 4	V _{DD} = 5.0 V		0.54	2.90	mA
current	Note 2	mode	speed main) mode Note 7		V _{DD} = 3.0 V		0.54	2.90	mA
				fih = 24 MHz Note 4	V _{DD} = 5.0 V		0.44	2.30	mA
					V _{DD} = 3.0 V		0.44	2.30	mA
				fih = 16 MHz Note 4	V _{DD} = 5.0 V		0.40	1.70	mA
					V _{DD} = 3.0 V		0.40	1.70	mA
			HS (high-	$f_{MX} = 20 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.28	1.90	mA
			speed main) mode Note 7	V _{DD} = 5.0 V	Resonator connection		0.45	2.00	mA
				$f_{MX} = 20 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.28	1.90	mA
				V _{DD} = 3.0 V	Resonator connection		0.45	2.00	mA
				$f_{MX} = 10 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.19	1.02	mA
				V _{DD} = 5.0 V	Resonator connection		0.26	1.10	mA
				$f_{MX} = 10 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.19	1.02	mA
				V _{DD} = 3.0 V	Resonator connection		0.26	1.10	mA
	Subsyster	Subsystem	fsub = 32.768 kHz ^{Note 5}	Square wave input		0.25	0.57	μА	
			clock	T _A = -40°C	Resonator connection		0.44	0.76	μА
			operation	fsub = 32.768 kHz ^{Note 5}	Square wave input		0.30	0.57	μА
				T _A = +25°C	Resonator connection		0.49	0.76	μА
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.37	1.17	μА
				T _A = +50°C	Resonator connection		0.56	1.36	μА
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.53	1.97	μА
				T _A = +70°C	Resonator connection		0.72	2.16	μА
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.82	3.37	μА
				T _A = +85°C	Resonator connection		1.01	3.56	μА
				fsub = 32.768 kHz ^{Note 5}	Square wave input		3.01	15.37	μА
				T _A = +105°C	Resonator connection		3.20	15.56	μА
	IDD3 ^{Note 6}	STOP	T _A = -40°C				0.18	0.50	μА
		mode ^{Note 8}	T _A = +25°C				0.23	0.50	μА
			T _A = +50°C				0.30	1.10	μА
			T _A = +70°C				0.46	1.90	μА
	T _A = +		T _A = +85°C			0.75	3.30	μА	
			T _A = +105°C				2.94	15.30	μА

(Notes and Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

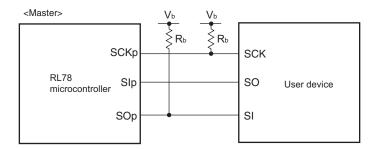
 $(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t ксу1	tkcy1 ≥ 4/fclk	$4.0~V \leq EV_{DD0} \leq 5.5~V,~2.7~V \leq V_b \leq 4.0$ $V,$ $C_b = 30~pF,~R_b = 1.4~k\Omega$	600		ns
			$2.7~V \leq EV_{DD0} < 4.0~V,~2.3~V \leq V_b \leq 2.7$ $V,$ $C_b = 30~pF,~R_b = 2.7~k\Omega$	1000		ns
			$2.4~V \leq EV_{DD0} < 3.3~V,~1.6~V \leq V_b \leq 2.0$ $V,$ $C_b = 30~pF,~R_b = 5.5~k\Omega$	2300		ns
SCKp high-level width	t кн1	$4.0~V \leq EV_{DD0} \leq 5.5~V,~2.7~V \leq V_b \leq 4.0~V,$ $C_b = 30~pF,~R_b = 1.4~k\Omega$		tксу1/2 - 150		ns
		$2.7~V \leq EV_{DD0} < 4.0~V,~2.3~V \leq V_b \leq 2.7~V,$ $C_b = 30~pF,~R_b = 2.7~k\Omega$		tkcy1/2 - 340		ns
		$2.4~V \leq EV_{DD0} < 3.3~V,~1.6~V \leq V_b \leq 2.0~V,$ $C_b = 30~pF,~R_b = 5.5~k\Omega$		tксу1/2 – 916		ns
SCKp low-level width	t _{KL1}	$4.0~V \leq EV_{DD0} \leq 5.5~V,~2.7~V \leq V_b \leq 4.0~V,$ $C_b = 30~pF,~R_b = 1.4~k\Omega$		tkcy1/2 - 24		ns
		$2.7~V \leq EV_{DD0} < 4.0~V,~2.3~V \leq V_b \leq 2.7~V,$ $C_b = 30~pF,~R_b = 2.7~k\Omega$		tkcy1/2 - 36		ns
		$2.4~V \leq \text{EV}_{\text{DDO}} < 3.3~V,~1.6~V \leq V_b \leq 2.0~V,$ $C_b = 30~\text{pF},~R_b = 5.5~\text{k}\Omega$		tксу1/2 — 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (Vpd tolerance (for the 20- to 52-pin products)/EVpd tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

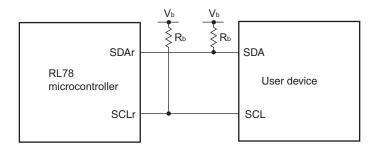
(Remarks are listed two pages after the next page.)

CSI mode connection diagram (during communication at different potential)

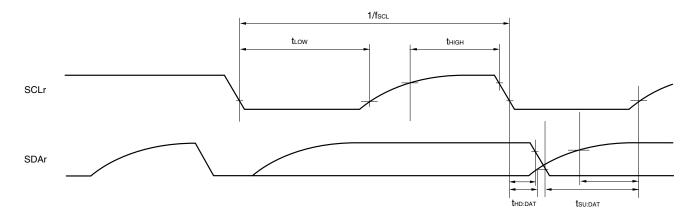


- Remarks 1. $R_b[\Omega]$:Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 - 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 - 3. fmck: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
 - **4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (VDD tolerance (for the 20- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (VDD tolerance (for the 20- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VH and VIL, see the DC characteristics with TTL input buffer selected.

- **Remarks 1.** R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage
 - 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 - 3. fmck: Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,n: Channel number (mn = 00, 01, 02, 10, 12, 13)

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