Renesas Electronics America Inc - R5F101LCDFB#30 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lcdfb-30

Table 1-1. List of Ordering Part Numbers

(8/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJAFA#V0, R5F100LKAFA#V0, R5F100LLAFA#V0 R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0,
			D	R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJAFA#X0, R5F100LKAFA#X0, R5F100LLAFA#X0 R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDFA#V0, R5F100LHDFA#V0, R5F100LJDFA#V0, R5F100LKDFA#V0, R5F100LLDFA#V0
			G	R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDFA#X0, R5F100LHDFA#X0, R5F100LJDFA#X0, R5F100LKDFA#X0, R5F100LLDFA#X0 R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0 R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0 R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0 R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJAFA#V0, R5F101LKAFA#V0, R5F101LLAFA#V0 R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0,
			D	R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJAFA#X0, R5F101LKAFA#X0, R5F101LLAFA#X0 R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDFA#V0, R5F101LHDFA#V0, R5F101LJDFA#V0, R5F101LKDFA#V0, R5F101LLDFA#V0 R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDFA#X0, R5F101LHDFA#X0, R5F101LJDFA#X0, R5F101LKDFA#X0, R5F101LLDFA#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

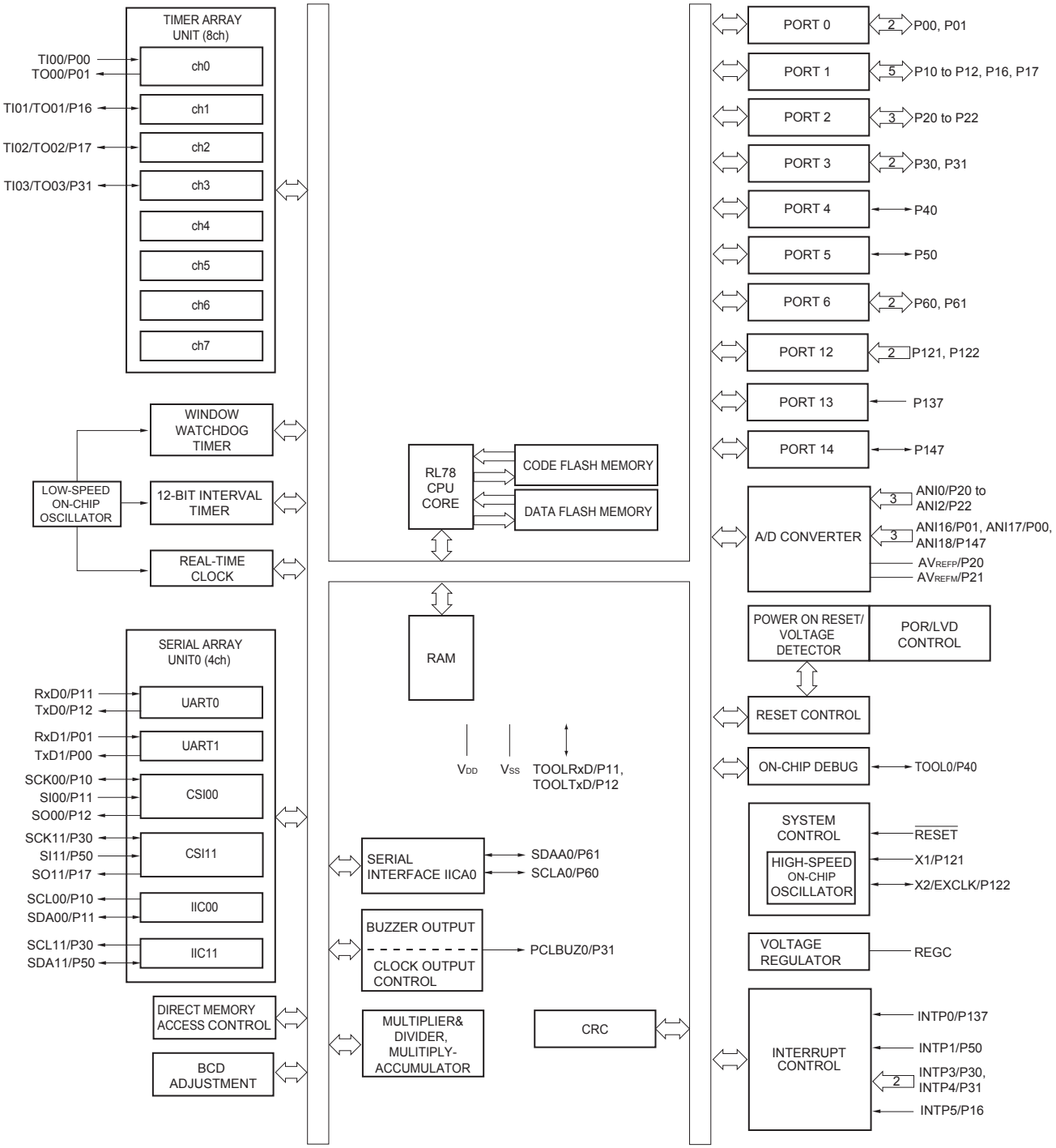
(10/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGAFA#V0, R5F100MHAFA#V0, R5F100MJAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGAFA#X0, R5F100MHAFA#X0, R5F100MJAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0
			D	R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0
			G	R5F100MFGFA#V0, R5F100MGGFA#V0, R5F100MHGFA#V0, R5F100MJGFA#V0 R5F100MFGFA#X0, R5F100MGGFA#X0, R5F100MHGFA#X0, R5F100MJGFA#X0
		Not mounted	A	R5F101MFAFA#V0, R5F101MGAFA#V0, R5F101MHAFA#V0, R5F101MJAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGAFA#X0, R5F101MHAFA#X0, R5F101MJAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0
			D	R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0
			D	R5F100MFDFB#V0, R5F100MGDFB#V0, R5F100MHDFB#V0, R5F100MJDFB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDFB#X0, R5F100MGDFB#X0, R5F100MHDFB#X0, R5F100MJDFB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0
			G	R5F100MFGFB#V0, R5F100MGGFB#V0, R5F100MHGFB#V0, R5F100MJGFB#V0 R5F100MFGFB#X0, R5F100MGGFB#X0, R5F100MHGFB#X0, R5F100MJGFB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0
			D	R5F101MFDFB#V0, R5F101MGDFB#V0, R5F101MHDFB#V0, R5F101MJDFB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDFB#X0, R5F101MGDFB#X0, R5F101MHDFB#X0, R5F101MJDFB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0

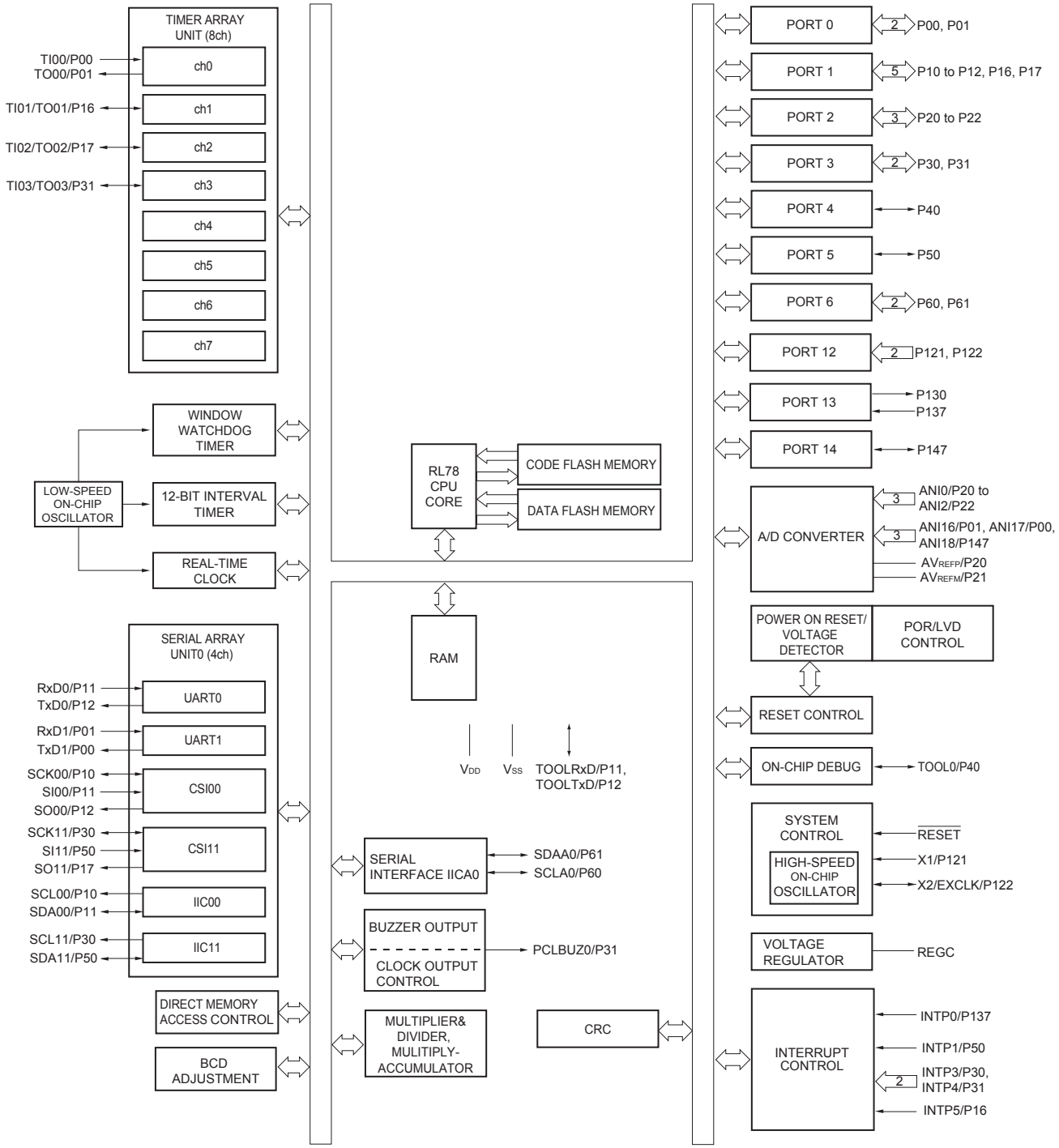
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

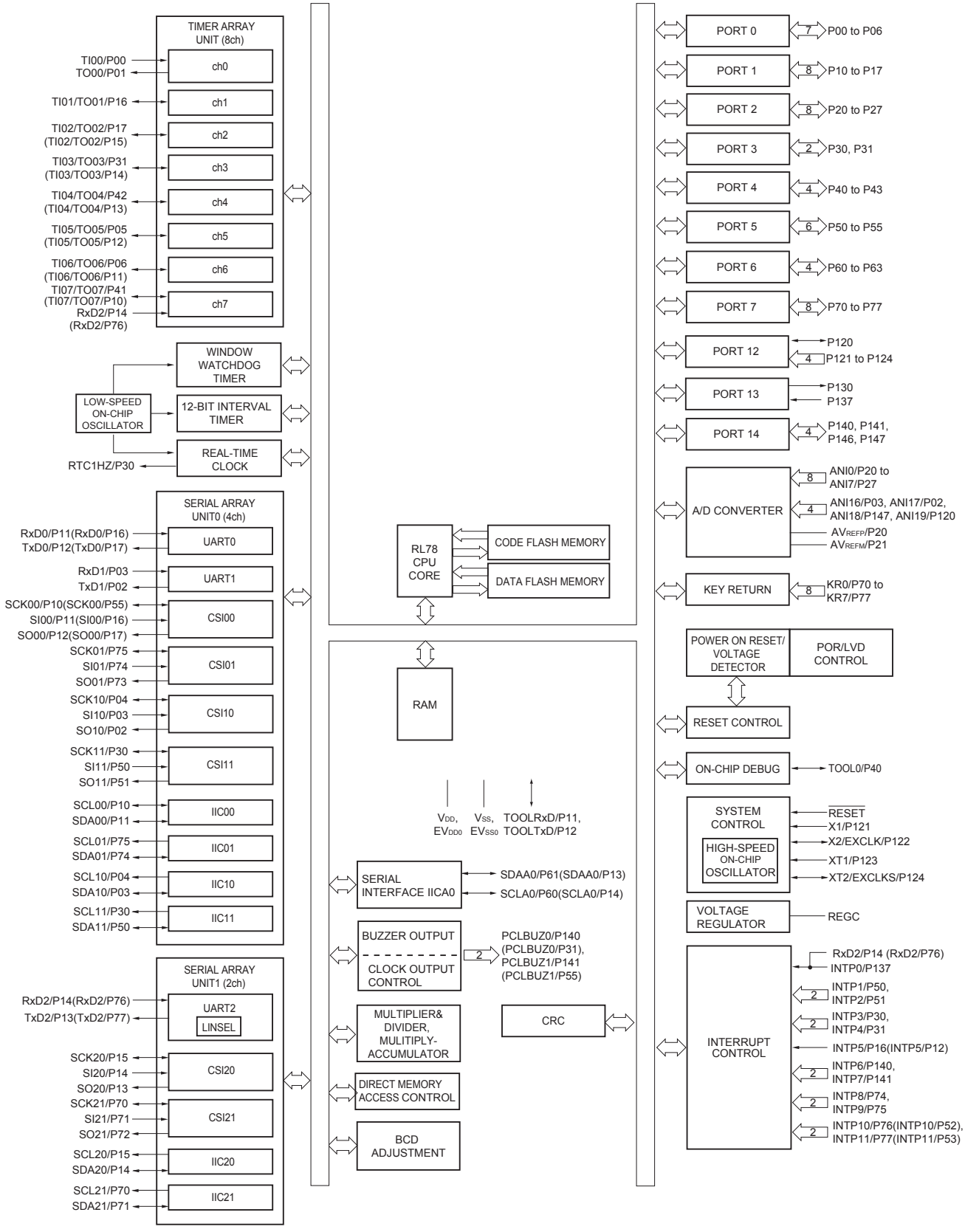
1.5.2 24-pin products



1.5.3 25-pin products



1.5.11 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4 Note1		2 to 4 Note1		2 to 4 Note1		2 to 12 Note1		2 to 12 Note1		2 to 12 Note1	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)											
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)											
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.											
I/O port	Total	16		20		21		26		28		32	
	CMOS I/O	13 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		21 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		22 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		26 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)	
	CMOS input	3		3		3		3		3		3	
	CMOS output	–		–		1		–		–		–	
	N-ch O.D. I/O (withstand voltage: 6 V)	–		2		2		2		3		3	
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel Note 2											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2 Note 3)		4 channels (PWM outputs: 3 Note 3)				4 channels (PWM outputs: 3 Note 3), 8 channels (PWM outputs: 7 Note 3) Note 4					
	RTC output	–											

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.3		mA
						V_{DD} = 3.0 V		2.3		mA
					Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.1	6.6	mA
						V_{DD} = 3.0 V		4.1	6.6	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.0	4.7	mA
						V_{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.1	mA
						V_{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(5) During communication at same potential (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		1850		1850		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		kHz
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		kHz
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		kHz
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Use it with $EV_{DD0} \geq V_b$.

3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T_A = –40 to +105°C
R5F100xxGxx

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.

4. Please contact Renesas Electronics sales office for derating of operation under T_A = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13 is used in the range of T_A = –40 to +85°C, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C)**.

There are following differences between the products "G: Industrial applications (T_A = –40 to +105°C)" and the products “A: Consumer applications, and D: Industrial applications”.

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	T_A = -40 to +85°C	T_A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V ±1.0%@ T_A = -20 to +85°C ±1.5%@ T_A = -40 to -20°C 1.6 V ≤ V_{DD} < 1.8 V ±5.0%@ T_A = -20 to +85°C ±5.5%@ T_A = -40 to -20°C	2.4 V ≤ V_{DD} ≤ 5.5 V ±2.0%@ T_A = +85 to +105°C ±1.0%@ T_A = -20 to +85°C ±1.5%@ T_A = -40 to -20°C
Serial array unit	UART CSI: f_{CLK}/2 (supporting 16 Mbps), f_{CLK}/4 Simplified I^2C communication	UART CSI: f_{CLK}/4 Simplified I^2C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(**Remark** is listed on the next page.)

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	−0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	−0.3 to EV_{DD0} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

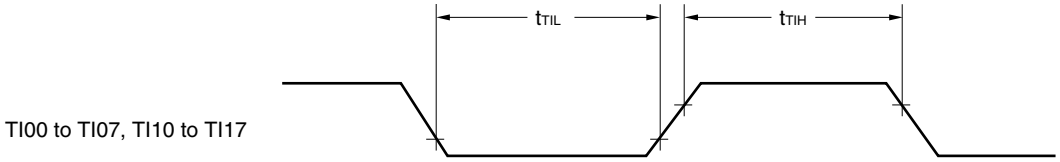
Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

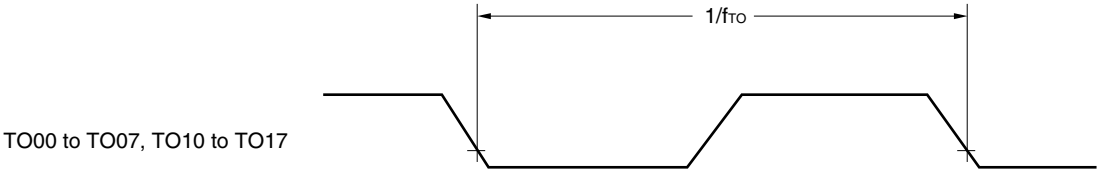
2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

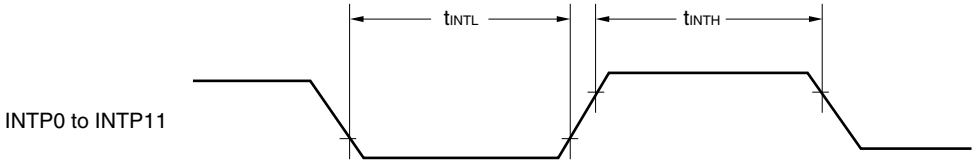
4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

TI/TO Timing

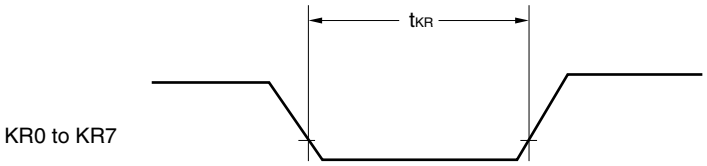




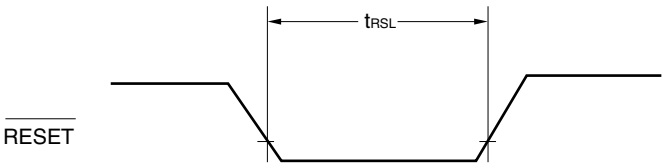
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.6 Note 2	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.4 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

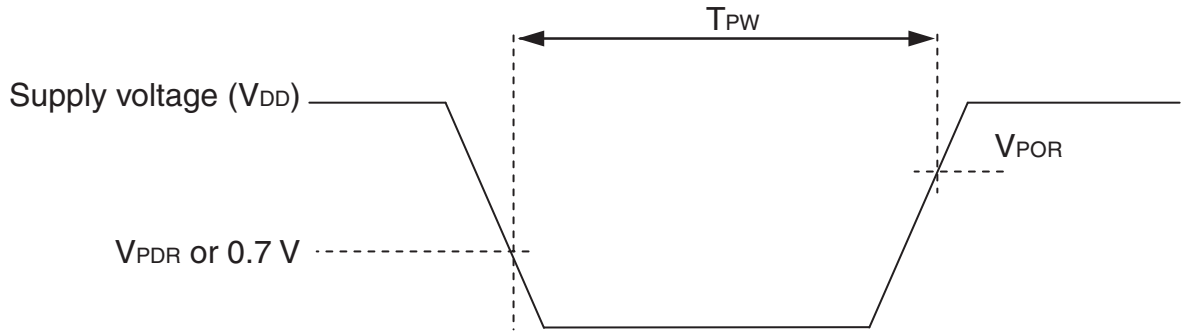
4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

3.6.3 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T_{PW}		300			μs

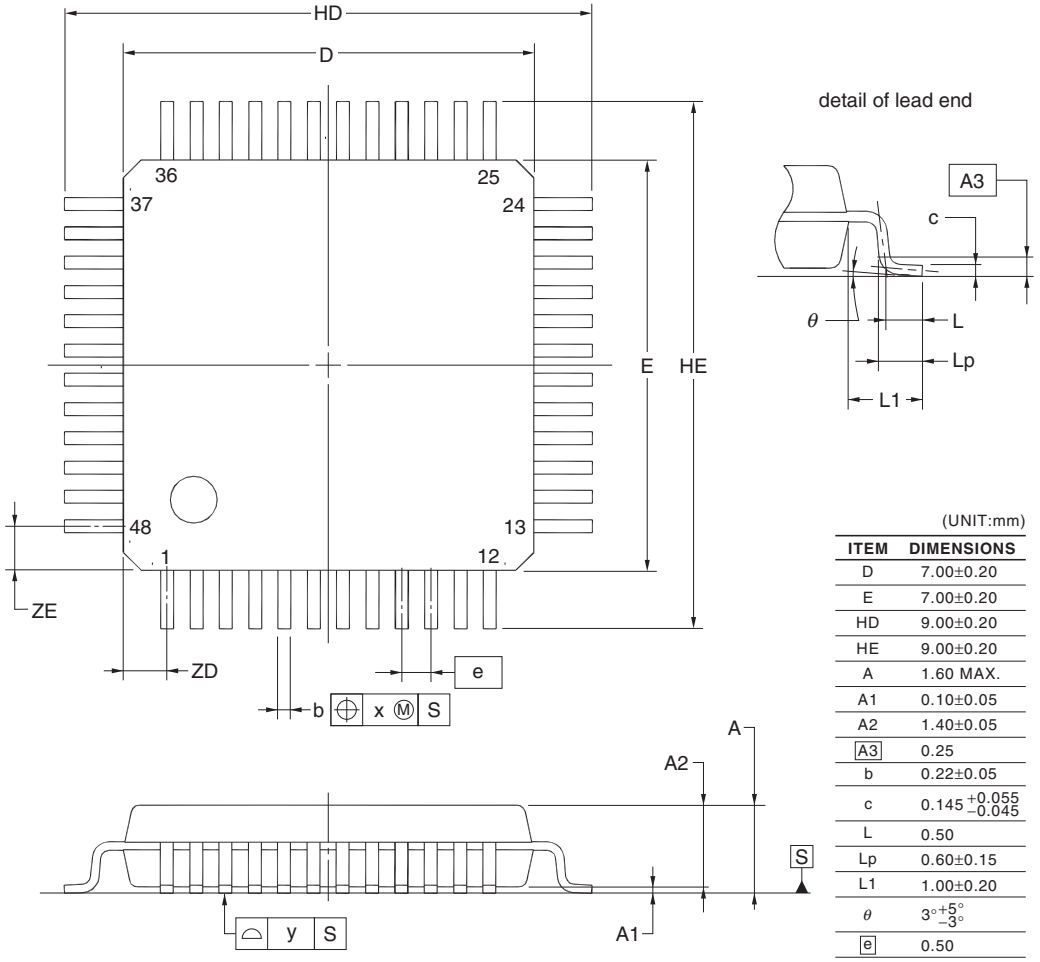
Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.9 48-pin Products

R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB, R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB
R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB, R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB
R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB, R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB, R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB
R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB, R5F100GHGFB, R5F100GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



(UNIT:mm)

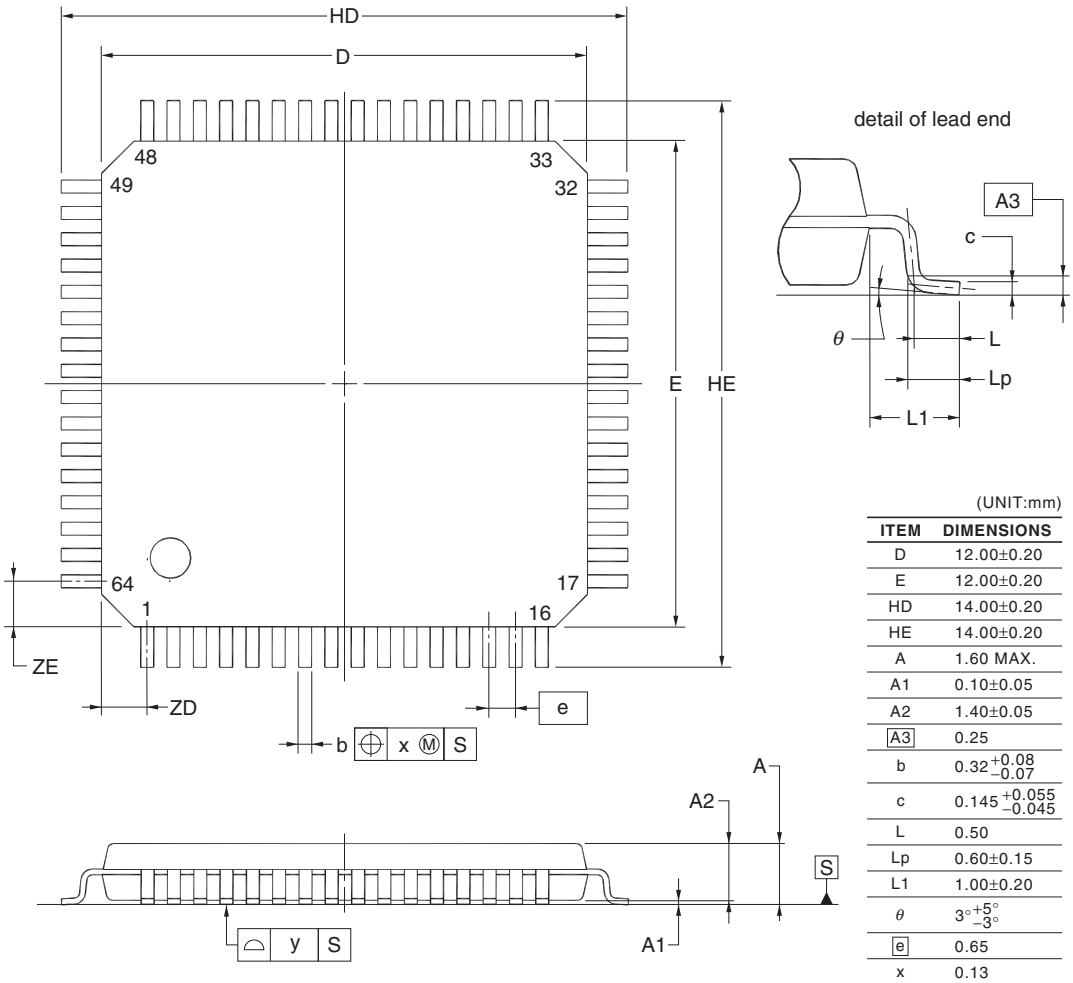
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA, R5F100LKAFA, R5F100LLAFA
R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA, R5F101LKAFA, R5F101LLAFA
R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LGDFA, R5F100LHDFA, R5F100LJDFA, R5F100LKDFA, R5F100LLDFA
R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LGDFA, R5F101LHDFA, R5F101LJDFA, R5F101LKDFA, R5F101LLDFA
R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA, R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{\text{ACK}}$ corrected to ACK
			$\overline{\text{ACK}}$ corrected to ACK