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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lcdfb-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lcdfb-x0</a>

Table 1-1. List of Ordering Part Numbers

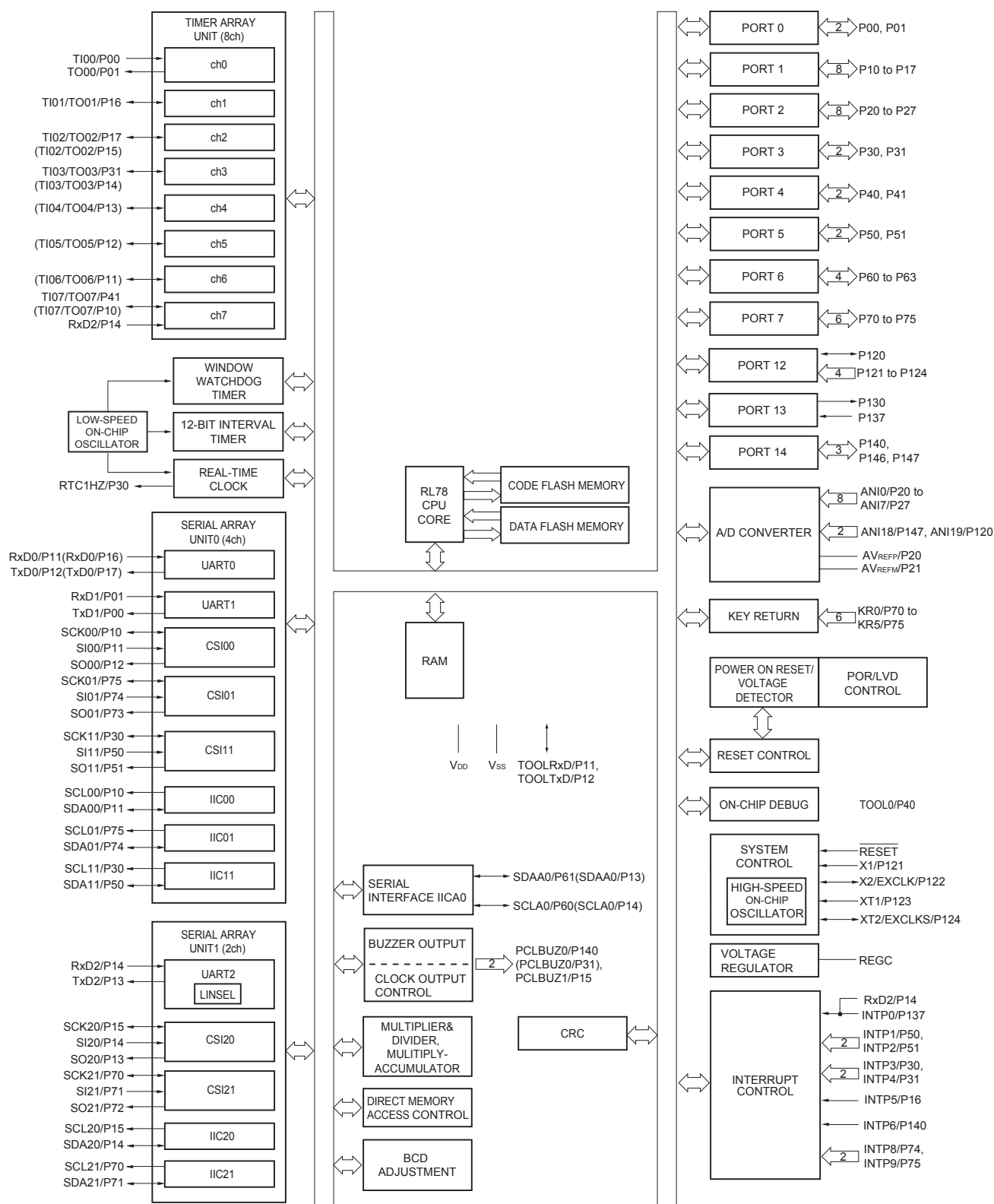
(11/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	Mounted	A	R5F100PFAFB#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0
			D	R5F100PFDFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJDFB#V0, R5F100PKDFA#V0, R5F100PLDFA#V0 R5F100PFDFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJDFB#X0, R5F100PKDFA#X0, R5F100PLDFA#X0
			G	R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0, R5F100PJGFB#V0 R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0, R5F100PJGFB#X0
		Not mounted	A	R5F101PFAFB#V0, R5F101PGAFA#V0, R5F101PHAFA#V0, R5F101PJAFB#V0, R5F101PKAFB#V0, R5F101PLAFB#V0 R5F101PFAFB#X0, R5F101PGAFA#X0, R5F101PHAFA#X0, R5F101PJAFB#X0, R5F101PKAFB#X0, R5F101PLAFB#X0
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	Mounted	A	R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFA#V0, R5F100PLAFA#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFA#X0, R5F100PLAFA#X0
			D	R5F100PFDFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJDFB#V0, R5F100PKDFA#V0, R5F100PLDFA#V0 R5F100PFDFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJDFB#X0, R5F100PKDFA#X0, R5F100PLDFA#X0
			G	R5F100PFGFA#V0, R5F100PGGFA#V0, R5F100PHGFA#V0, R5F100PJGFA#V0 R5F100PFGFA#X0, R5F100PGGFA#X0, R5F100PHGFA#X0, R5F100PJGFA#X0
		Not mounted	A	R5F101PFAFA#V0, R5F101PGAFA#V0, R5F101PHAFA#V0, R5F101PJAFB#V0, R5F101PKAFA#V0, R5F101PLAFA#V0 R5F101PFAFA#X0, R5F101PGAFA#X0, R5F101PHAFA#X0, R5F101PJAFB#X0, R5F101PKAFA#X0, R5F101PLAFA#X0
			D	R5F101PFDFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJDFB#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PFDFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJDFB#X0, R5F101PKDFA#X0, R5F101PLDFA#X0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

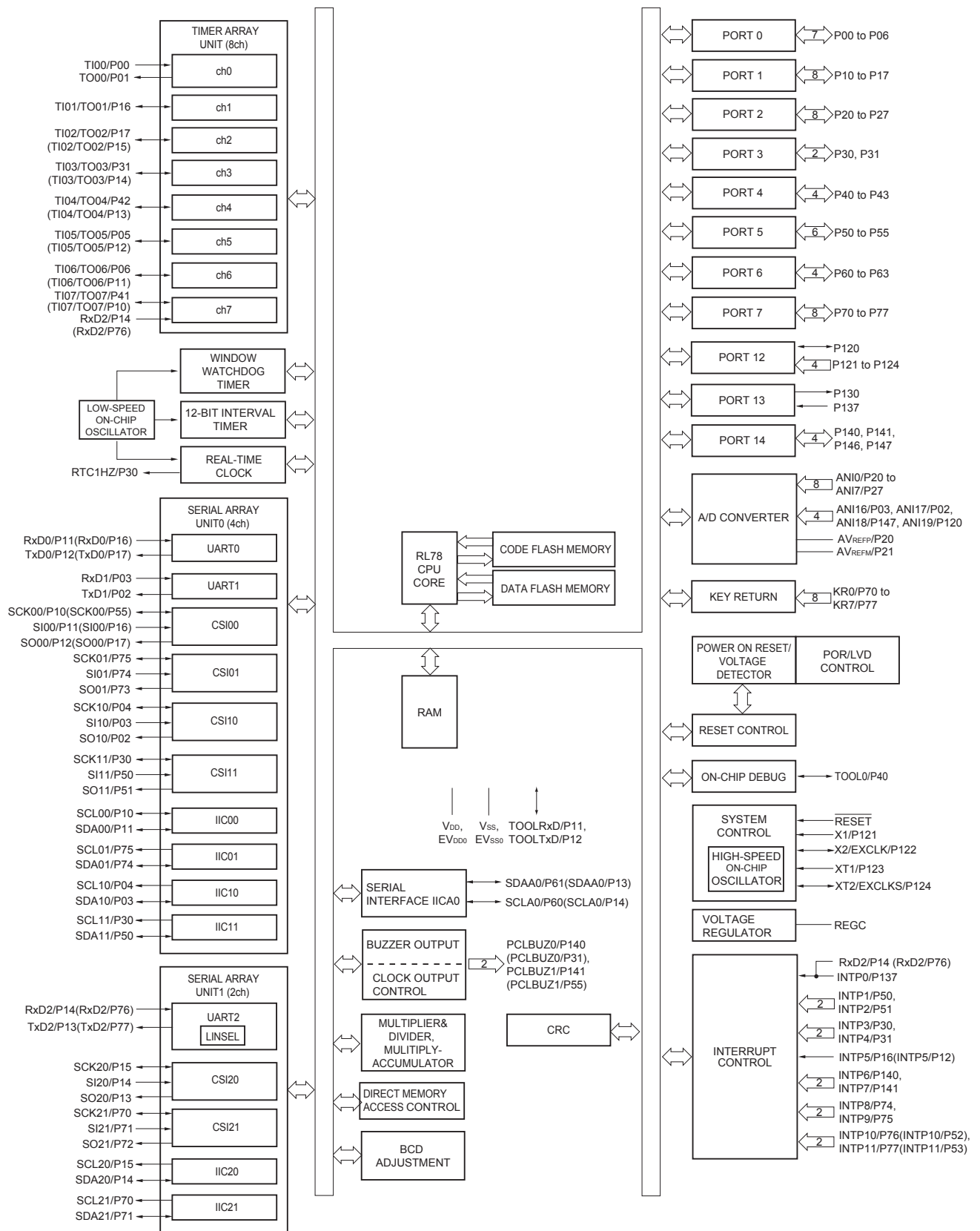
**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.5.9 48-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.11 64-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output	—		1		1		2		2		2	
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation)											
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface	[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I <sup>2</sup> C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I <sup>2</sup> C bus	—	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller	2 channels											
Vectored interrupt sources	Internal	23	24		24		27		27		27	
	External	3	5		5		6		6		6	
Key interrupt	—											
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector	• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function	Provided											
Power supply voltage	V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)											
Operating ambient temperature	T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications ) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)											

**Note** The illegal instruction is generated when instruction code FFH is executed.

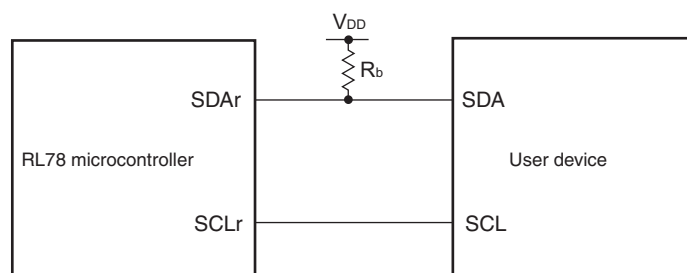
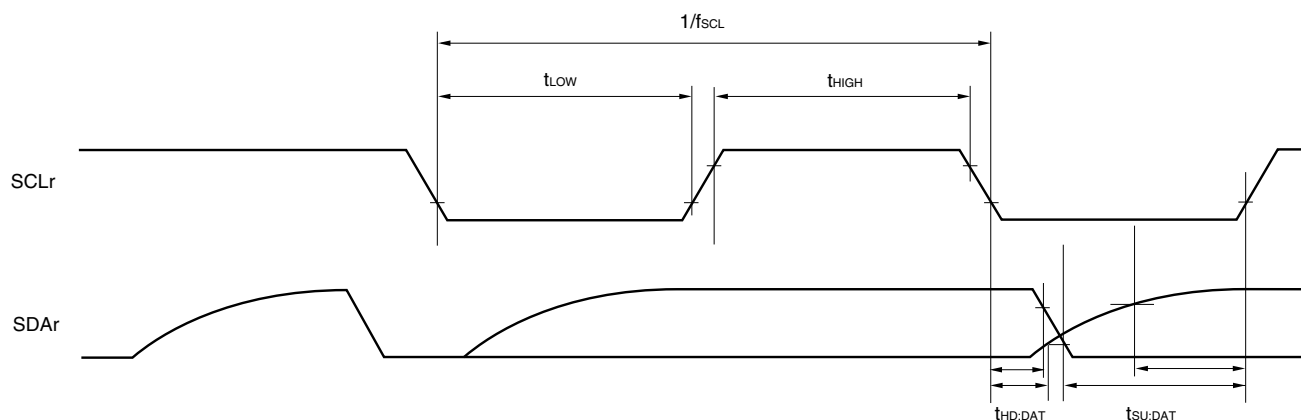
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I <sub>OL</sub> <sup>Note 1</sup>	I <sub>OL1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			20.0 <sup>Note 2</sup>	mA
		Per pin for P60 to P63			15.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		70.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		15.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		9.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		80.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		35.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		20.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )			150.0	mA
	I <sub>OL2</sub>	Per pin for P20 to P27, P150 to P156			0.4 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		5.0	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV<sub>SS0</sub>, EV<sub>SS1</sub> and V<sub>SS</sub> pin.
  2. However, do not exceed the total current value.
  3. Specification under conditions where the duty factor ≤ 70%.  
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
    - Total output current of pins = (I<sub>OL</sub> × 0.7)/(n × 0.01)
 <Example> Where n = 80% and I<sub>OL</sub> = 10.0 mA  
 Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA  
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor.  
 A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
  2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),  
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main)		LS (low-speed main)		LV (low-voltage main)		Unit	
				Mode		Mode		Mode			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		Transmission	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V			Note 1		Note 1		Note 1	bps
						2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V			Note 3		Note 3		Note 3	bps
						1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V			Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
						0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps



3. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> < 4.0 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.
6. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

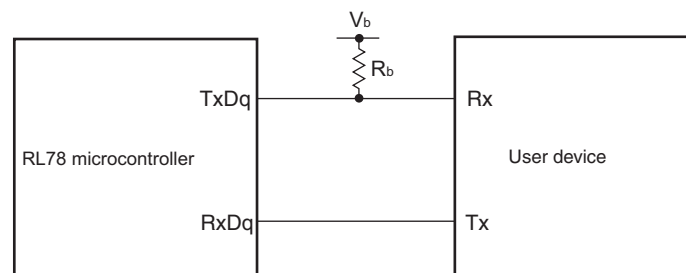
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

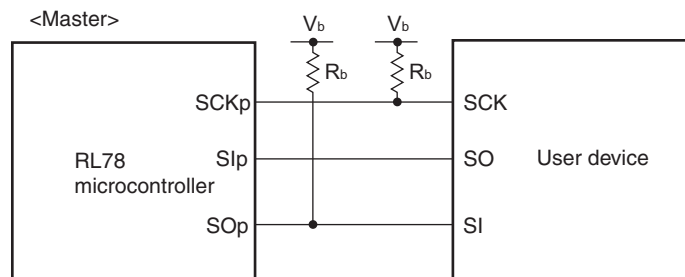
\* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the Rx<sub>Dq</sub> pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the Tx<sub>Dq</sub> pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

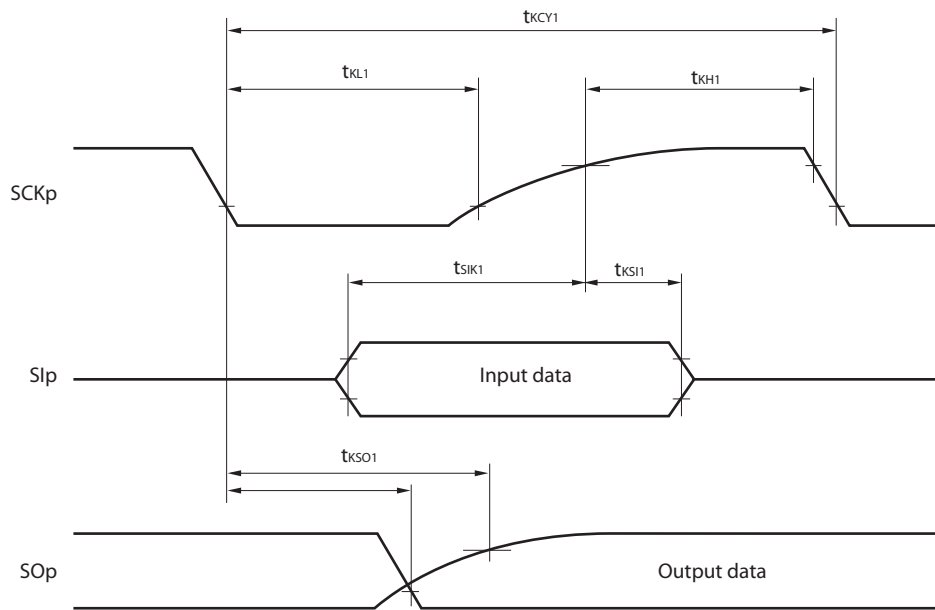
UART mode connection diagram (during communication at different potential)



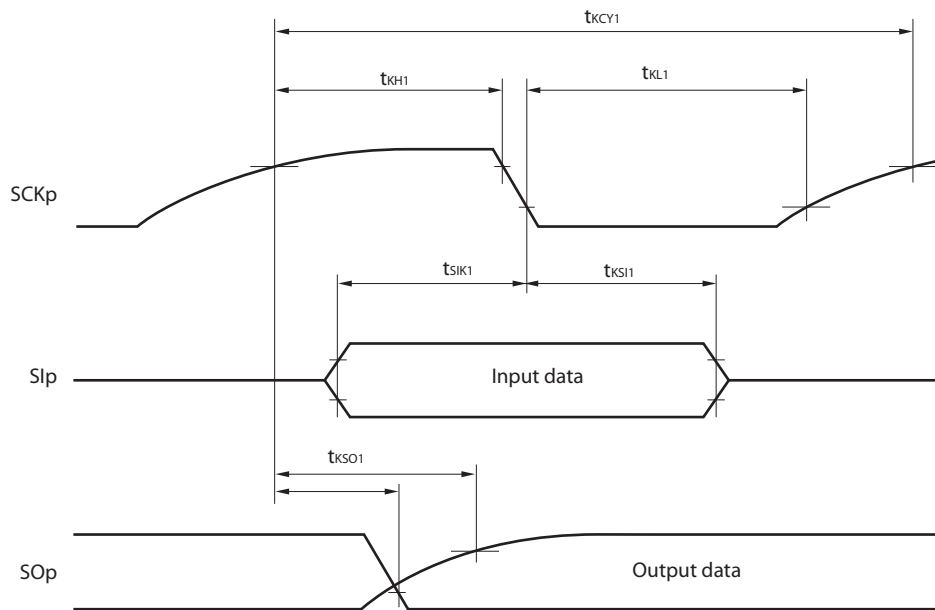
**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage
  2. p: CSI number ( $p = 00, 01, 10, 20, 30, 31$ ), m: Unit number, n: Channel number ( $mn = 00, 01, 02, 10, 12, 13$ ), g: PIM and POM number ( $g = 0, 1, 4, 5, 8, 14$ )
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number ( $mn = 00$ ))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

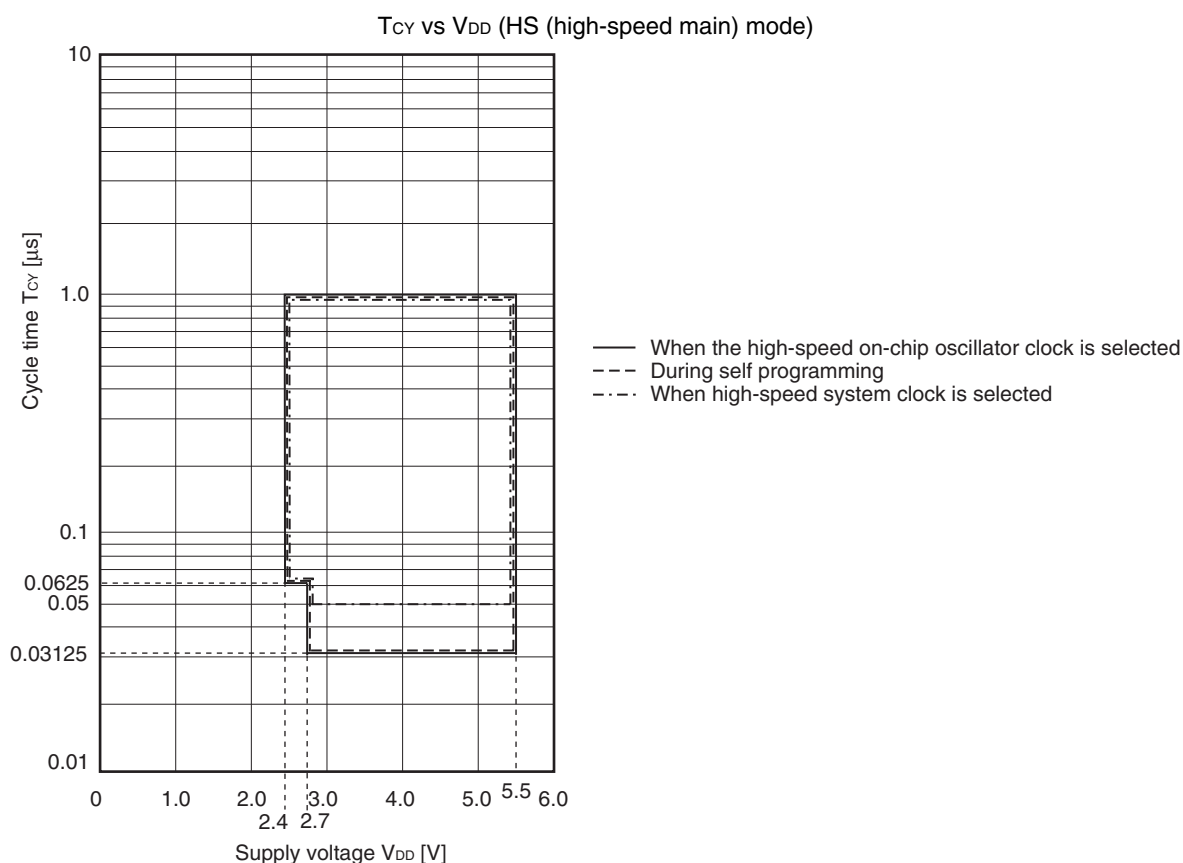
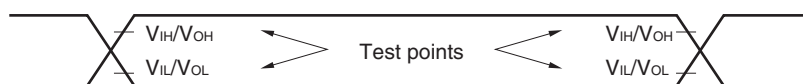
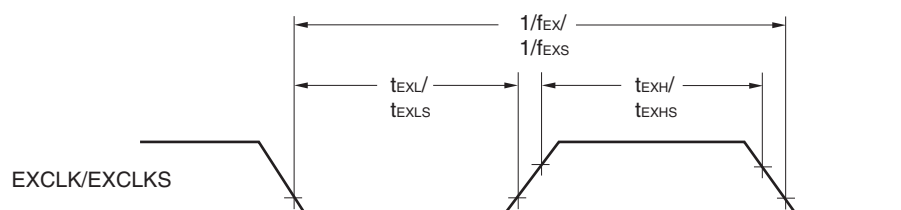
### 3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = V_{SS0} = 0\text{ V}$ ) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		2.1		mA
						$V_{DD} = 3.0\text{ V}$		2.1		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		4.6	7.5	mA
						$V_{DD} = 3.0\text{ V}$		4.6	7.5	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		3.7	5.8	mA
						$V_{DD} = 3.0\text{ V}$		3.7	5.8	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	4.2	mA
						$V_{DD} = 3.0\text{ V}$		2.7	4.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock operation		$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	$\mu\text{A}$
						Resonator connection		4.2	5.0	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	$\mu\text{A}$
						Resonator connection		4.2	5.0	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.2	5.5	$\mu\text{A}$
						Resonator connection		4.3	5.6	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	6.3	$\mu\text{A}$
						Resonator connection		4.4	6.4	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.6	7.7	$\mu\text{A}$
						Resonator connection		4.7	7.8	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7	$\mu\text{A}$
						Resonator connection		7.0	19.8	$\mu\text{A}$

(Notes and Remarks are listed on the next page.)

**Minimum Instruction Execution Time during Main System Clock Operation****AC Timing Test Points****External System Clock Timing**

5. The smaller maximum transfer rate derived by using  $f_{MCK}/12$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

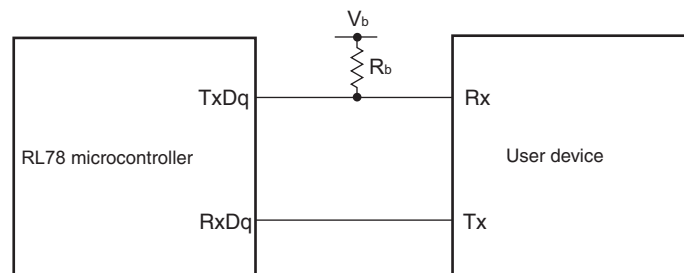
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

**UART mode connection diagram (during communication at different potential)**



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	$t_{\text{KCY1}}$	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	600		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	1000		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 5.5\text{ k}\Omega$	2300		ns
SCKp high-level width	$t_{\text{KH1}}$		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 150$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 340$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 916$		ns
SCKp low-level width	$t_{\text{KL1}}$		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 24$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 36$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 100$		ns

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $\text{V}_{\text{IH}}$  and  $\text{V}_{\text{IL}}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

## (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time <sup>Note 1</sup>	$t_{KCY2}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{MCK}$	$28/f_{MCK}$		ns
			$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$24/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$20/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{MCK}$	$40/f_{MCK}$		ns
			$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$32/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{MCK}$	$96/f_{MCK}$		ns
			$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$72/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$		ns
SCKp high-/low-level width	$t_{KH2}$ , $t_{KL2}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$t_{KCY2}/2 - 24$		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$t_{KCY2}/2 - 36$		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ <sup>Note 2</sup>		$t_{KCY2}/2 - 100$		ns
Slp setup time (to SCKp $\uparrow$ ) <sup>Note 2</sup>	$t_{SIK2}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$1/f_{MCK} + 40$		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note 3</sup>	$t_{KSI2}$			$1/f_{MCK} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 4</sup>	$t_{KSO2}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			$2/f_{MCK} + 240$	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$			$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$			$2/f_{MCK} + 1146$	ns

(Notes, Caution and Remarks are listed on the next page.)



**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ <small>Note 2</small>		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ <small>Note 2</small>		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.8\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ <small>Note 2</small>		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ <small>Note 2</small>		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 570$ <small>Note 2</small>		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	0	1215	ns

**Notes** 1. The value must also be equal to or less than  $f_{\text{MCK}}/4$ .2. Set the  $f_{\text{MCK}}$  value to keep the hold time of  $\text{SCLr} = \text{"L"}$  and  $\text{SCLr} = \text{"H"}$ .

**Caution** Select the TTL input buffer and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the  $\text{SDAr}$  pin and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the  $\text{SCLr}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $\text{V}_{\text{IH}}$  and  $\text{V}_{\text{IL}}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(3) When reference voltage (+) =  $V_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) =  $V_{SS}$  (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ , Reference voltage (–) =  $V_{SS}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	$\pm 7.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	E <sub>FS</sub>	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 4.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI0 to ANI14		0		$V_{DD}$	V
		ANI16 to ANI26		0		$EV_{DD0}$	V
		Internal reference voltage output ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{BGR}$ <sup>Note 3</sup>			V
		Temperature sensor output voltage ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{TMPS25}$ <sup>Note 3</sup>			V

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

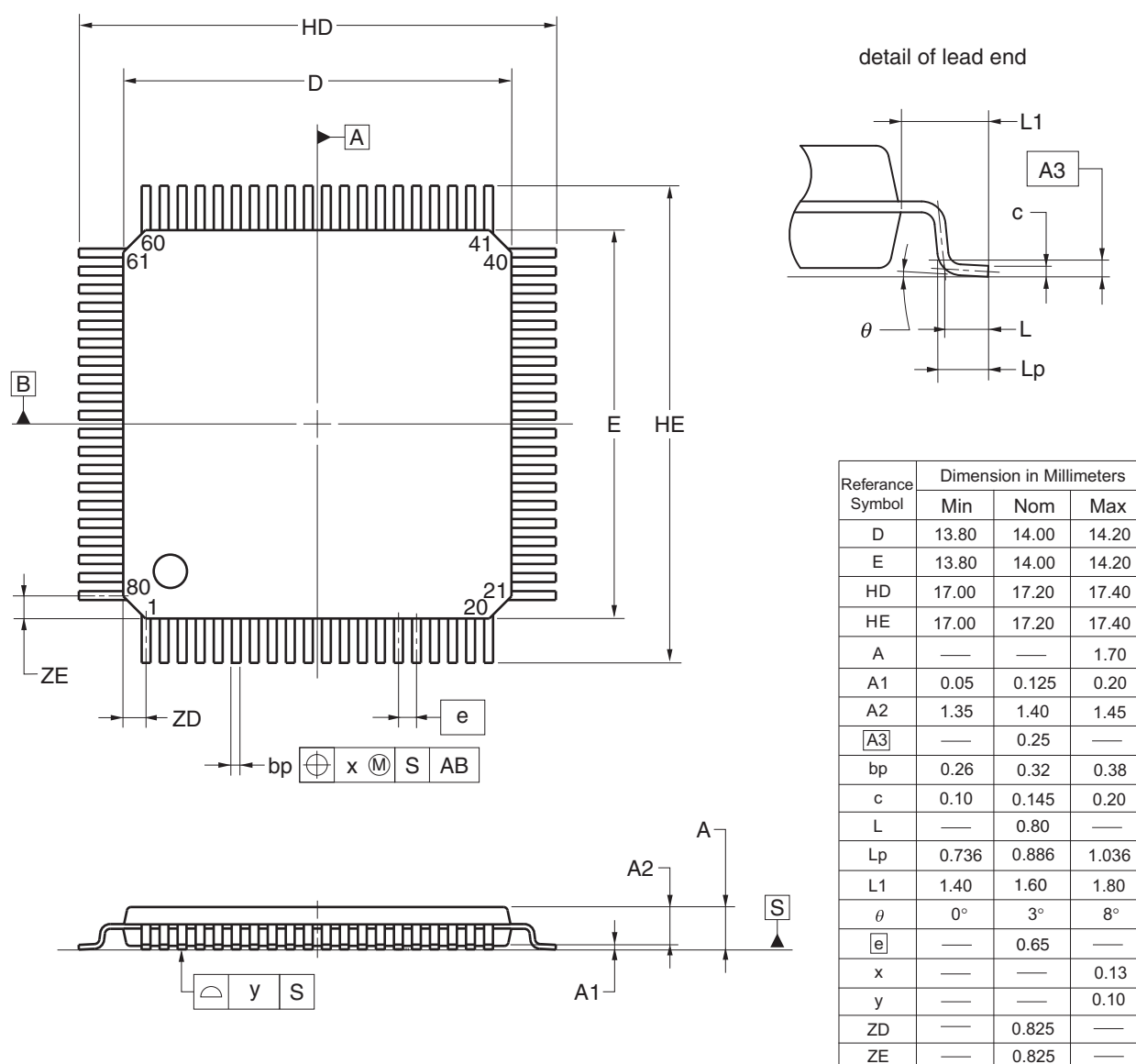
2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

## 4.12 80-pin Products

R5F100MFAFA, R5F100MGFAFA, R5F100MHAFA, R5F100MJFAFA, R5F100MKAFA, R5F100MLAFA  
 R5F101MFAFA, R5F101MGFAFA, R5F101MHAFA, R5F101MJFAFA, R5F101MKAFA, R5F101MLAFA  
 R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA  
 R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA  
 R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (2/2)
		109	Addition of (1) I <sup>2</sup> C standard mode
		111	Addition of (2) I <sup>2</sup> C fast mode
		112	Addition of (3) I <sup>2</sup> C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)

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