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**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

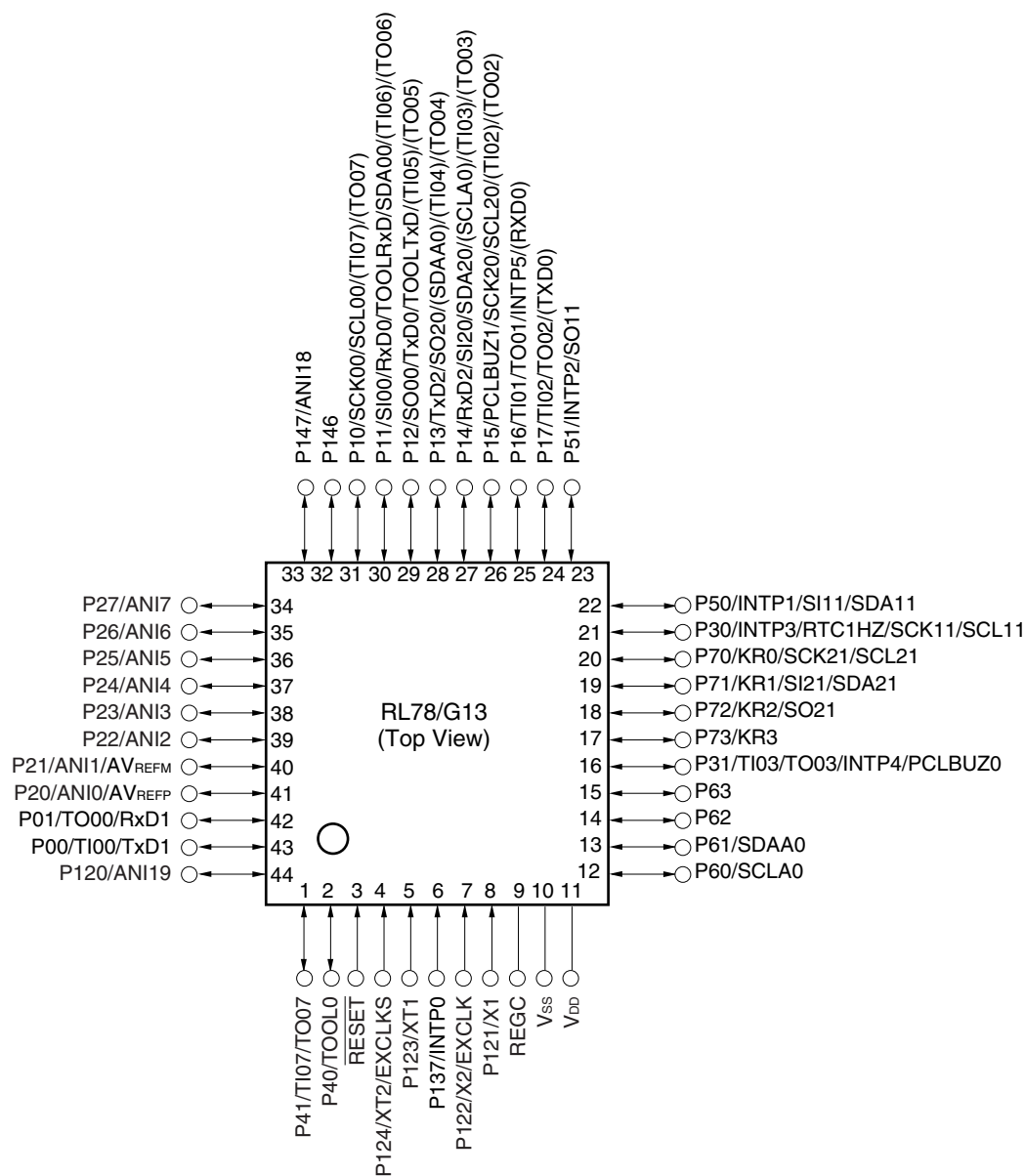| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101ldafb-v0 |

**Table 1-1.  List of Ordering Part Numbers**

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 25 pins | 25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch) | Mounted | A | R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0<br>R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0 |
| | | | G | R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0<br>R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0 |
| | | Not mounted | A | R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0<br>R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0 |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch) | Mounted | A | R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0<br>R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0 |
| | | | D | R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDSP#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0<br>R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDSP#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0 |
| | | | G | R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0,R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0<br>R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0,R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0 |
| | | Not mounted | A | R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0<br>R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0 |
| | | | D | R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDSP#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0<br>R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDSP#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0 |
| 32 pins | 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch) | Mounted | A | R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0<br>R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0 |
| | | | D | R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0<br>R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0 |
| | | | G | R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0<br>R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0 |
| | | Not mounted | A | R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0<br>R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0 |
| | | | D | R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0<br>R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0 |

**Note**    For the fields of application, refer to **Figure 1-1  Part Number, Memory Size, and Package of RL78/G13**.

**Caution  The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

### 1.3.8  44-pin products
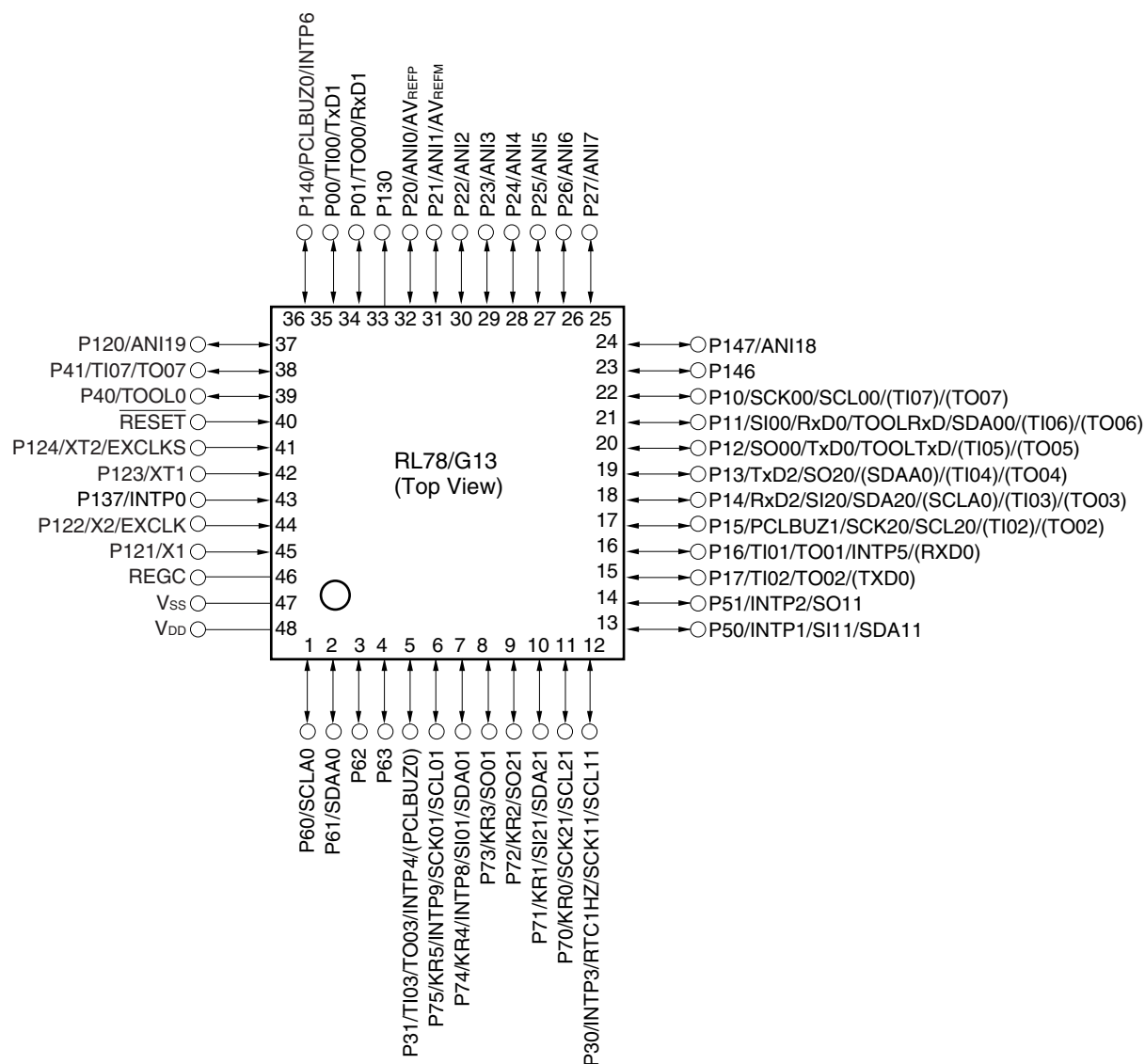
- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



**Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.**  For pin identification, see **1.4  Pin Identification**.
   **2.**  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.3.9  48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

Pins (top): P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7 (pins 36 35 34 33 32 31 30 29 28 27 26 25)

Left side:
- P120/ANI19 — 37
- P41/TI07/TO07 — 38
- P40/TOOL0 — 39
- $\overline{\text{RESET}}$ — 40
- P124/XT2/EXCLKS — 41
- P123/XT1 — 42
- P137/INTP0 — 43
- P122/X2/EXCLK — 44
- P121/X1 — 45
- REGC — 46
- V$_{SS}$ — 47
- V$_{DD}$ — 48

RL78/G13
(Top View)

Right side:
- 24 — P147/ANI18
- 23 — P146
- 22 — P10/SCK00/SCL00/(TI07)/(TO07)
- 21 — P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 — P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 — P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 — P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 — P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 — P16/TI01/TO01/INTP5/(RXD0)
- 15 — P17/TI02/TO02/(TXD0)
- 14 — P51/INTP2/SO11
- 13 — P50/INTP1/SI11/SDA11

Pins (bottom, 1–12): P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

**Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).**

**Remarks 1.** For pin identification, see **1.4  Pin Identification**.
**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

**Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | |
|------|---|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| | | R5F1006x | R5F1016x | R5F1007x | R5F1017x | R5F1008x | R5F1018x | R5F100Ax | R5F101Ax | R5F100Bx | R5F101Bx | R5F100Cx | R5F101Cx |
| Code flash memory (KB) | | 16 to 64 | | 16 to 64 | | 16 to 64 | | 16 to 128 | | 16 to 128 | | 16 to 128 | |
| Data flash memory (KB) | | 4 | – | 4 | – | 4 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 4[Note1] | | 2 to 4[Note1] | | 2 to 4[Note1] | | 2 to 12[Note1] | | 2 to 12[Note1] | | 2 to 12[Note1] | |
| Address space | | 1 MB | | | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| Subsystem clock | | – | | | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 $\mu$s (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | | | | | | | |
| | | 0.05 $\mu$s (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | | | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | | | |
| I/O port | Total | 16 | | 20 | | 21 | | 26 | | 28 | | 32 | |
| | CMOS I/O | 13<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 5) | | 15<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 6) | | 15<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 6) | | 21<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 9) | | 22<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 9) | | 26<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 10) | |
| | CMOS input | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | |
| | CMOS output | – | | – | | 1 | | – | | – | | – | |
| | N-ch O.D. I/O<br>(withstand voltage: 6 V) | – | | 2 | | 2 | | 2 | | 3 | | 3 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel [Note 2] | | | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | | | |
| | Timer output | 3 channels<br>(PWM outputs:<br>2 [Note 3]) | | 4 channels<br>(PWM outputs: 3 [Note 3]) | | | | 4 channels (PWM outputs: 3 [Note 3]),<br>8 channels (PWM outputs: 7 [Note 3]) [Note 4] | | | | | |
| | RTC output | – | | | | | | | | | | | |

**Notes  1.**   The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
    R5F100xD, R5F101xD (x = 6 to 8, A to C):   Start address FF300H
    R5F100xE, R5F101xE (x = 6 to 8, A to C):   Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

    **2.**   Only the constant-period interrupt function when the low-speed on-chip oscillator clock ($f_{IL}$) is selected

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency (f$_X$)[Note] | Ceramic resonator/ crystal resonator | 2.7 V ≤ V$_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ V$_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ V$_{DD}$ < 2.4 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ V$_{DD}$ < 1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency (f$_X$)[Note] | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

### 2.2.2 On-chip oscillator characteristics

**(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency[Notes 1, 2] | f$_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | −20 to +85 °C | 1.8 V ≤ V$_{DD}$ ≤ 5.5 V | −1.0 | | +1.0 | % |
| | | | 1.6 V ≤ V$_{DD}$ < 1.8 V | −5.0 | | +5.0 | % |
| | | −40 to −20 °C | 1.8 V ≤ V$_{DD}$ ≤ 5.5 V | −1.5 | | +1.5 | % |
| | | | 1.6 V ≤ V$_{DD}$ < 1.8 V | −5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | f$_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | −15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.
  **2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | | | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | $I_{DD2}$ [Note 2] | HALT mode | HS (high-speed main) mode [Note 7] | $f_{IH}$ = 32 MHz [Note 4] | $V_{DD}$ = 5.0 V | | 0.62 | 1.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 1.86 | mA |
| | | | | $f_{IH}$ = 24 MHz [Note 4] | $V_{DD}$ = 5.0 V | | 0.50 | 1.45 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 1.45 | mA |
| | | | | $f_{IH}$ = 16 MHz [Note 4] | $V_{DD}$ = 5.0 V | | 0.44 | 1.11 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.44 | 1.11 | mA |
| | | | LS (low-speed main) mode [Note 7] | $f_{IH}$ = 8 MHz [Note 4] | $V_{DD}$ = 3.0 V | | 290 | 620 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 290 | 620 | μA |
| | | | LV (low-voltage main) mode [Note 7] | $f_{IH}$ = 4 MHz [Note 4] | $V_{DD}$ = 3.0 V | | 440 | 680 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 440 | 680 | μA |
| | | | HS (high-speed main) mode [Note 7] | $f_{MX}$ = 20 MHz [Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | $f_{MX}$ = 20 MHz [Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | LS (low-speed main) mode [Note 7] | $f_{MX}$ = 8 MHz [Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 160 | 420 | μA |
| | | | | $f_{MX}$ = 8 MHz [Note 3], $V_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 160 | 420 | μA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz [Note 5], $T_A$ = −40°C | Square wave input | | 0.28 | 0.61 | μA |
| | | | | | Resonator connection | | 0.47 | 0.80 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 5], $T_A$ = +25°C | Square wave input | | 0.34 | 0.61 | μA |
| | | | | | Resonator connection | | 0.53 | 0.80 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 5], $T_A$ = +50°C | Square wave input | | 0.41 | 2.30 | μA |
| | | | | | Resonator connection | | 0.60 | 2.49 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 5], $T_A$ = +70°C | Square wave input | | 0.64 | 4.03 | μA |
| | | | | | Resonator connection | | 0.83 | 4.22 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 5], $T_A$ = +85°C | Square wave input | | 1.09 | 8.04 | μA |
| | | | | | Resonator connection | | 1.28 | 8.23 | μA |
| | $I_{DD3}$ [Note 6] | STOP mode [Note 8] | $T_A$ = −40°C | | | | 0.19 | 0.52 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.52 | μA |
| | | | $T_A$ = +50°C | | | | 0.32 | 2.21 | μA |
| | | | $T_A$ = +70°C | | | | 0.55 | 3.94 | μA |
| | | | $T_A$ = +85°C | | | | 1.00 | 7.95 | μA |

(**Notes** and **Remarks** are listed on the next page.)

6. Current flowing only to the A/D converter.  The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit.  The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**


**Remarks 1.** $f_{IL}$:    Low-speed on-chip oscillator clock frequency

       **2.** $f_{SUB}$:  Subsystem clock frequency (XT1 clock oscillation frequency)

       **3.** $f_{CLK}$:  CPU/peripheral hardware clock frequency

       **4.** Temperature condition of the TYP. value is $T_A$ = 25°C

**(4)　During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)**

**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) [Note 1] | t$_{SIK2}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1/f$_{MCK}$+20 | | 1/f$_{MCK}$+30 | | 1/f$_{MCK}$+30 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1/f$_{MCK}$+30 | | 1/f$_{MCK}$+30 | | 1/f$_{MCK}$+30 | | ns |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1/f$_{MCK}$+40 | | 1/f$_{MCK}$+40 | | 1/f$_{MCK}$+40 | | ns |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 1/f$_{MCK}$+40 | | 1/f$_{MCK}$+40 | | ns |
| SIp hold time (from SCKp↑) [Note 2] | t$_{KSI2}$ | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1/f$_{MCK}$+31 | | 1/f$_{MCK}$+31 | | 1/f$_{MCK}$+31 | | ns |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1/f$_{MCK}$+250 | | 1/f$_{MCK}$+250 | | 1/f$_{MCK}$+250 | | ns |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 1/f$_{MCK}$+250 | | 1/f$_{MCK}$+250 | | ns |
| Delay time from SCKp↓ to SOp output [Note 3] | t$_{KSO2}$ | C = 30 pF [Note 4] | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 2/f$_{MCK}$+44 | | 2/f$_{MCK}$+110 | | 2/f$_{MCK}$+110 | ns |
| | | | 2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 2/f$_{MCK}$+75 | | 2/f$_{MCK}$+110 | | 2/f$_{MCK}$+110 | ns |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 2/f$_{MCK}$+110 | | 2/f$_{MCK}$+110 | | 2/f$_{MCK}$+110 | ns |
| | | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 2/f$_{MCK}$+220 | | 2/f$_{MCK}$+220 | | 2/f$_{MCK}$+220 | ns |
| | | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 2/f$_{MCK}$+220 | | 2/f$_{MCK}$+220 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution　Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

**2.** f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) [Note 1] | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) [Note 1] | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output [Note 1] | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

Notes  1.  When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
       2.  Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution  Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the next page.)

## 2.5.2 Serial interface IICA

### (1) I²C standard mode

**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | f$_{SCL}$ | Standard mode: f$_{CLK}$ ≥ 1 MHz | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | t$_{SU:STA}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |
| Hold time[Note 1] | t$_{HD:STA}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Hold time when SCLA0 = "L" | t$_{LOW}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |
| Hold time when SCLA0 = "H" | t$_{HIGH}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Data setup time (reception) | t$_{SU:DAT}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 250 | | 250 | | ns |
| Data hold time (transmission)[Note 2] | t$_{HD:DAT}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 0 | 3.45 | 0 | 3.45 | μs |
| Setup time of stop condition | t$_{SU:STO}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Bus-free time | t$_{BUF}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |

(**Notes**, **Caution** and **Remark** are listed on the next page.)

**(2) I$^2$C fast mode**

**($T_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | $\mu$s |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | $\mu$s |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | $\mu$s |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | $\mu$s |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | $\mu$s |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | $\mu$s |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

&lt;R&gt;    **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

   Fast mode:  C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**(T$_A$ = –40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (–) = AV$_{REFM}$ = 0 V [Note 4], HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | t$_{CONV}$ | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | 17 | | 39 | $\mu$s |
| Zero-scale error[Notes 1, 2] | E$_{ZS}$ | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error[Note 1] | DLE | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | V$_{AIN}$ | | | 0 | | V$_{BGR}$ [Note 3] | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

    **2.** This value is indicated as a ratio (%FSR) to the full-scale value.

    **3.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

    **4.** When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.

        Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV$_{REFM}$.

        Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

        Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)**

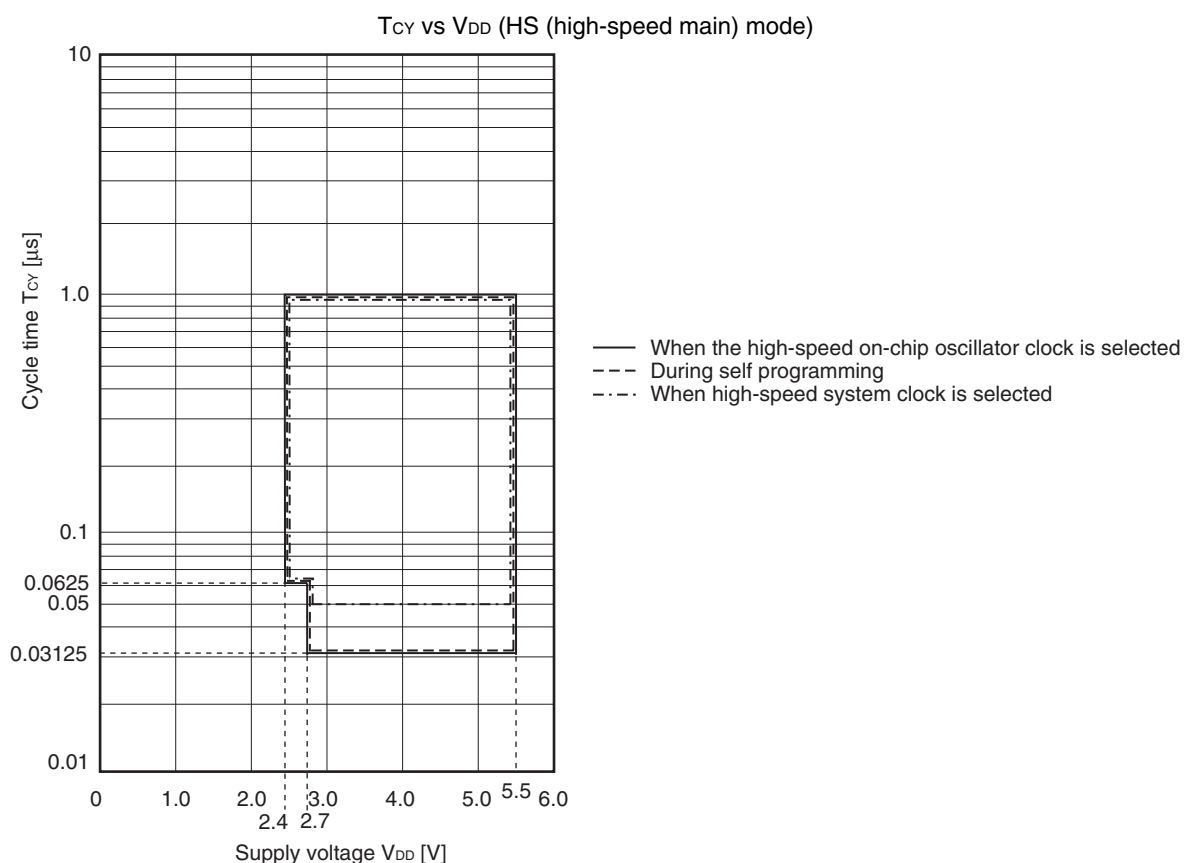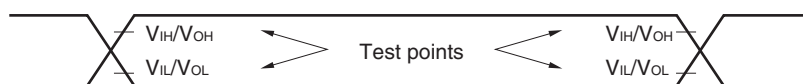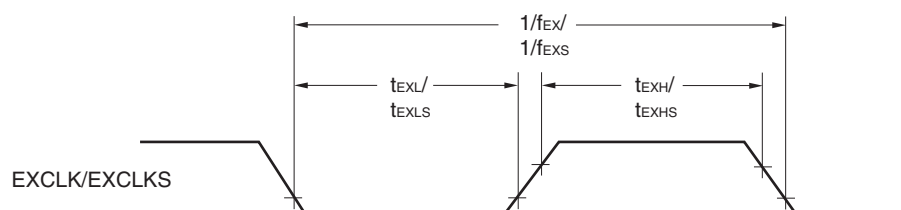| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | I$_{DD1}$ | Operating mode | HS (high-speed main) mode [Note 5] | f$_{IH}$ = 32 MHz [Note 3] | Basic operation | V$_{DD}$ = 5.0 V | | 2.3 | | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 2.3 | | mA |
| | | | | | Normal operation | V$_{DD}$ = 5.0 V | | 5.2 | 9.2 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 5.2 | 9.2 | mA |
| | | | | f$_{IH}$ = 24 MHz [Note 3] | Normal operation | V$_{DD}$ = 5.0 V | | 4.1 | 7.0 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 4.1 | 7.0 | mA |
| | | | | f$_{IH}$ = 16 MHz [Note 3] | Normal operation | V$_{DD}$ = 5.0 V | | 3.0 | 5.0 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 3.0 | 5.0 | mA |
| | | | HS (high-speed main) mode [Note 5] | f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 5.9 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.0 | mA |
| | | | | f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 5.9 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.0 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.5 | mA |
| | | | | | | Resonator connection | | 2.1 | 3.5 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.5 | mA |
| | | | | | | Resonator connection | | 2.1 | 3.5 | mA |
| | | | Subsystem clock operation | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = −40°C | Normal operation | Square wave input | | 4.8 | 5.9 | μA |
| | | | | | | Resonator connection | | 4.9 | 6.0 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 5.9 | μA |
| | | | | | | Resonator connection | | 5.0 | 6.0 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C | Normal operation | Square wave input | | 5.0 | 7.6 | μA |
| | | | | | | Resonator connection | | 5.1 | 7.7 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C | Normal operation | Square wave input | | 5.2 | 9.3 | μA |
| | | | | | | Resonator connection | | 5.3 | 9.4 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C | Normal operation | Square wave input | | 5.7 | 13.3 | μA |
| | | | | | | Resonator connection | | 5.8 | 13.4 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +105°C | Normal operation | Square wave input | | 10.0 | 46.0 | μA |
| | | | | | | Resonator connection | | 10.0 | 46.0 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$.  The values below the MAX. column include the peripheral operation current.  However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped.  When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).  The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** f$_{MX}$:    High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** f$_{IH}$:    High-speed on-chip oscillator clock frequency

**3.** f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

**Minimum Instruction Execution Time during Main System Clock Operation**

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)



—— When the high-speed on-chip oscillator clock is selected
- - - During self programming
- · - When high-speed system clock is selected

**AC Timing Test Points**



V$_{IH}$/V$_{OH}$     V$_{IH}$/V$_{OH}$
V$_{IL}$/V$_{OL}$     Test points     V$_{IL}$/V$_{OL}$

**External System Clock Timing**



1/f$_{EX}$/
1/f$_{EXS}$

t$_{EXL}$/     t$_{EXH}$/
t$_{EXLS}$     t$_{EXHS}$

EXCLK/EXCLKS

**(3)  During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**

**(T_A = –40 to +105°C, 2.4 V ≤ EV_DD0 = EV_DD1 ≤ V_DD ≤ 5.5 V, V_SS = EV_SS0 = EV_SS1 = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time [Note 5] | $t_{KCY2}$ | 4.0 V ≤ EV_DD0 ≤ 5.5 V | 20 MHz < $f_{MCK}$ | $16/f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | $12/f_{MCK}$ | | ns |
| | | 2.7 V ≤ EV_DD0 ≤ 5.5 V | 16 MHz < $f_{MCK}$ | $16/f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | $12/f_{MCK}$ | | ns |
| | | 2.4 V ≤ EV_DD0 ≤ 5.5 V | | $16/f_{MCK}$ | | ns |
| | | | | $12/f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ EV_DD0 ≤ 5.5 V | | $t_{KCY2}/2 - 14$ | | ns |
| | | 2.7 V ≤ EV_DD0 ≤ 5.5 V | | $t_{KCY2}/2 - 16$ | | ns |
| | | 2.4 V ≤ EV_DD0 ≤ 5.5 V | | $t_{KCY2}/2 - 36$ | | ns |
| SIp setup time (to SCKp↑) [Note 1] | $t_{SIK2}$ | 2.7 V ≤ EV_DD0 ≤ 5.5 V | | $1/f_{MCK}+40$ | | ns |
| | | 2.4 V ≤ EV_DD0 ≤ 5.5 V | | $1/f_{MCK}+60$ | | ns |
| SIp hold time (from SCKp↑) [Note 2] | $t_{KSI2}$ | 2.4 V ≤ EV_DD0 ≤ 5.5 V | | $1/f_{MCK}+62$ | | ns |
| Delay time from SCKp↓ to SOp output [Note 3] | $t_{KSO2}$ | C = 30 pF [Note 4] | 2.7 V ≤ EV_DD0 ≤ 5.5 V | | $2/f_{MCK}+66$ | ns |
| | | | 2.4 V ≤ EV_DD0 ≤ 5.5 V | | $2/f_{MCK}+113$ | ns |

**Notes  1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

 **2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

 **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

 **4.** C is the load capacitance of the SOp output lines.

 **5.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**Caution**  **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks  1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
    n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

 **2.** $f_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  m: Unit number,
    n: Channel number (mn = 00 to 03, 10 to 13))

**CSI mode connection diagram (during communication at same potential)**
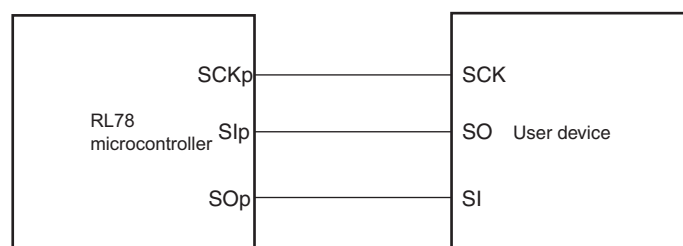
**(6)  Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

**($T_A$ = −40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) [Note] | $t_{SIK1}$ | 4.0 V $\leq$ EV$_{DD}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) [Note] | $t_{KSI1}$ | 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output [Note] | $t_{KSO1}$ | 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | | 50 | ns |

**Note**    When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution    Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**(7) Communication at different potential (1.8 V, 2.5 V, 3 V)  (CSI mode) (slave mode, SCKp... external clock input)**

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time [Note 1] | t$_{KCY2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | 24 MHz < f$_{MCK}$ | 28/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 24/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 20 MHz | 20/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 16/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 12/f$_{MCK}$ | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | 24 MHz < f$_{MCK}$ | 40/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 32/f$_{MCK}$ | | ns |
| | | | 16 MHz < f$_{MCK}$ ≤ 20 MHz | 28/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 16 MHz | 24/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 16/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 12/f$_{MCK}$ | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V | 24 MHz < f$_{MCK}$ | 96/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 72/f$_{MCK}$ | | ns |
| | | | 16 MHz < f$_{MCK}$ ≤ 20 MHz | 64/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 16 MHz | 52/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 32/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 20/f$_{MCK}$ | | ns |
| SCKp high-/low-level width | t$_{KH2}$, t$_{KL2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | | t$_{KCY2}$/2 − 24 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | | t$_{KCY2}$/2 − 36 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2] | | t$_{KCY2}$/2 − 100 | | ns |
| SIp setup time (to SCKp↑) [Note 2] | t$_{SIK2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | | 1/f$_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | | 1/f$_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V | | 1/f$_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) [Note 3] | t$_{KSI2}$ | | | 1/f$_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output [Note 4] | t$_{KSO2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | | | 2/f$_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | | | 2/f$_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | | | 2/f$_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

## 4.2  24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
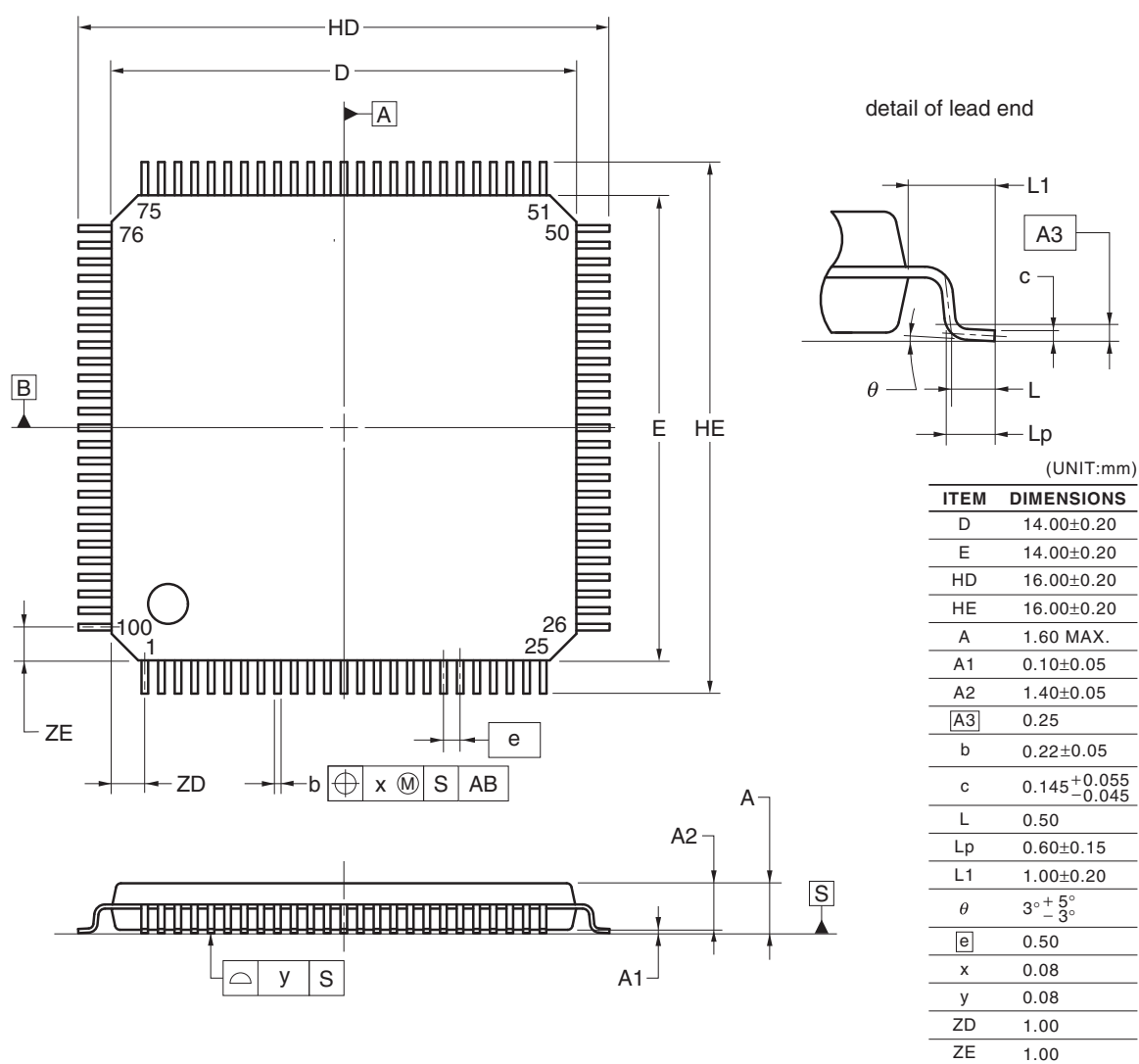R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

| JEITA Package  code | RENESAS  code | Previous  code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 3.95 | 4.00 | 4.05 |
| E | 3.95 | 4.00 | 4.05 |
| A | —— | —— | 0.80 |
| $A_1$ | 0.00 | —— | —— |
| b | 0.18 | 0.25 | 0.30 |
| $\boxed{e}$ | —— | 0.50 | —— |
| Lp | 0.30 | 0.40 | 0.50 |
| x | —— | —— | 0.05 |
| y | —— | —— | 0.05 |
| $Z_D$ | —— | 0.75 | —— |
| $Z_E$ | —— | 0.75 | —— |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | —— | 2.50 | —— |
| $E_2$ | —— | 2.50 | —— |
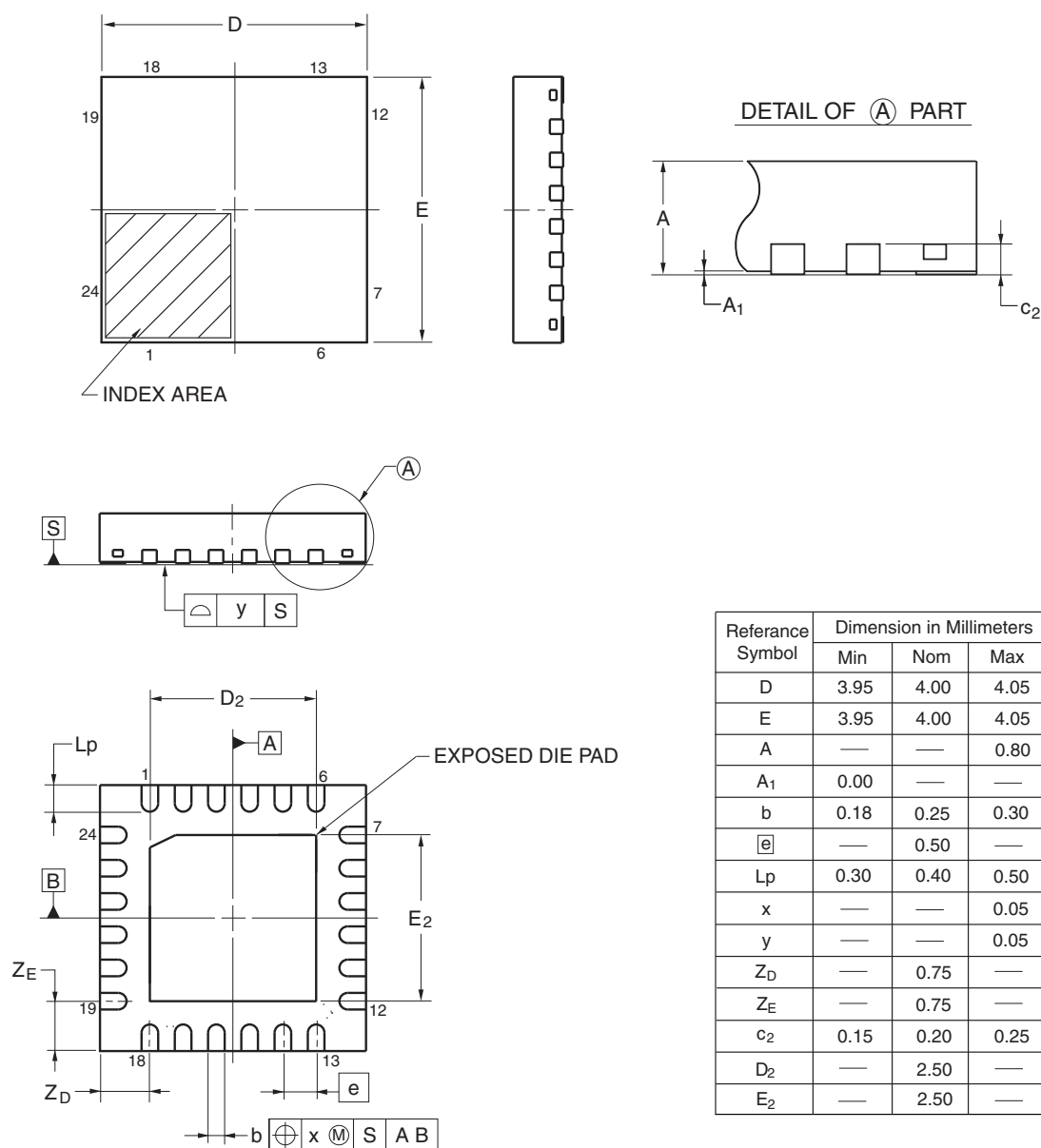
## 4.13  100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KE-A | P100GC-50-GBR-1 | 0.69 |

detail of lead end

(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.20 |
| E | 14.00±0.20 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| $\theta$ | $3°^{+5°}_{-3°}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.00 |
| ZE | 1.00 |