What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
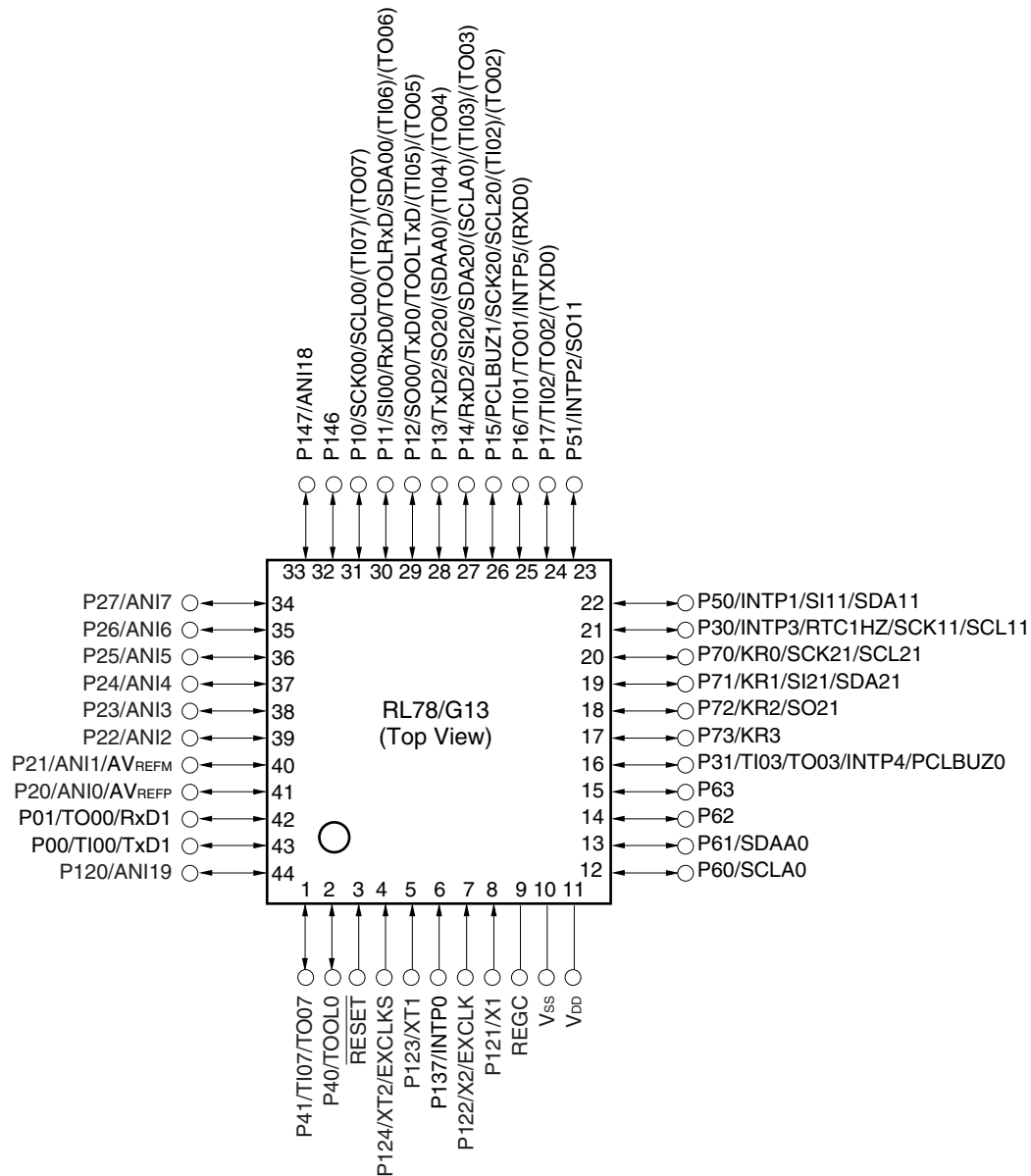
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lfafb-30

1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)

Top pins (23–33, left to right at positions 33 down to 23):
- P147/ANI18
- P146
- P10/SCK00/SCL00/(TI07)/(TO07)
- P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- P16/TI01/TO01/INTP5/(RXD0)
- P17/TI02/TO02/(TXD0)
- P51/INTP2/SO11

Left pins:
- P27/ANI7 — 34
- P26/ANI6 — 35
- P25/ANI5 — 36
- P24/ANI4 — 37
- P23/ANI3 — 38
- P22/ANI2 — 39
- P21/ANI1/AV$_{REFM}$ — 40
- P20/ANI0/AV$_{REFP}$ — 41
- P01/TO00/RxD1 — 42
- P00/TI00/TxD1 — 43
- P120/ANI19 — 44

RL78/G13 (Top View)

Right pins:
- 22 — P50/INTP1/SI11/SDA11
- 21 — P30/INTP3/RTC1HZ/SCK11/SCL11
- 20 — P70/KR0/SCK21/SCL21
- 19 — P71/KR1/SI21/SDA21
- 18 — P72/KR2/SO21
- 17 — P73/KR3
- 16 — P31/TI03/TO03/INTP4/PCLBUZ0
- 15 — P63
- 14 — P62
- 13 — P61/SDAA0
- 12 — P60/SCLA0

Bottom pins (1–11, left to right):
- P41/TI07/TO07
- P40/TOOL0
- RESET
- P124/XT2/EXCLKS
- P123/XT1
- P137/INTP0
- P122/X2/EXCLK
- P121/X1
- REGC
- V$_{SS}$
- V$_{DD}$

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.9 48-pin products
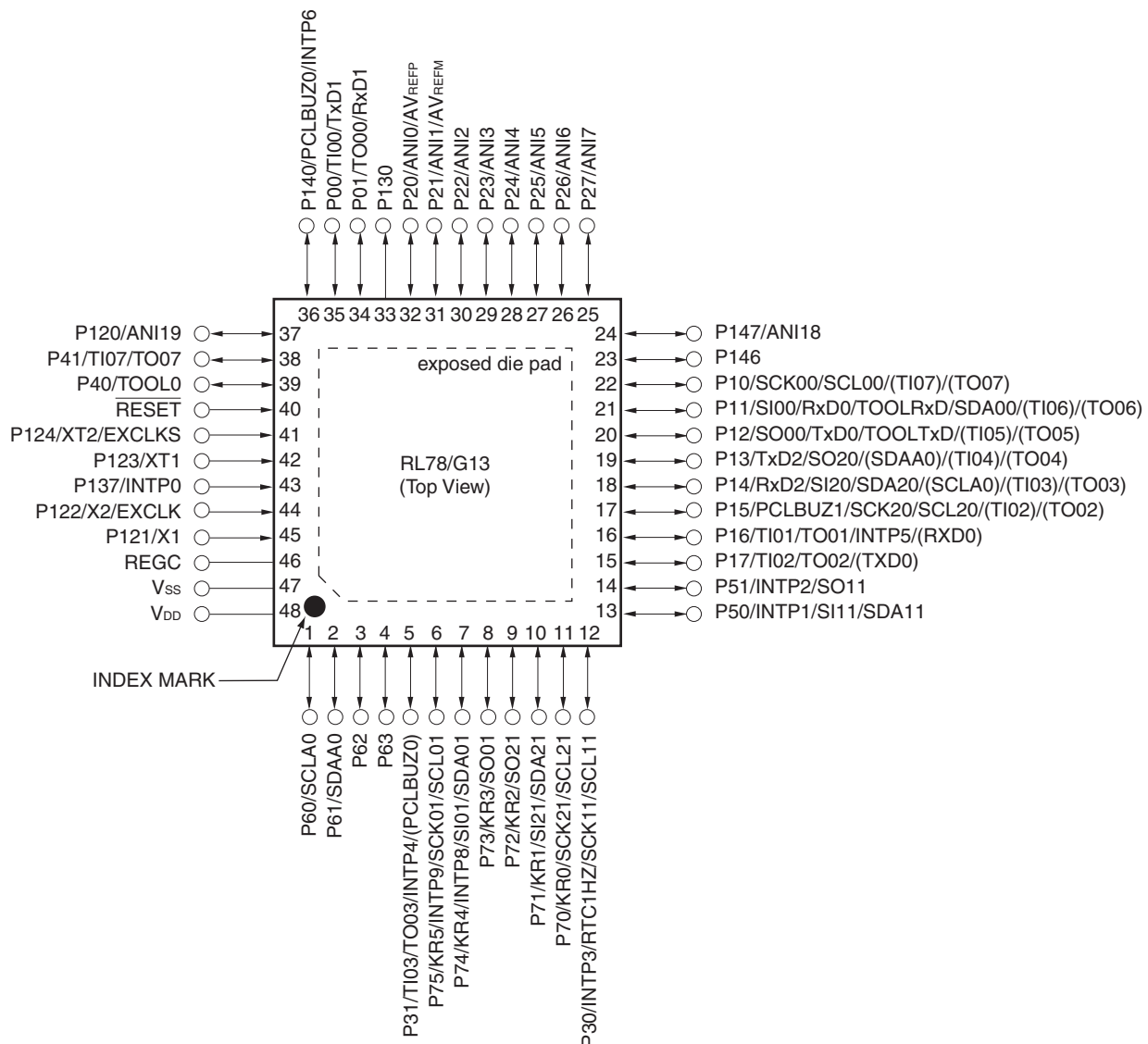
- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)
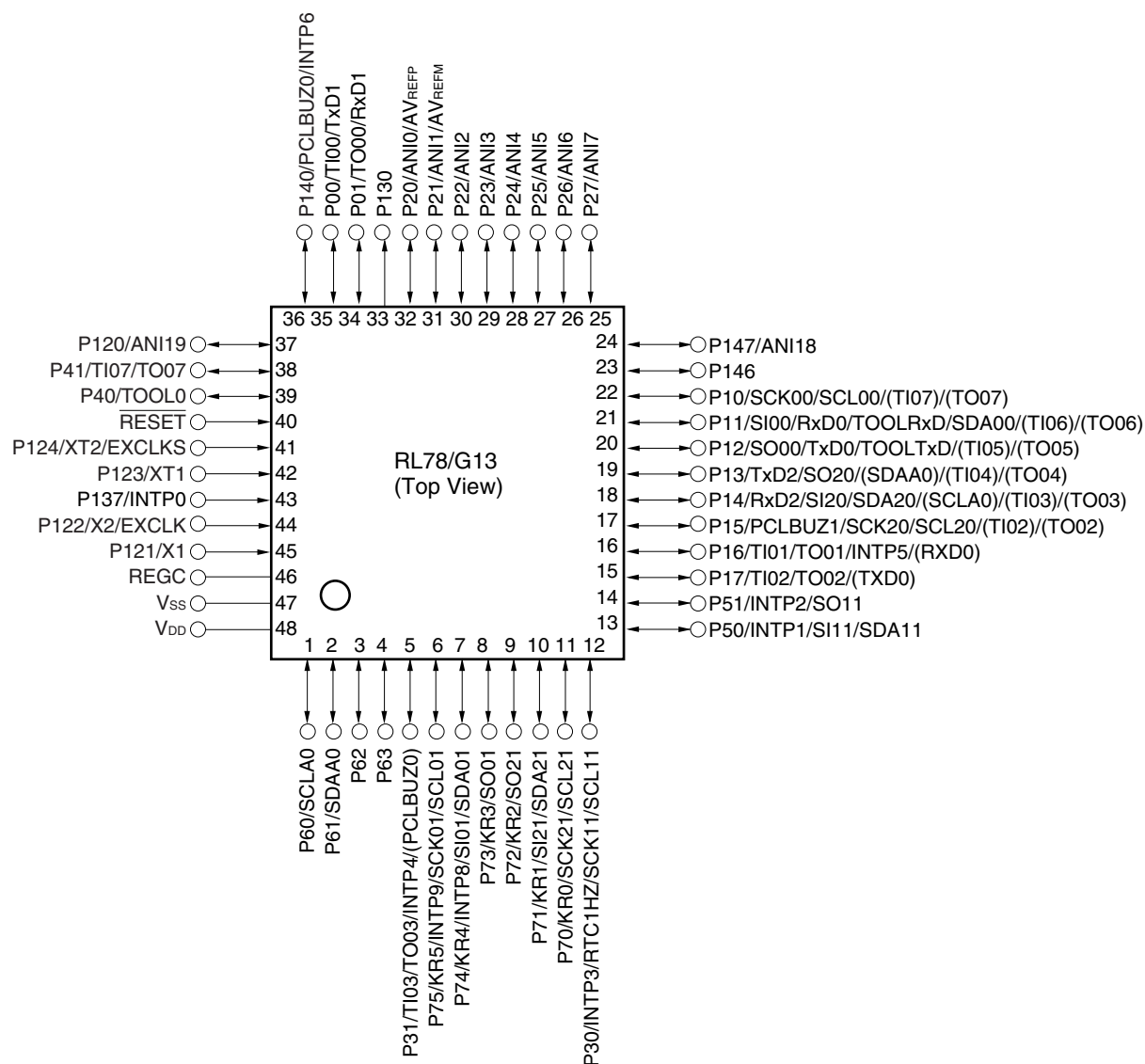
Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Pins (top, left to right): P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Top pin numbers: 36 35 34 33 32 31 30 29 28 27 26 25

Left side:
- P120/ANI19 — 37
- P41/TI07/TO07 — 38
- P40/TOOL0 — 39
- $\overline{\text{RESET}}$ — 40
- P124/XT2/EXCLKS — 41
- P123/XT1 — 42
- P137/INTP0 — 43
- P122/X2/EXCLK — 44
- P121/X1 — 45
- REGC — 46
- V$_{SS}$ — 47
- V$_{DD}$ — 48

exposed die pad

RL78/G13
(Top View)

Right side:
- 24 — P147/ANI18
- 23 — P146
- 22 — P10/SCK00/SCL00/(TI07)/(TO07)
- 21 — P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 — P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 — P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 — P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 — P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 — P16/TI01/TO01/INTP5/(RXD0)
- 15 — P17/TI02/TO02/(TXD0)
- 14 — P51/INTP2/SO11
- 13 — P50/INTP1/SI11/SDA11

Bottom pin numbers: 1 2 3 4 5 6 7 8 9 10 11 12

INDEX MARK

Bottom pins (left to right): P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to Vss.

1.3.13 100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)
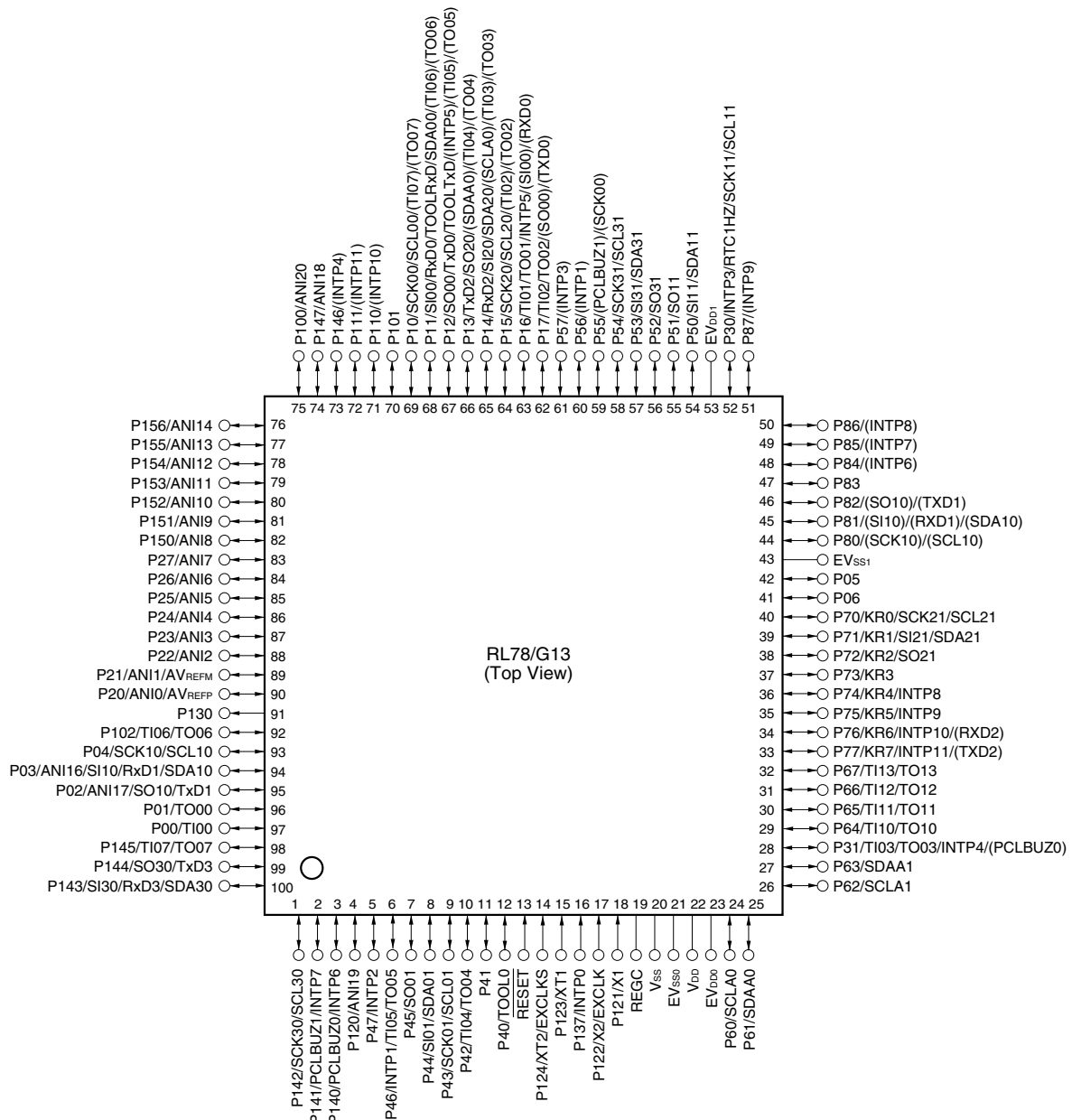
Cautions 1. Make EV$_{SS0}$, EV$_{SS1}$ pins the same potential as V$_{SS}$ pin.

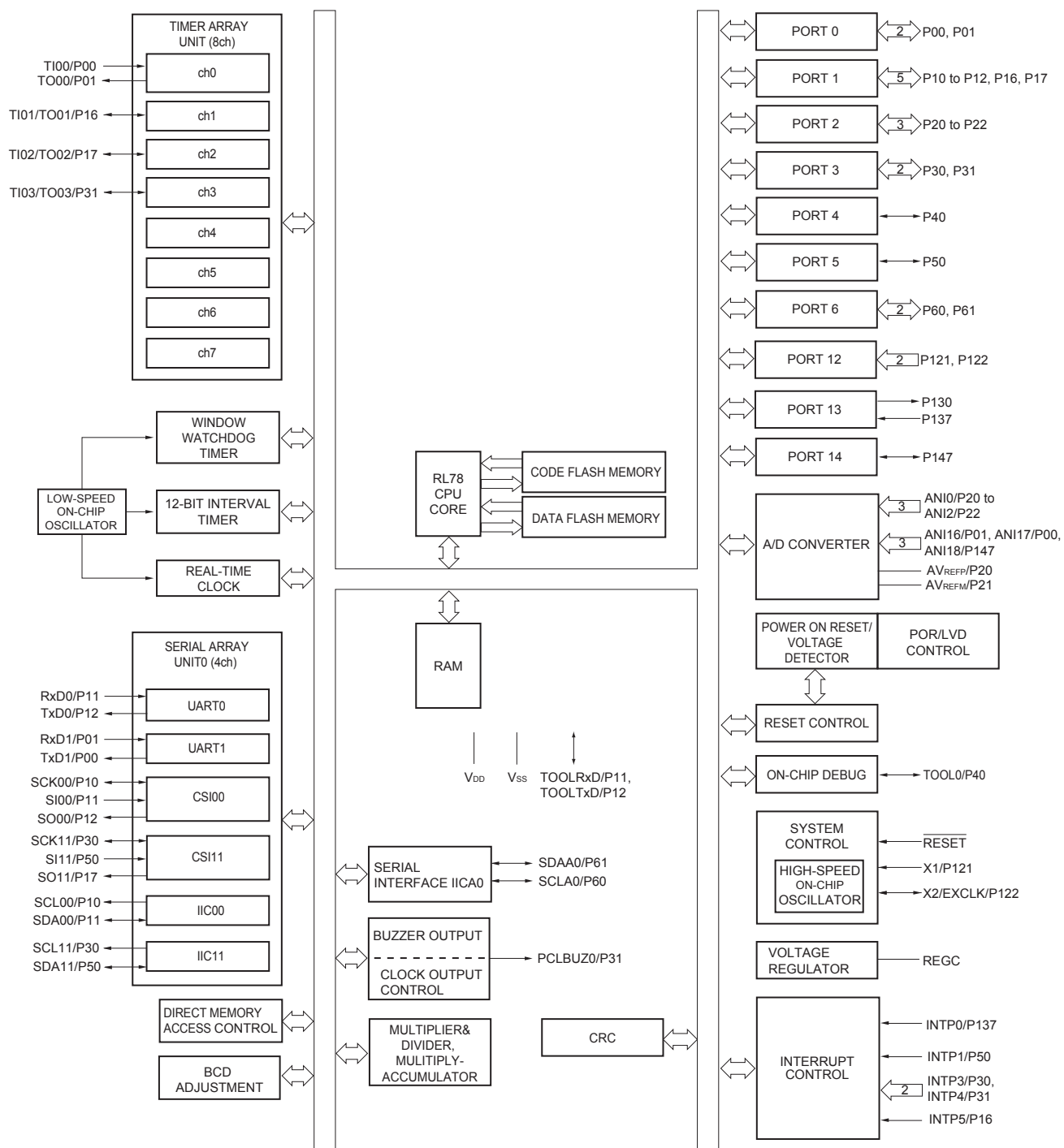**2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$, EV$_{DD1}$ pins (EV$_{DD0}$ = EV$_{DD1}$).**

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

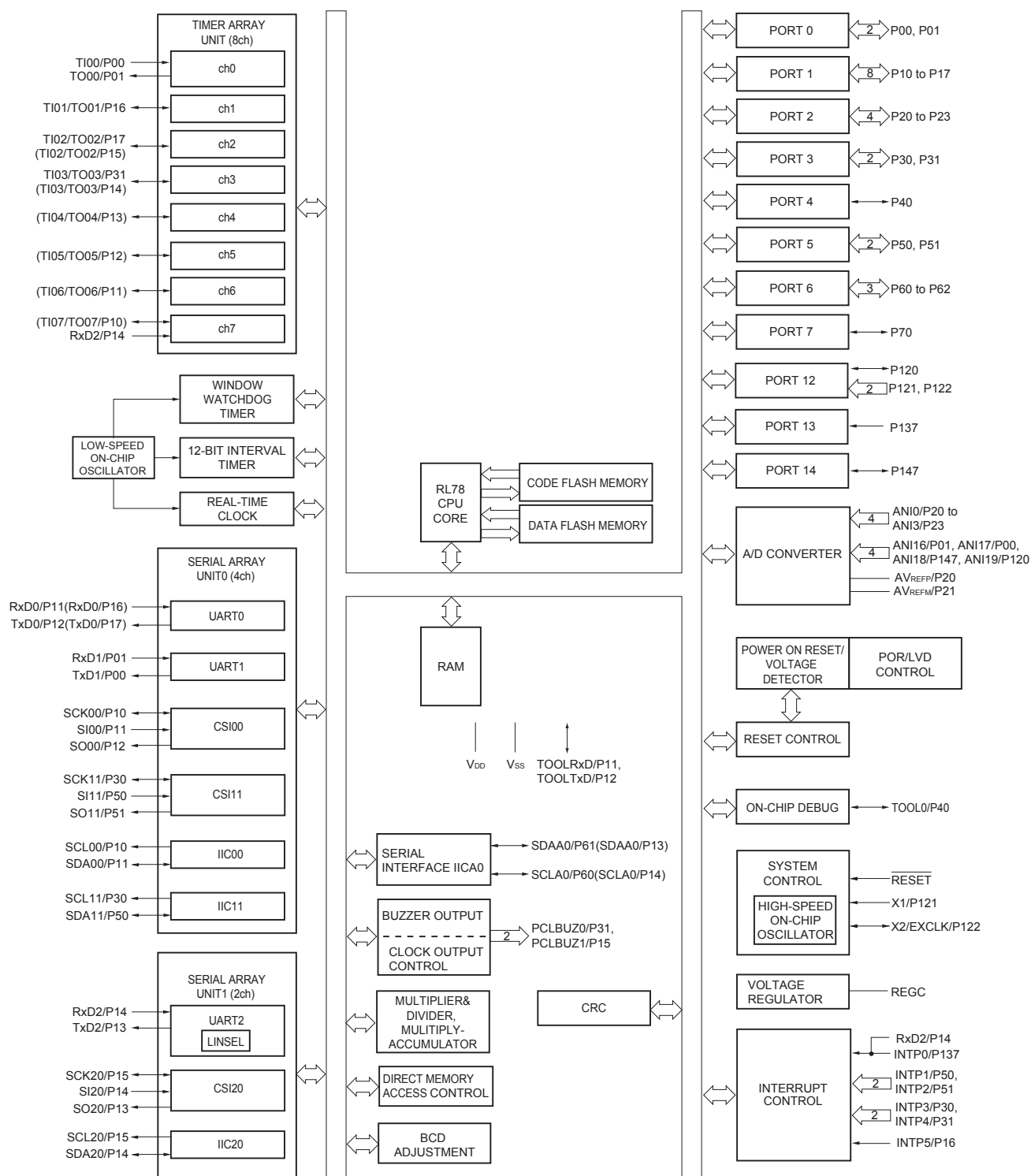**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$, EV$_{DD0}$ and EV$_{DD1}$ pins and connect the V$_{SS}$, EV$_{SS0}$ and EV$_{SS1}$ pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
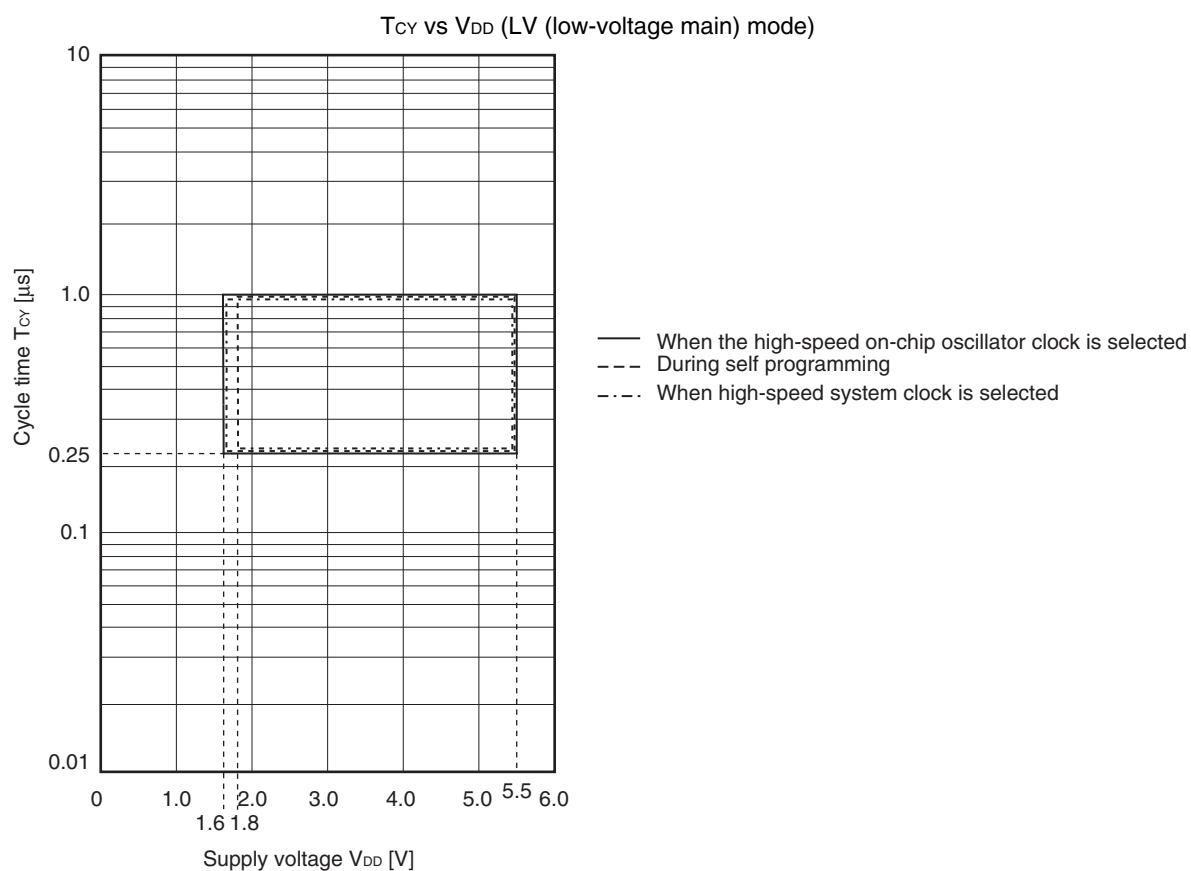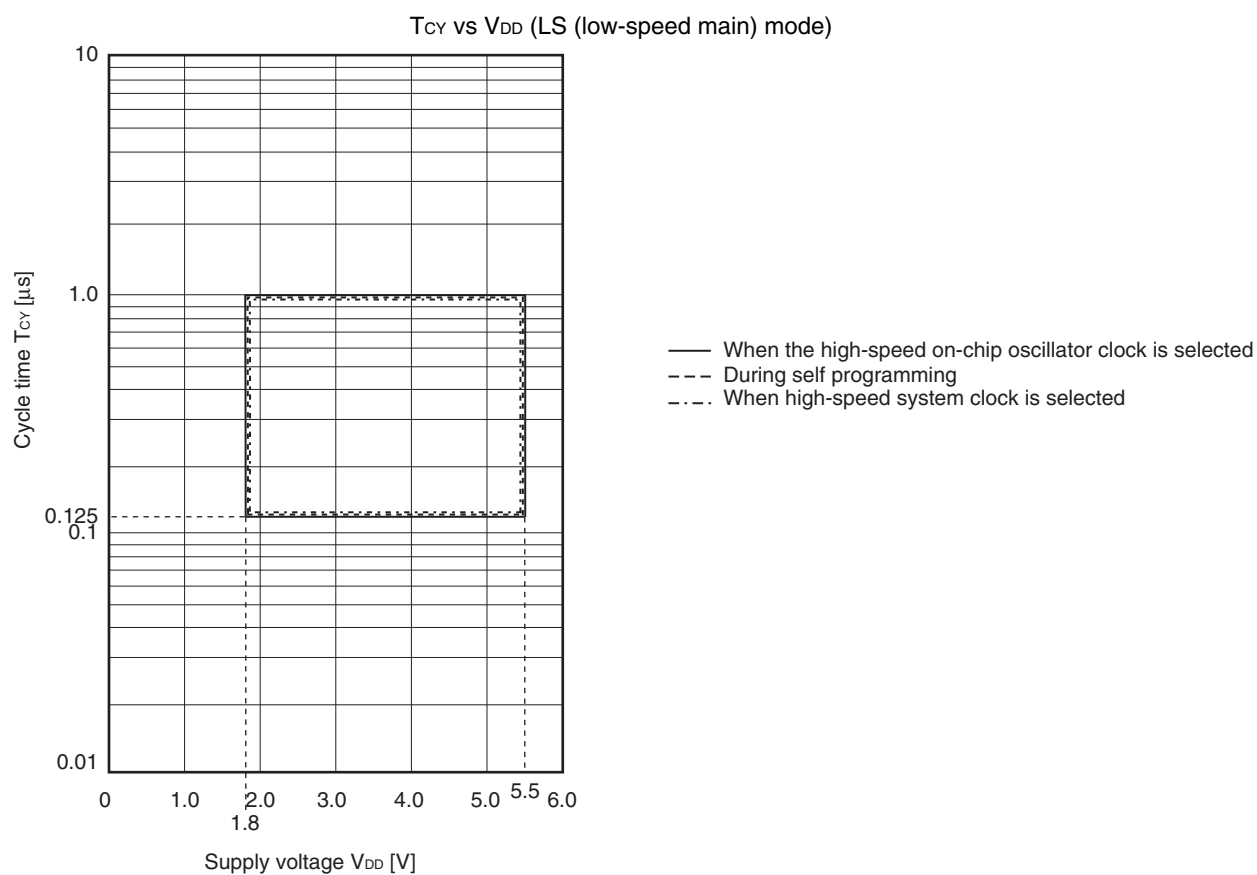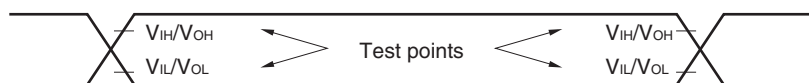
1.5.3 25-pin products

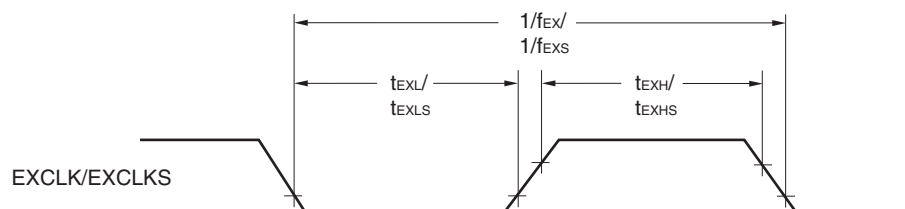Block diagram showing the functional blocks of the RL78/G13 25-pin product.

Left side blocks:

TIMER ARRAY UNIT (8ch)
- ch0 ← TI00/P00, TO00/P01
- ch1 ← TI01/TO01/P16
- ch2 ← TI02/TO02/P17
- ch3 ← TI03/TO03/P31
- ch4
- ch5
- ch6
- ch7

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR → 12-BIT INTERVAL TIMER

REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)
- UART0 ← RxD0/P11, TxD0/P12
- UART1 ← RxD1/P01, TxD1/P00
- CSI00 ← SCK00/P10, SI00/P11, SO00/P12
- CSI11 ← SCK11/P30, SI11/P50, SO11/P17
- IIC00 ← SCL00/P10, SDA00/P11
- IIC11 ← SCL11/P30, SDA11/P50

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

Center blocks:

RL78 CPU CORE
- CODE FLASH MEMORY
- DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 → SDAA0/P61, SCLA0/P60

BUZZER OUTPUT / CLOCK OUTPUT CONTROL → PCLBUZ0/P31

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

Right side blocks:

PORT 0 → 2 P00, P01
PORT 1 → 5 P10 to P12, P16, P17
PORT 2 → 3 P20 to P22
PORT 3 → 2 P30, P31
PORT 4 → P40
PORT 5 → P50
PORT 6 → 2 P60, P61
PORT 12 → 2 P121, P122
PORT 13 → P130, P137
PORT 14 → P147

A/D CONVERTER
- 3 ANI0/P20 to ANI2/P22
- 3 ANI16/P01, ANI17/P00, ANI18/P147
- AV_{REFP}/P20
- AV_{REFM}/P21

POWER ON RESET/ VOLTAGE DETECTOR / POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG → TOOL0/P40

SYSTEM CONTROL
HIGH-SPEED ON-CHIP OSCILLATOR
- RESET
- X1/P121
- X2/EXCLK/P122

VOLTAGE REGULATOR → REGC

INTERRUPT CONTROL
- INTP0/P137
- INTP1/P50
- 2 INTP3/P30, INTP4/P31
- INTP5/P16

1.5.5 32-pin products

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

                                   2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

   LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 8 MHz

   LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

T_{CY} vs V_{DD} (LS (low-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-.-. When high-speed system clock is selected

T_{CY} vs V_{DD} (LV (low-voltage main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-.-. When high-speed system clock is selected

AC Timing Test Points

External System Clock Timing

TI/TO Timing
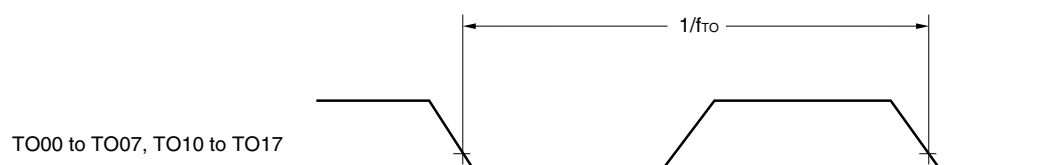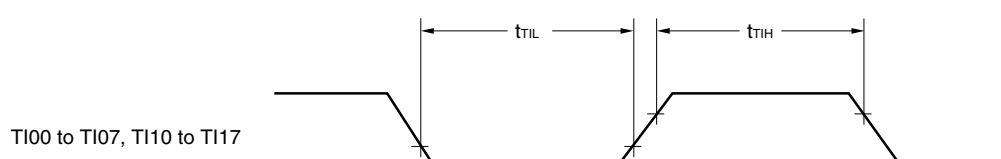
Interrupt Request Input Timing

Key Interrupt Input Timing
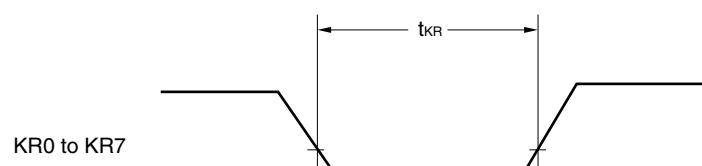
RESET Input Timing
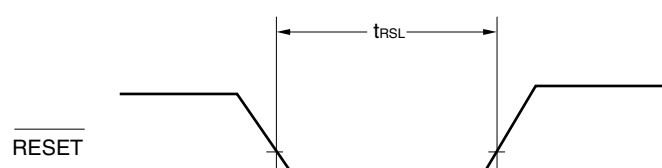
2.5 Peripheral Functions Characteristics

AC Timing Test Points
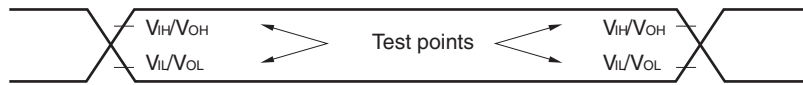
2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note 1]		2.4 V ≤ EV_{DD0} ≤ 5.5 V			$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		5.3		1.3		0.6	Mbps
		1.8 V ≤ EV_{DD0} ≤ 5.5 V			$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		5.3		1.3		0.6	Mbps
		1.7 V ≤ EV_{DD0} ≤ 5.5 V			$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]		5.3		1.3		0.6	Mbps
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—			$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} [Note 3]	—			1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ EV_{DD0} < 1.8 V : MAX. 0.6 Mbps

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
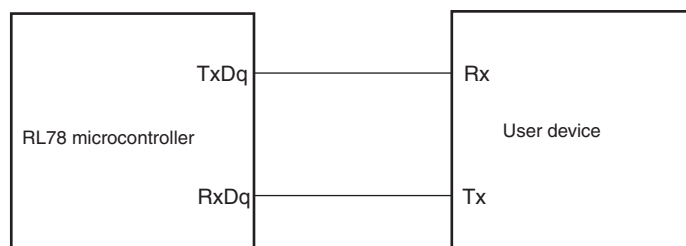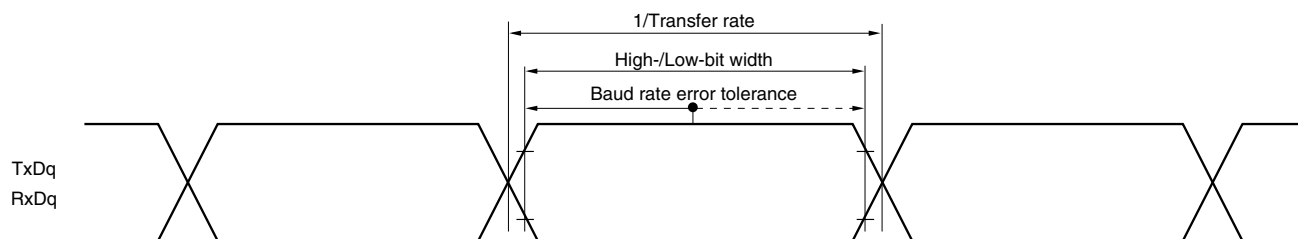
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

                                        16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution   **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

UART mode connection diagram (during communication at same potential)

RL78 microcontroller		User device
TxDq	——	Rx
RxDq	——	Tx

UART mode bit width (during communication at same potential) (reference)

1/Transfer rate

High-/Low-bit width

Baud rate error tolerance

TxDq
RxDq

Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

    2. f$_{MCK}$: Serial array unit operation clock frequency

      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

      n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = −40 to +85°C, 2.7 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI1}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO1}$	C = 20 pF [Note 4]			10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

      2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

      3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

      4. C is the load capacitance of the SCKp and SOp output lines.

Caution   **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1.   This value is valid only when CSI00's peripheral I/O redirect function is not used.

      2.   p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
         g: PIM and POM numbers (g = 1)

      3.   f$_{MCK}$: Serial array unit operation clock frequency

         (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

         n: Channel number (mn = 00))

3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

    * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with EV$_{DD0}$ $\geq$ V$_b$.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ EV$_{DD0}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

    * This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)
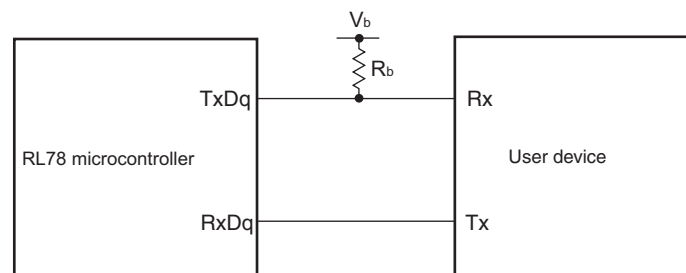
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		1/f$_{MCK}$ + 190 **Note 3**		kHz
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Use it with EV$_{DD0}$ ≥ V$_b$.

3. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

2.6.5 Power supply voltage rising slope characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

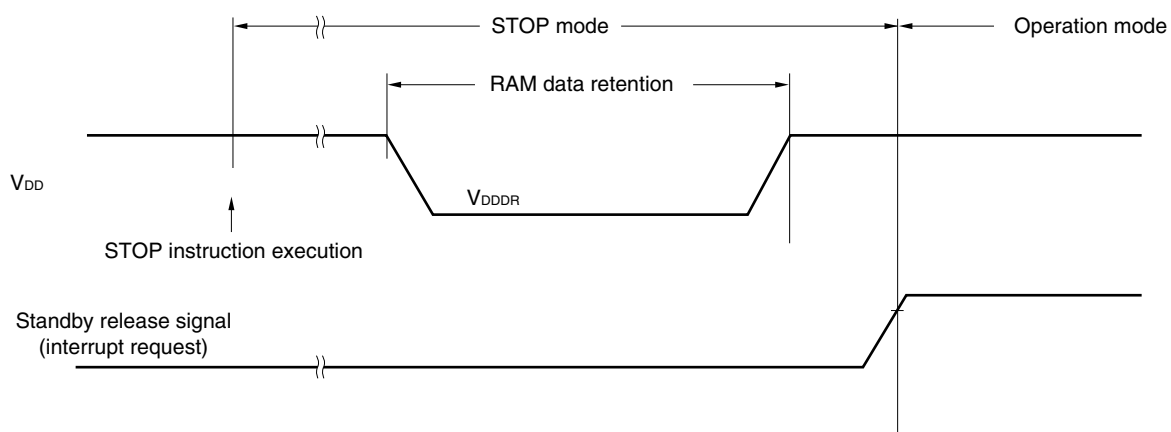| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution **Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

2.7 RAM Data Retention Characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

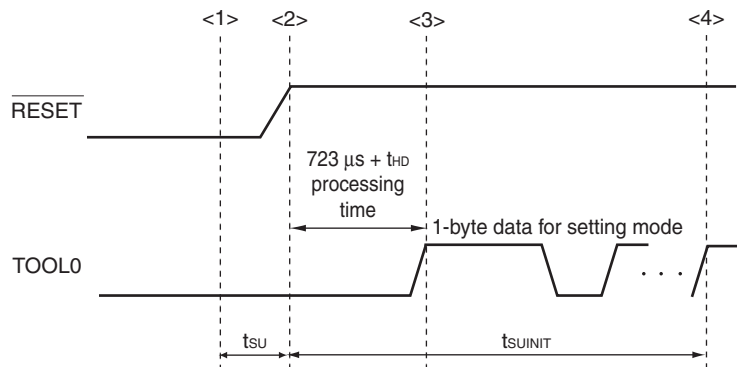| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

2.10 Timing of Entry to Flash Memory Programming Mode**s**

(T$_A$ = −40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms

<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t$_{SU}$:　　Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:　　Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)
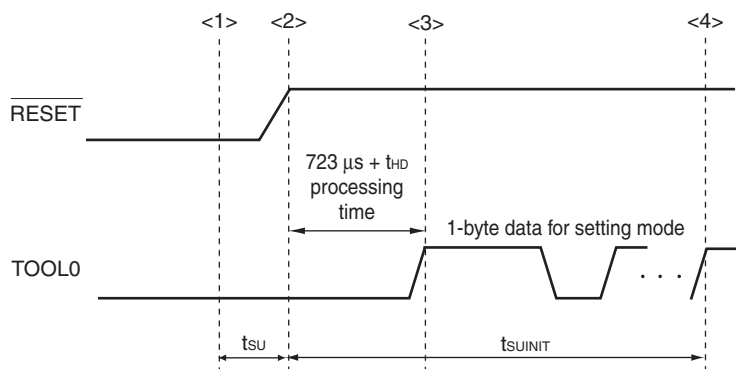
UART mode bit width (during communication at different potential) (reference)
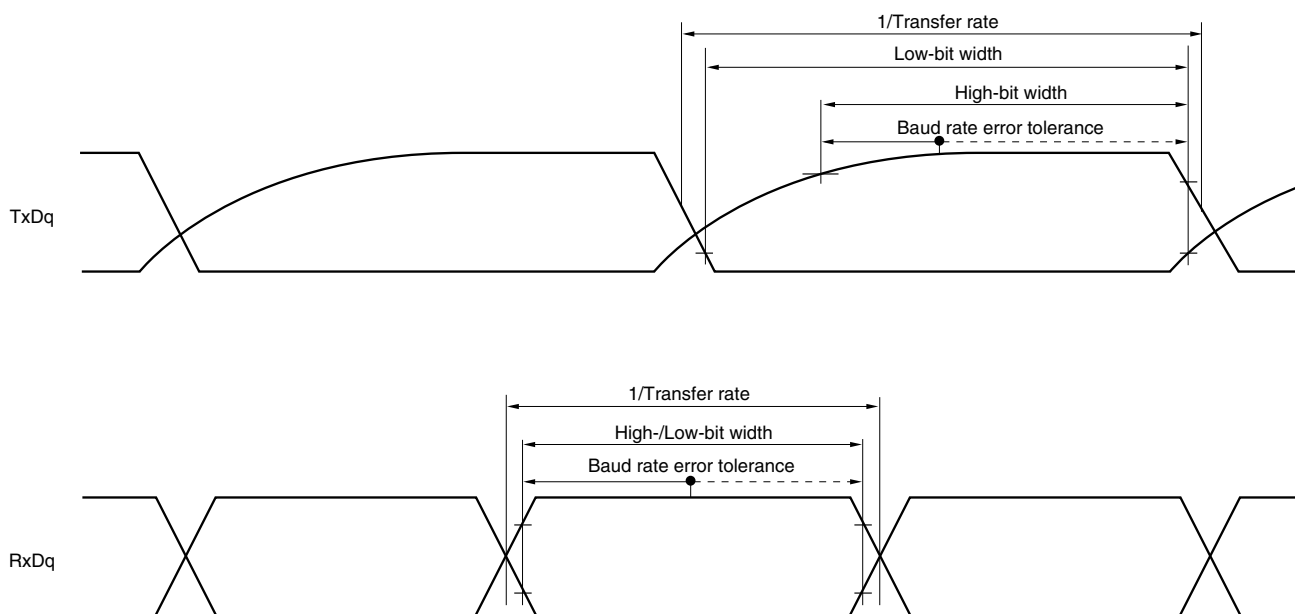
Remarks 1. R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection

register (PIOR) is 1.

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105°C$, 2.4 V $\leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms

<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
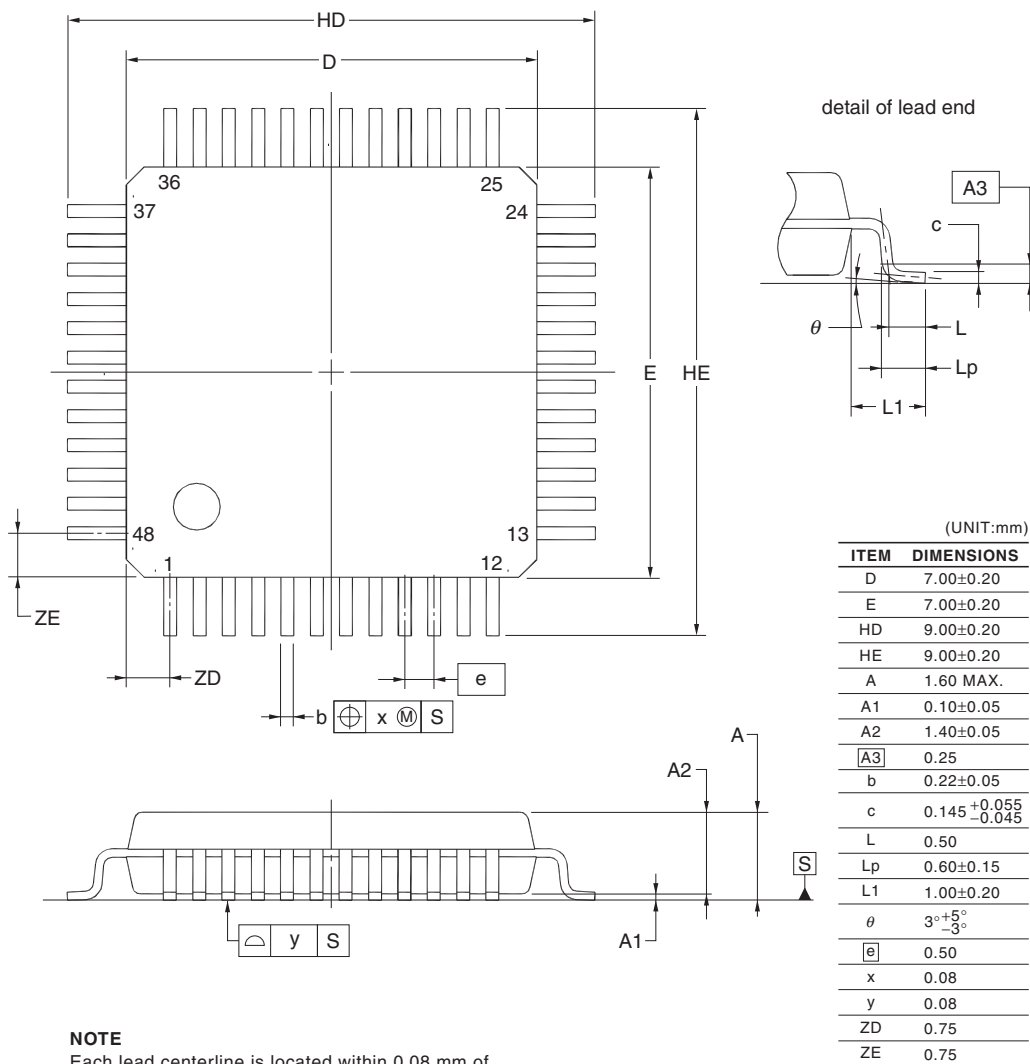
t_{SU}:   Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}:   Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)
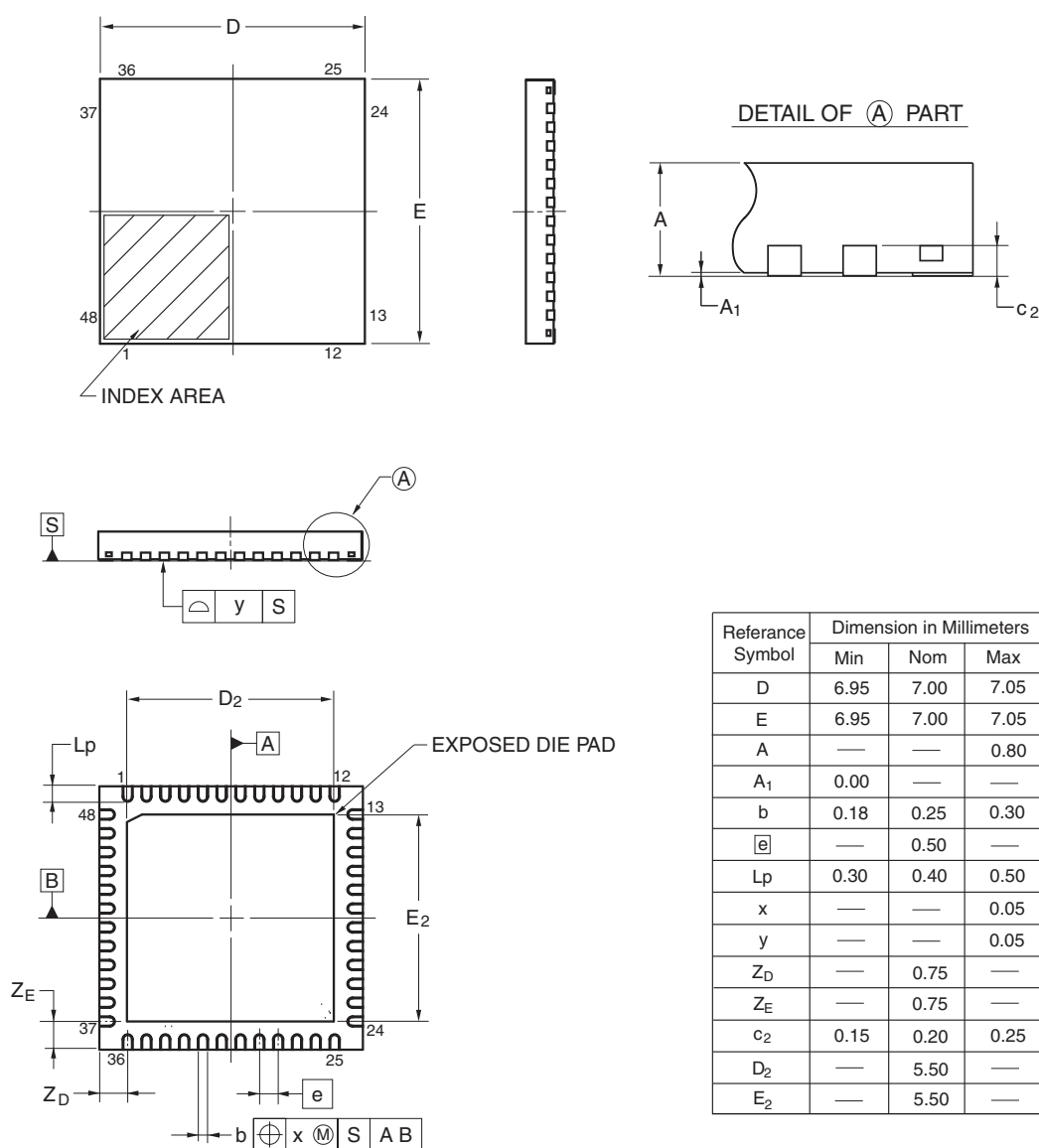
4.9 48-pin Products

R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB,
R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB
R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB,
R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB
R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB,
R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB,
R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB
R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB,
R5F100GHGFB, R5F100GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 {}^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° {}^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA, R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA

R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA, R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA

R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA, R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA

R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA, R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA

R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA, R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c₂	0.15	0.20	0.25
D₂	—	5.50	—
E₂	—	5.50	—