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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lfdfb-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101lfdfb-x0</a>

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
		Not mounted	D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
			A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

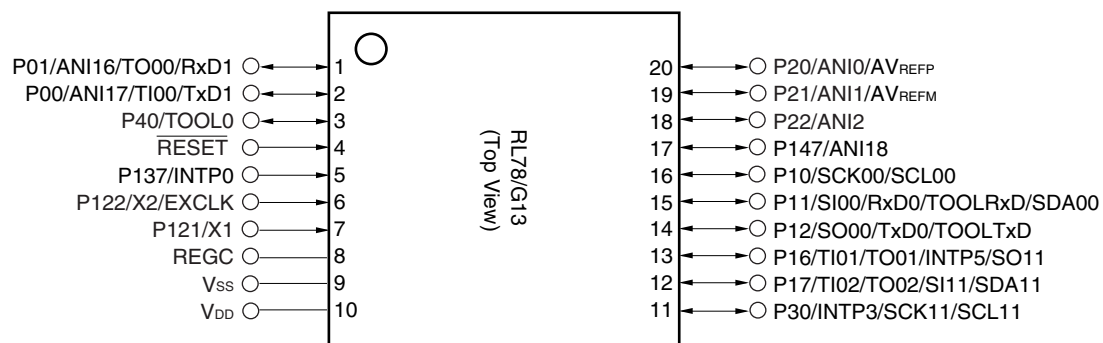
**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



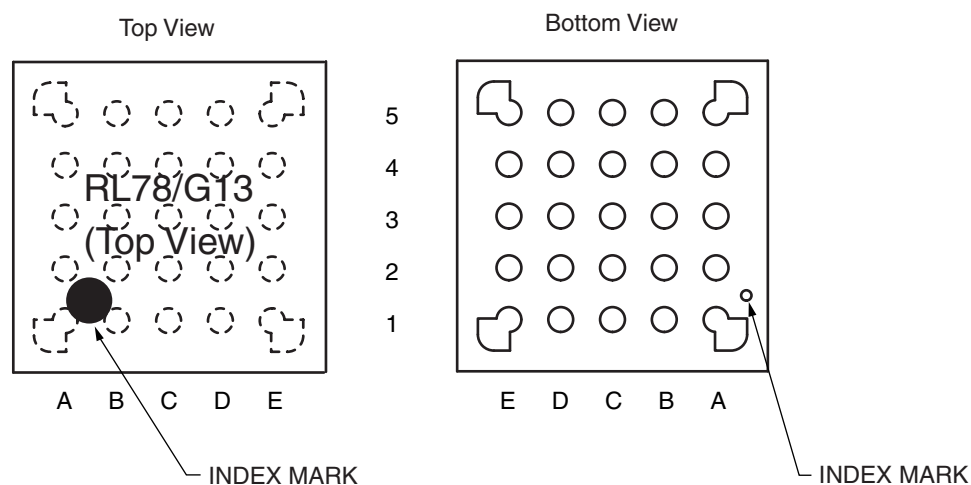
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remark** For pin identification, see 1.4 Pin Identification.

## 1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

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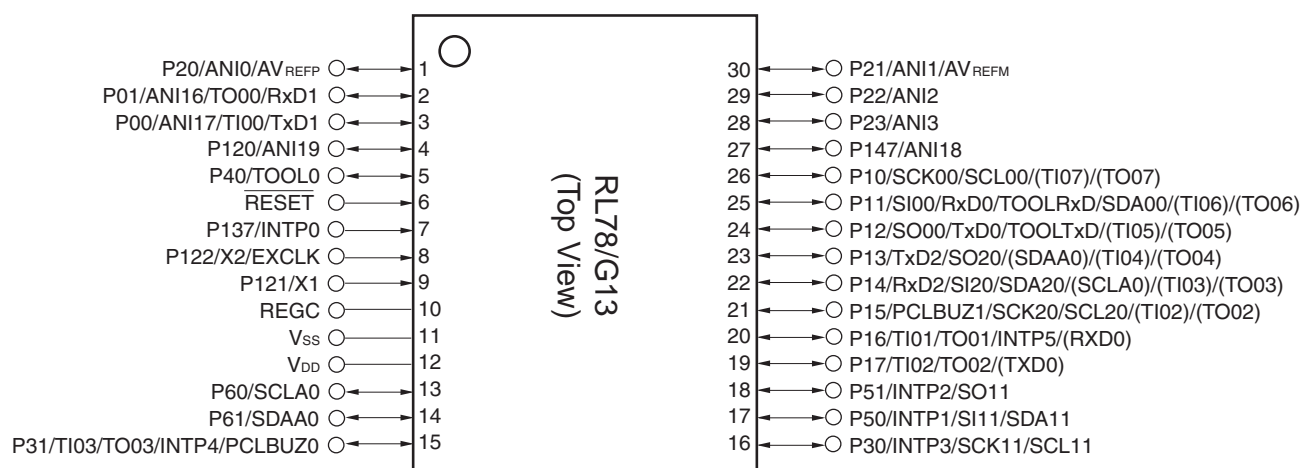
	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AV <sub>REFM</sub>	P10/SCK00/ SCL00	4
3	P121/X1	V <sub>DD</sub>	P20/ANI0/ AV <sub>REFP</sub>	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V <sub>SS</sub>	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remark** For pin identification, see 1.4 Pin Identification.

## 1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

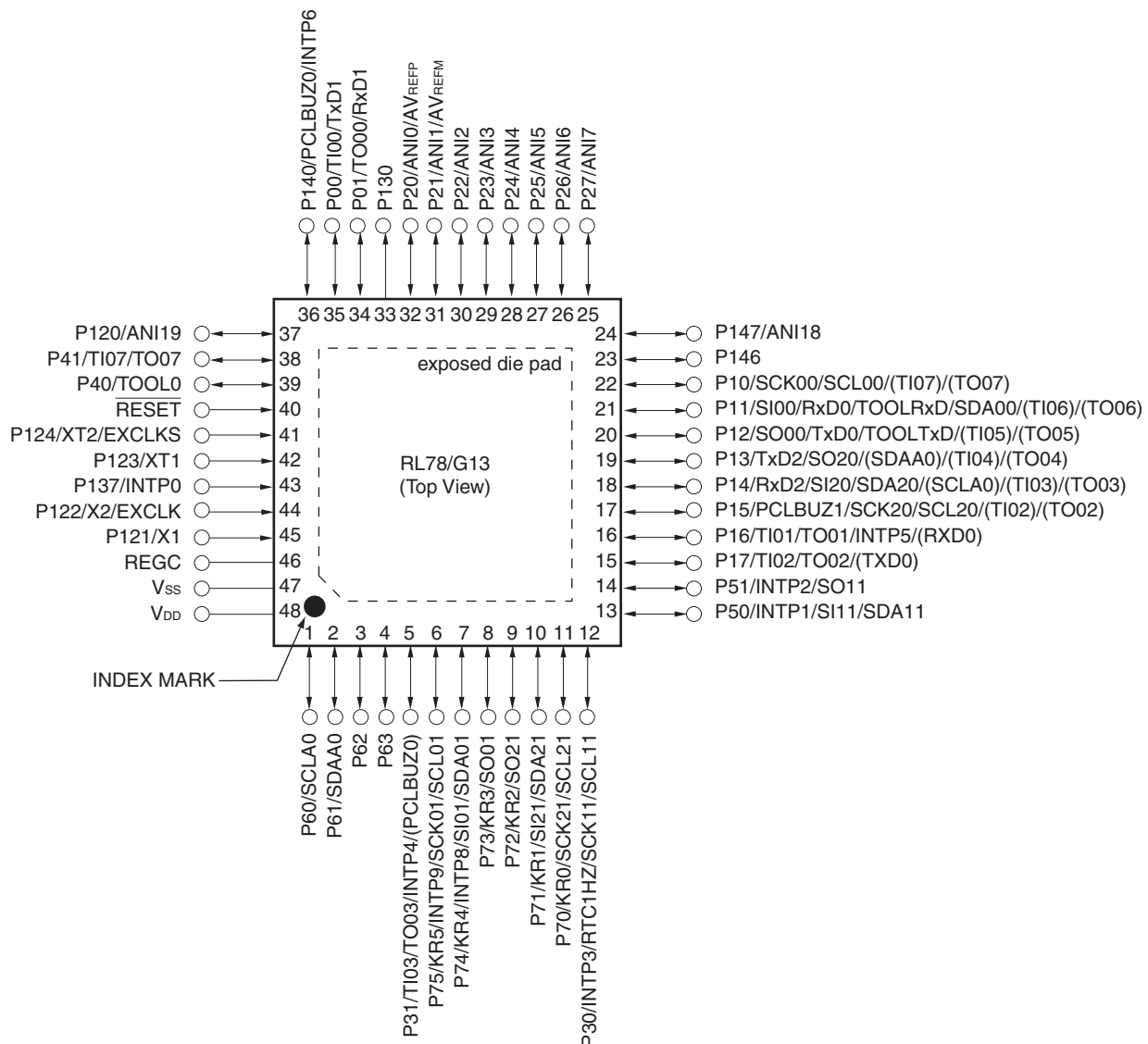


**Caution** Connect the REGC pin to V<sub>ss</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to V<sub>ss</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to V<sub>ss</sub>.

## 1.4 Pin Identification

ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI26:	Analog input	RESET:	Reset
AVREFM:	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EVDD0, EVDD1:	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EVSS0, EVSS1:	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30,	
KR0 to KR7:	Key return	SDA31:	Serial data input/output
P00 to P07:	Port 0	SI00, SI01, SI10, SI11,	
P10 to P17:	Port 1	SI20, SI21, SI30, SI31:	Serial data input
P20 to P27:	Port 2	SO00, SO01, SO10,	
P30 to P37:	Port 3	SO11, SO20, SO21,	
P40 to P47:	Port 4	SO30, SO31:	Serial data output
P50 to P57:	Port 5	TI00 to TI07,	
P60 to P67:	Port 6	TI10 to TI17:	Timer input
P70 to P77:	Port 7	TO00 to TO07,	
P80 to P87:	Port 8	TO10 to TO17:	Timer output
P90 to P97:	Port 9	TOOL0:	Data input/output for tool
P100 to P106:	Port 10	TOOLRxD, TOOLTxD:	Data input/output for external device
P110 to P117:	Port 11	TxD0 to TxD3:	Transmit data
P120 to P127:	Port 12	V <sub>DD</sub> :	Power supply
P130, P137:	Port 13	V <sub>SS</sub> :	Ground
P140 to P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
P150 to P156:	Port 15	XT1, XT2:	Crystal oscillator (subsystem clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		<ul style="list-style-type: none"><li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f<sub>MAIN</sub> = 20 MHz operation)</li><li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f<sub>SUB</sub> = 32.768 kHz operation)</li></ul>					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products]					
		<ul style="list-style-type: none"><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li></ul>					
	I <sup>2</sup> C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		<ul style="list-style-type: none"><li>16 bits × 16 bits = 32 bits (Unsigned or signed)</li><li>32 bits ÷ 32 bits = 32 bits (Unsigned)</li><li>16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)</li></ul>					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		<ul style="list-style-type: none"><li>Reset by <math>\overline{\text{RESET}}</math> pin</li><li>Internal reset by watchdog timer</li><li>Internal reset by power-on-reset</li><li>Internal reset by voltage detector</li><li>Internal reset by illegal instruction execution <sup>Note</sup></li><li>Internal reset by RAM parity error</li><li>Internal reset by illegal-memory access</li></ul>					
Power-on-reset circuit		<ul style="list-style-type: none"><li>Power-on-reset: 1.51 V (TYP.)</li><li>Power-down-reset: 1.50 V (TYP.)</li></ul>					
Voltage detector		<ul style="list-style-type: none"><li>Rising edge : 1.67 V to 4.06 V (14 stages)</li><li>Falling edge : 1.63 V to 3.98 V (14 stages)</li></ul>					
On-chip debug function		Provided					
Power supply voltage		V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)					
Operating ambient temperature		T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications ) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)					

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

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## (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 38		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t <sub>KSI1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t <sub>KSO1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			25		25		25	ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			—		25		25	ns

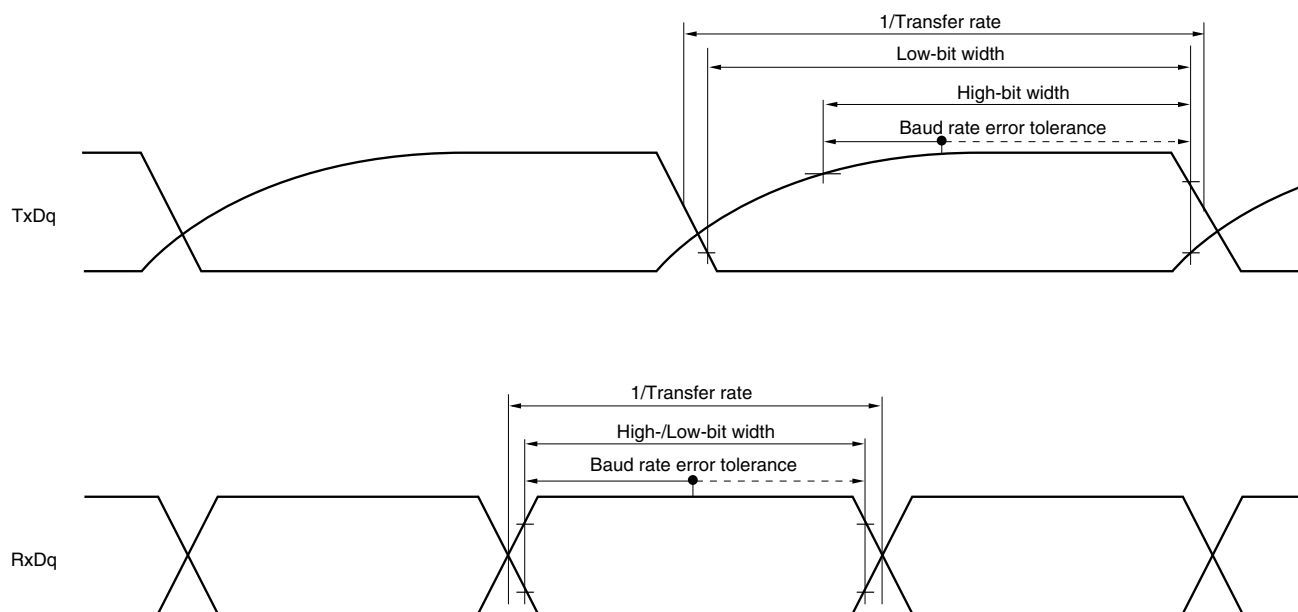
- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(5) During communication at same potential (simplified I<sup>2</sup>C mode) (1/2)(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV <sub>DD0</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV <sub>DD0</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)  
(1/3)(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t <sub>KH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 75		t <sub>KCY1</sub> /2 – 75		t <sub>KCY1</sub> /2 – 75		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 170		t <sub>KCY1</sub> /2 – 170		t <sub>KCY1</sub> /2 – 170		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 – 458		t <sub>KCY1</sub> /2 – 458		t <sub>KCY1</sub> /2 – 458		ns
SCKp low-level width	t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns

**Note** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

## 2.6.5 Power supply voltage rising slope characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	$S_{VDD}$				54	V/ms

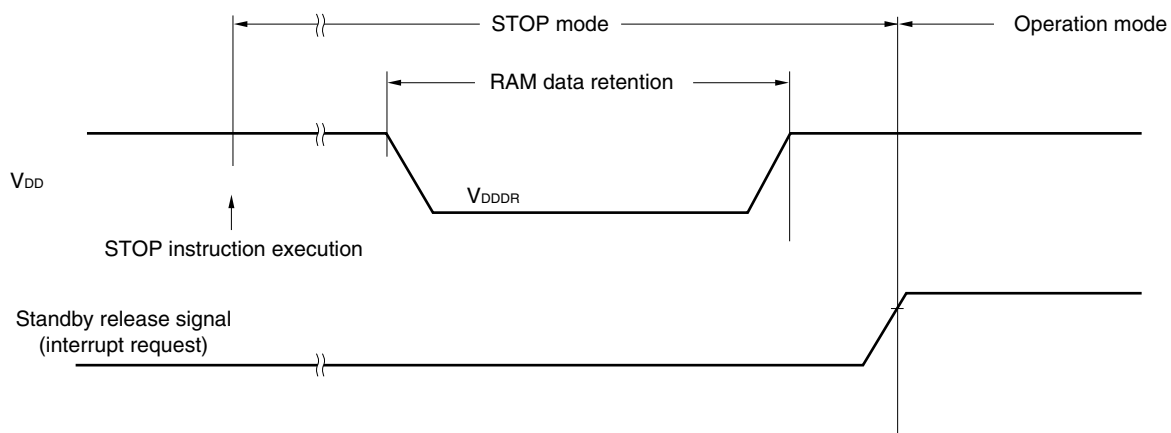
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until  $V_{DD}$  reaches the operating voltage range shown in 2.4 AC Characteristics.

## 2.7 RAM Data Retention Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.46 <sup>Note</sup>		5.5	V

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



## 2.8 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	$f_{CLK}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	$C_{erwr}$	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

**Notes** 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
 HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

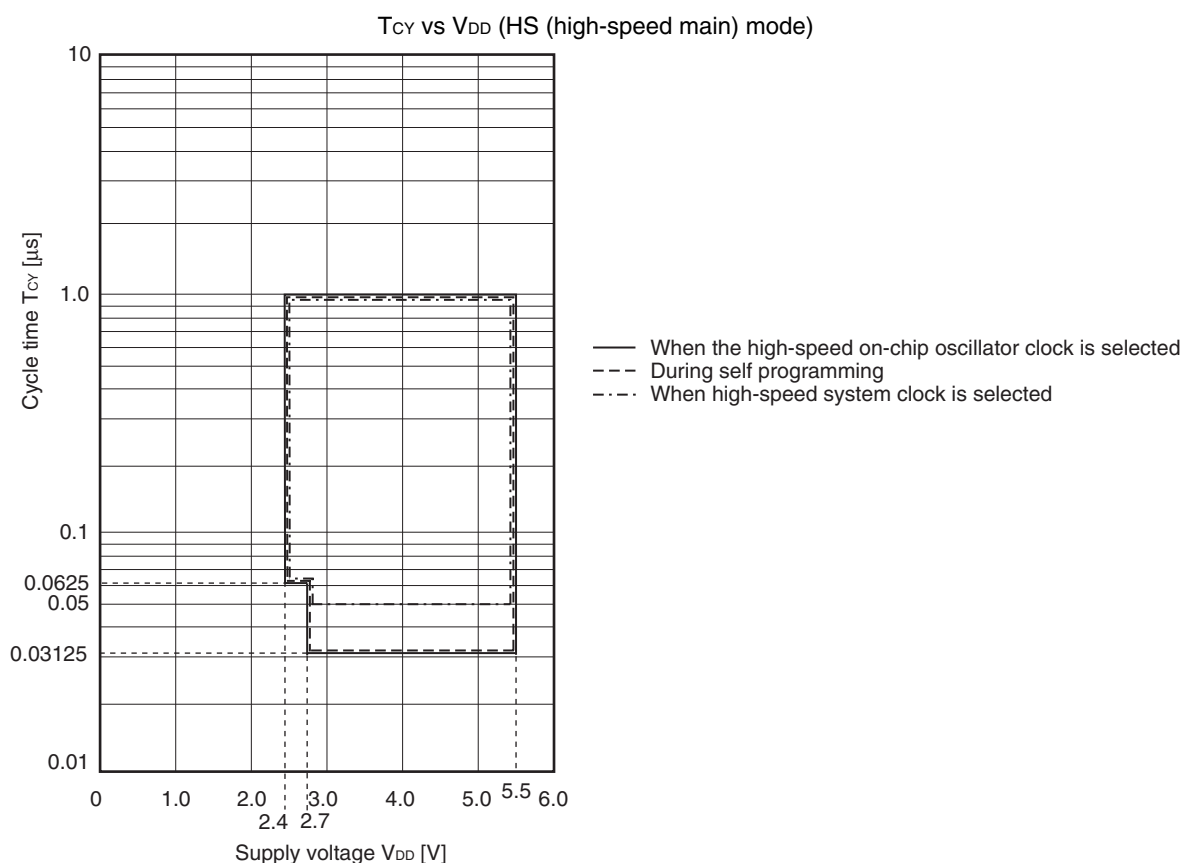
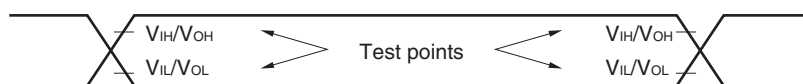
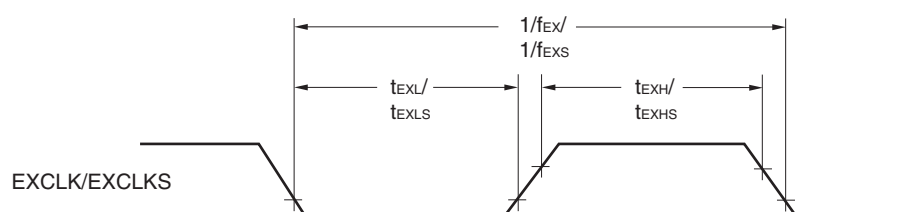
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$



**Minimum Instruction Execution Time during Main System Clock Operation****AC Timing Test Points****External System Clock Timing**

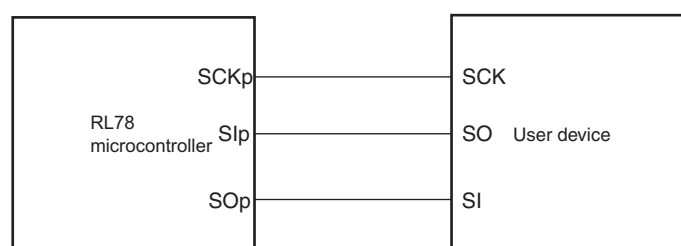
**(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time <sup>Note 5</sup>	t <sub>KCY2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	20 MHz < f <sub>MCK</sub>	16/f <sub>MCK</sub>		ns
			f <sub>MCK</sub> ≤ 20 MHz	12/f <sub>MCK</sub>		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	16 MHz < f <sub>MCK</sub>	16/f <sub>MCK</sub>		ns
			f <sub>MCK</sub> ≤ 16 MHz	12/f <sub>MCK</sub>		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		16/f <sub>MCK</sub>		ns
				12/f <sub>MCK</sub> and 1000		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 14		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 16		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 36		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK2</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +40		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +60		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI2</sub>	2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +62		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO2</sub>	C = 30 pF <sup>Note 4</sup>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +66	ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +113	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes “to SCKp $\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes “from SCKp $\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The delay time to SOp output becomes “from SCKp $\uparrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

**CSI mode connection diagram (during communication at same potential)**

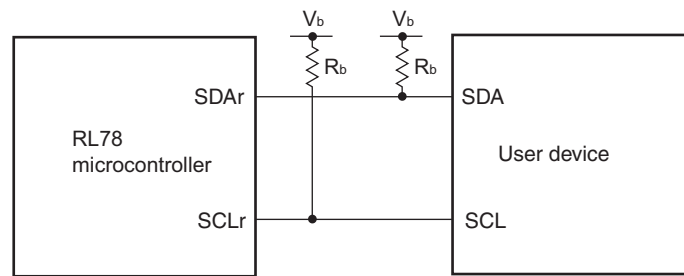
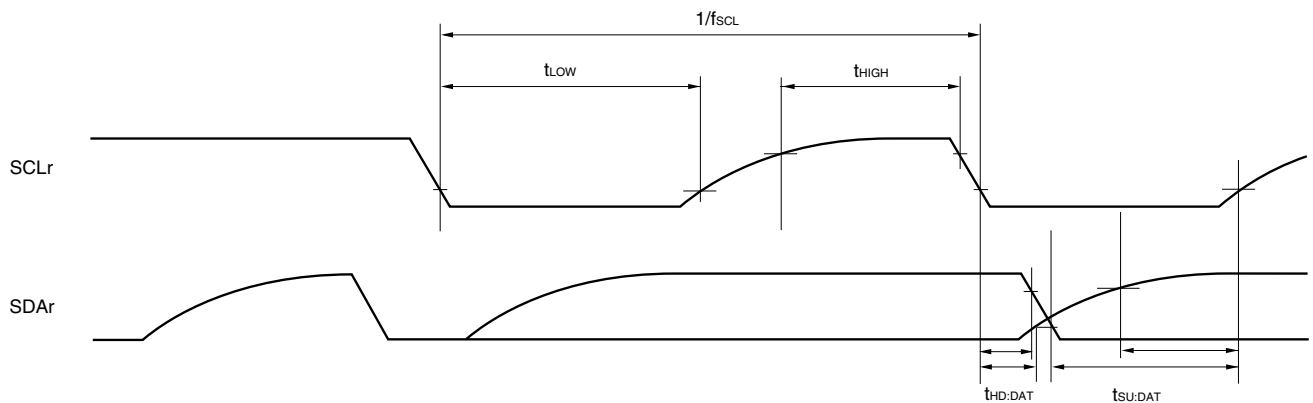
**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	$f_{\text{SCL}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		400 <sup>Note1</sup>	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$		100 <sup>Note1</sup>	
Hold time when SCLr = "L"	$t_{\text{LOW}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		
Hold time when SCLr = "H"	$t_{\text{HIGH}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ <sup>Note2</sup>		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ <sup>Note2</sup>		
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	0	1420	

**Notes** 1. The value must also be equal to or less than  $f_{\text{MCK}}/4$ .2. Set the  $f_{\text{MCK}}$  value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

**Caution** Select the TTL input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

## 4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA,  
 R5F100LKAFA, R5F100LLAFA  
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA,  
 R5F101LKAFA, R5F101LLAFA  
 R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LHDFA, R5F100LJDFA,  
 R5F100LK DFA, R5F100LLDFA  
 R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LHDFA, R5F101LJDFA,  
 R5F101LK DFA, R5F101LLDFA  
 R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,  
 R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

