What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101mjdfb-50

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	Mounted	A	R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0 R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0
			G	R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0 R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0
		Not mounted	A	R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0 R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0 R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0
			D	R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDSP#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0 R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDSP#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0
			G	R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0,R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0 R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0,R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0
		Not mounted	A	R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0 R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0
			D	R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDSP#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0 R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDSP#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	Mounted	A	R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0 R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0
			D	R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0 R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0
			G	R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0 R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0
		Not mounted	A	R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0 R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0
			D	R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0 R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.
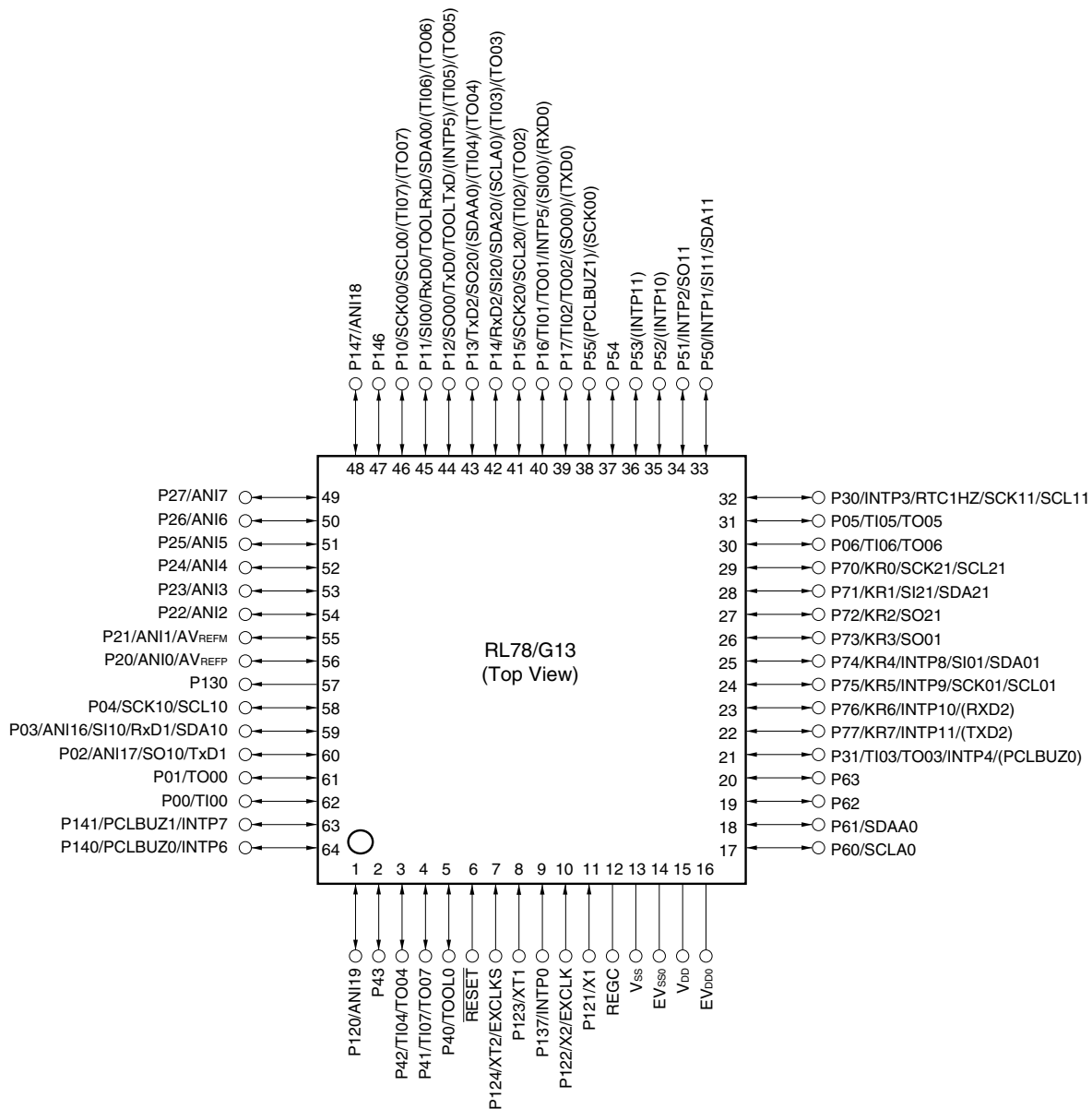
Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0
				R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0
			D	R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0
				R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0
			G	R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0
				R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0
		Not mounted	A	R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0
				R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0
			D	R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0
				R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.
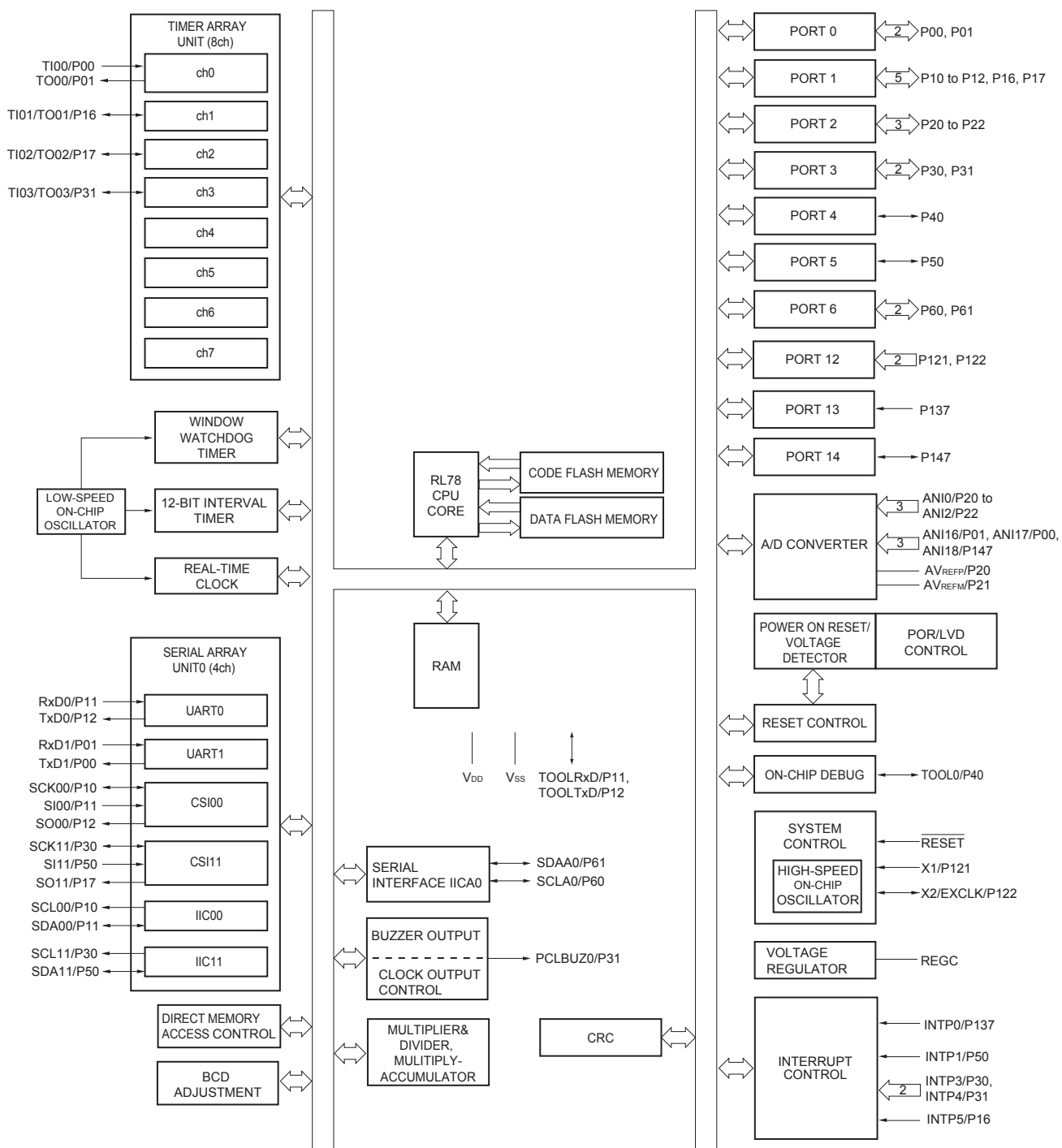
1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

Top pins (48–33):

P147/ANI18 (48), P146 (47), P10/SCK00/SCL00/(TI07)/(TO07) (46), P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06) (45), P12/SO00/TxD0/TOOLTxD/((INTP5)/(TI05)/(TO05) (44), P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04) (43), P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03) (42), P15/SCK20/SCL20/(TI02)/(TO02) (41), P16/TI01/TO01/INTP5/(SI00)/(RXD0) (40), P17/TI02/TO02/(SO00)/(TXD0) (39), P55/(PCLBUZ1)/(SCK00) (38), P54 (37), P53/(INTP11) (36), P52/(INTP10) (35), P51/INTP2/SO11 (34), P50/INTP1/SI11/SDA11 (33)

RL78/G13 (Top View)

Left pins (49–64):

P27/ANI7 (49), P26/ANI6 (50), P25/ANI5 (51), P24/ANI4 (52), P23/ANI3 (53), P22/ANI2 (54), P21/ANI1/AV$_{REFM}$ (55), P20/ANI0/AV$_{REFP}$ (56), P130 (57), P04/SCK10/SCL10 (58), P03/ANI16/SI10/RxD1/SDA10 (59), P02/ANI17/SO10/TxD1 (60), P01/TO00 (61), P00/TI00 (62), P141/PCLBUZ1/INTP7 (63), P140/PCLBUZ0/INTP6 (64)

Right pins (32–17):

P30/INTP3/RTC1HZ/SCK11/SCL11 (32), P05/TI05/TO05 (31), P06/TI06/TO06 (30), P70/KR0/SCK21/SCL21 (29), P71/KR1/SI21/SDA21 (28), P72/KR2/SO21 (27), P73/KR3/SO01 (26), P74/KR4/INTP8/SI01/SDA01 (25), P75/KR5/INTP9/SCK01/SCL01 (24), P76/KR6/INTP10/(RXD2) (23), P77/KR7/INTP11/(TXD2) (22), P31/TI03/TO03/INTP4/(PCLBUZ0) (21), P63 (20), P62 (19), P61/SDAA0 (18), P60/SCLA0 (17)

Bottom pins (1–16):

P120/ANI19 (1), P43 (2), P42/TI04/TO04 (3), P41/TI07/TO07 (4), P40/TOOL0 (5), RESET (6), P124/XT2/EXCLKS (7), P123/XT1 (8), P137/INTP0 (9), P122/X2/EXCLK (10), P121/X1 (11), REGC (12), V$_{SS}$ (13), EV$_{SS0}$ (14), V$_{DD}$ (15), EV$_{DD0}$ (16)

Cautions 1. Make EV$_{SS0}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins and connect the V$_{SS}$ and EV$_{SS0}$ pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.2 24-pin products

TIMER ARRAY UNIT (8ch)
- ch0 — TI00/P00, TO00/P01
- ch1 — TI01/TO01/P16
- ch2 — TI02/TO02/P17
- ch3 — TI03/TO03/P31
- ch4
- ch5
- ch6
- ch7

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12-BIT INTERVAL TIMER

REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)
- UART0 — RxD0/P11, TxD0/P12
- UART1 — RxD1/P01, TxD1/P00
- CSI00 — SCK00/P10, SI00/P11, SO00/P12
- CSI11 — SCK11/P30, SI11/P50, SO11/P17
- IIC00 — SCL00/P10, SDA00/P11
- IIC11 — SCL11/P30, SDA11/P50

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

RL78 CPU CORE

CODE FLASH MEMORY

DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61, SCLA0/P60

BUZZER OUTPUT
- - - - - - - - - - - - → PCLBUZ0/P31
CLOCK OUTPUT CONTROL

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

PORT 0 — 2 P00, P01

PORT 1 — 5 P10 to P12, P16, P17

PORT 2 — 3 P20 to P22

PORT 3 — 2 P30, P31

PORT 4 — P40

PORT 5 — P50

PORT 6 — 2 P60, P61

PORT 12 — 2 P121, P122

PORT 13 — P137

PORT 14 — P147

A/D CONVERTER
- 3 ANI0/P20 to ANI2/P22
- 3 ANI16/P01, ANI17/P00, ANI18/P147
- AV$_{REFP}$/P20
- AV$_{REFM}$/P21

POWER ON RESET/ VOLTAGE DETECTOR   POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL   RESET
HIGH-SPEED ON-CHIP OSCILLATOR
- X1/P121
- X2/EXCLK/P122

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- INTP0/P137
- INTP1/P50
- 2 INTP3/P30, INTP4/P31
- INTP5/P16

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel					
	I²C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)					
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)					
On-chip debug function		Provided					
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)					
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)					

<R>

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (T$_A$ = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications T$_A$ = −40 to +85°C

R5F100xxAxx, R5F101xxAxx

D: Industrial applications T$_A$ = −40 to +85°C

R5F100xxDxx, R5F101xxDxx

G: Industrial applications when T$_A$ = −40 to +105°C products is used in the range of T$_A$ = −40 to +85°C

R5F100xxGxx

Cautions 1. **The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

2. **With products not provided with an EV$_{DD0}$, EV$_{DD1}$, EV$_{SS0}$, or EV$_{SS1}$ pin, replace EV$_{DD0}$ and EV$_{DD1}$ with V$_{DD}$, or replace EV$_{SS0}$ and EV$_{SS1}$ with V$_{SS}$.**

3. **The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.**

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V$_{DD}$		−0.5 to +6.5	V
	EV$_{DD0}$, EV$_{DD1}$	EV$_{DD0}$ = EV$_{DD1}$	−0.5 to +6.5	V
	EV$_{SS0}$, EV$_{SS1}$	EV$_{SS0}$ = EV$_{SS1}$	−0.5 to +0.3	V
REGC pin input voltage	V$_{IREGC}$	REGC	−0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1]	V
Input voltage	V$_{I1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{I2}$	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V$_{I3}$	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{RESET}$	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Output voltage	V$_{O1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{O2}$	P20 to P27, P150 to P156	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Analog input voltage	V$_{AI1}$	ANI16 to ANI26	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V
	V$_{AI2}$	ANI0 to ANI14	−0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
  2. Must be 6.5 V or lower.
  3. Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
  2. AV$_{REF}$ (+) : + side reference voltage of the A/D converter.
  3. V$_{SS}$: Reference voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			15.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			9.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			35.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			20.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P156				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$, EV$_{SS1}$ and V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

\<Example\> Where n = 80% and I$_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2　Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (high-speed main) mode [Note 5]	f$_{IH}$ = 32 MHz [Note 3]	Basic operation	V$_{DD}$ = 5.0 V		2.1		mA
						V$_{DD}$ = 3.0 V		2.1		mA
					Normal operation	V$_{DD}$ = 5.0 V		4.6	7.0	mA
						V$_{DD}$ = 3.0 V		4.6	7.0	mA
				f$_{IH}$ = 24 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		3.7	5.5	mA
						V$_{DD}$ = 3.0 V		3.7	5.5	mA
				f$_{IH}$ = 16 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		2.7	4.0	mA
						V$_{DD}$ = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode [Note 5]	f$_{IH}$ = 8 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.2	1.8	mA
						V$_{DD}$ = 2.0 V		1.2	1.8	mA
			LV (low-voltage main) mode [Note 5]	f$_{IH}$ = 4 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.2	1.7	mA
						V$_{DD}$ = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode [Note 5]	f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			LS (low-speed main) mode [Note 5]	f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = –40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 32 MHz
2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                     2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

    LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

    LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

Remarks 1.   p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

       g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

   2.   f$_{MCK}$: Serial array unit operation clock frequency

       (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

       n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

     2. Use it with EV$_{DD0}$ ≥ V$_b$.

     3. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (–) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]		1.2	±8.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target ANI pin : ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±0.60	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI26		0		AV$_{REFP}$ and EV$_{DD0}$	V

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

4. When AV$_{REFP}$ < EV$_{DD0}$ ≤ V$_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol		Conditions			MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	3.40	mA
					V$_{DD}$ = 3.0 V		0.62	3.40	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	2.70	mA
					V$_{DD}$ = 3.0 V		0.50	2.70	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.90	mA
					V$_{DD}$ = 3.0 V		0.44	1.90	mA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +105°C	Square wave input		5.50	41.00	μA
					Resonator connection		5.50	41.00	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.19	0.52	μA
			T$_A$ = +25°C				0.25	0.52	μA
			T$_A$ = +50°C				0.32	2.21	μA
			T$_A$ = +70°C				0.55	3.94	μA
			T$_A$ = +85°C				1.00	7.95	μA
			T$_A$ = +105°C				5.00	40.00	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

3.4 AC Characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
		Subsystem clock (f$_{SUB}$) operation		2.4 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns**Note**
TO00 to TO07, TO10 to TO17 output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
		INTP1 to INTP11	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		1			μs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		250			ns
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

Note The following conditions are required for low voltage interface when EV$_{DD0}$ < V$_{DD}$
2.4V ≤ EV$_{DD0}$ < 2.7 V : MIN. 125 ns

Remark f$_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

3.5 Peripheral Functions Characteristics

AC Timing Test Points
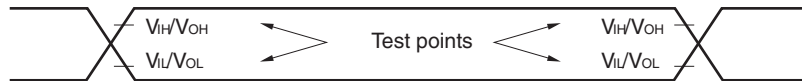
3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate [Note 1]				$f_{MCK}/12$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
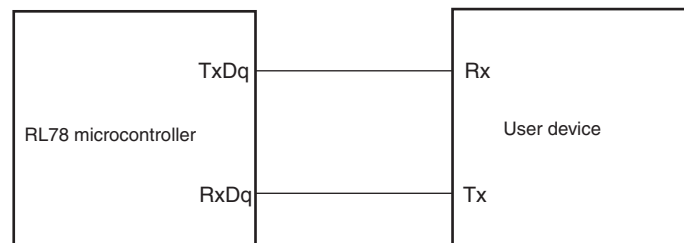
UART mode bit width (during communication at same potential) (reference)
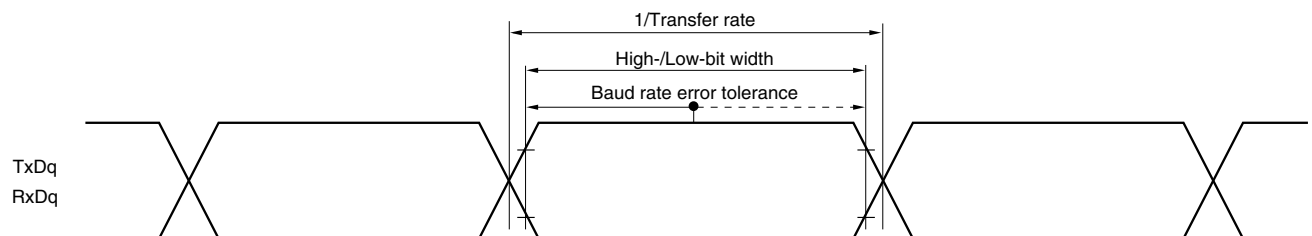
Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (1/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		100 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		100 [Note 1]	kHz
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	4600		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	4600		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	620		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	500		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	2700		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	2400		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1830		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ $^{Note 3}$, Reference voltage (−) = AV$_{REFM}$ $^{Note 4}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs