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### What is "[Embedded - Microcontrollers](#)"?

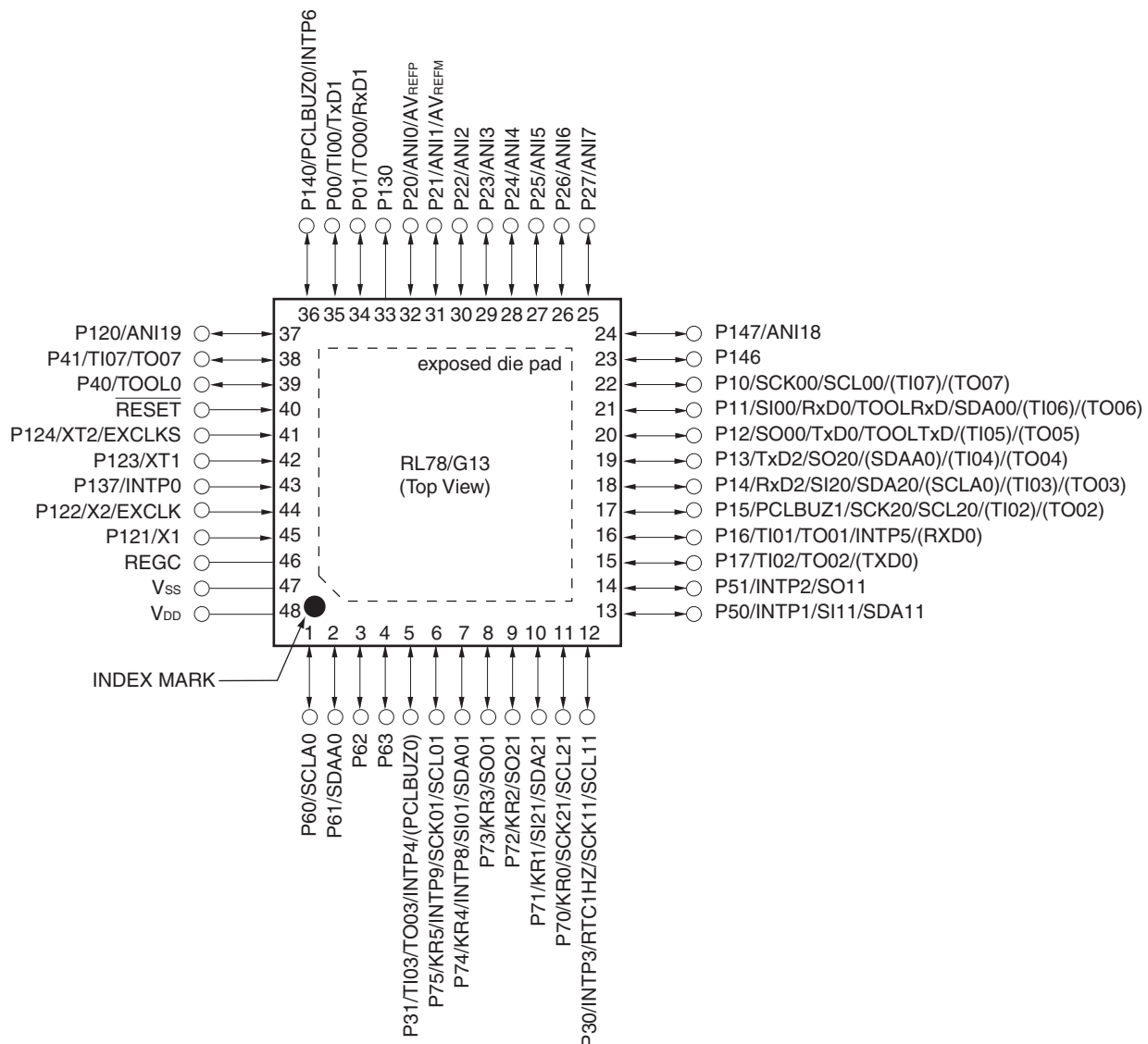
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101mjdfb-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101mjdfb-x0</a>

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



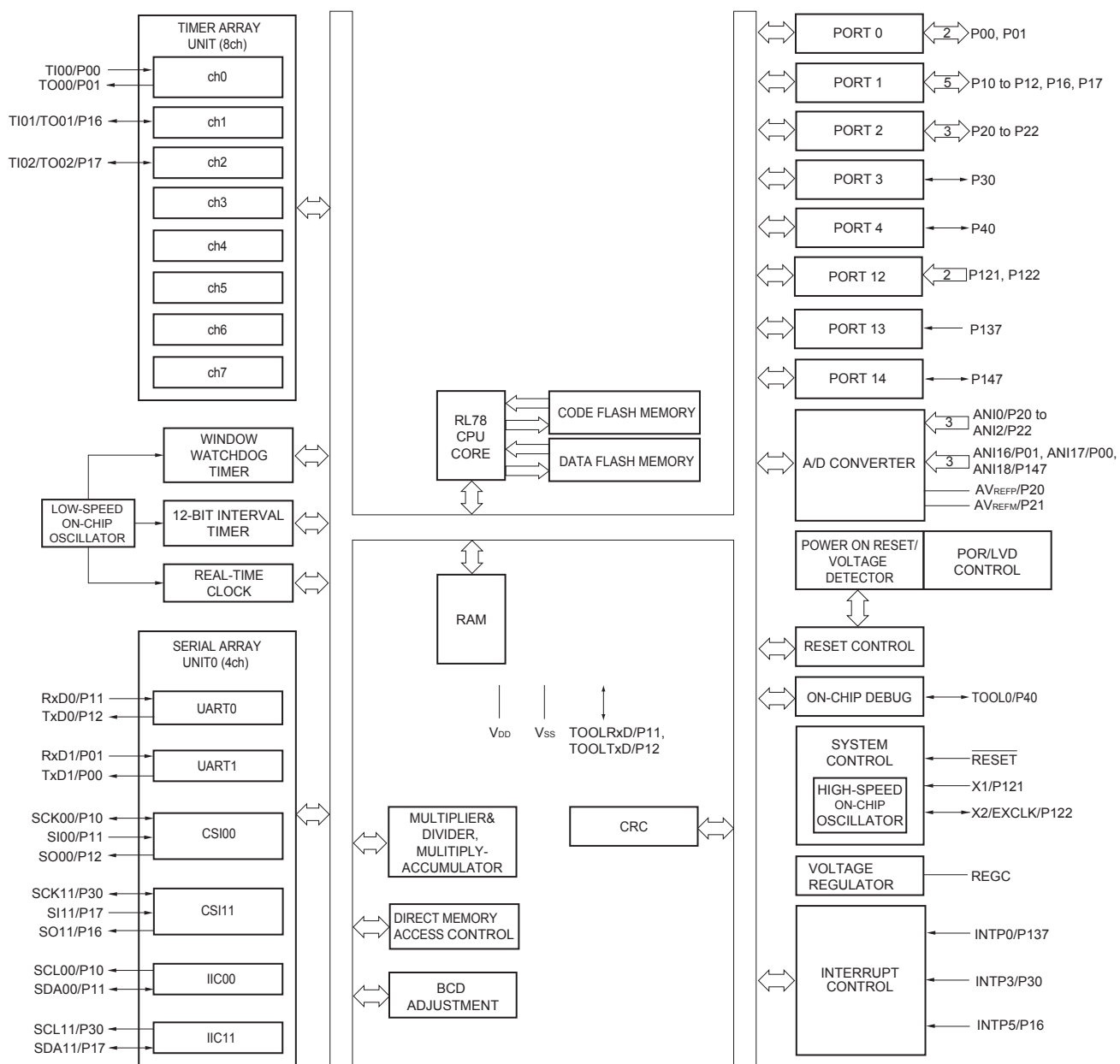
**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

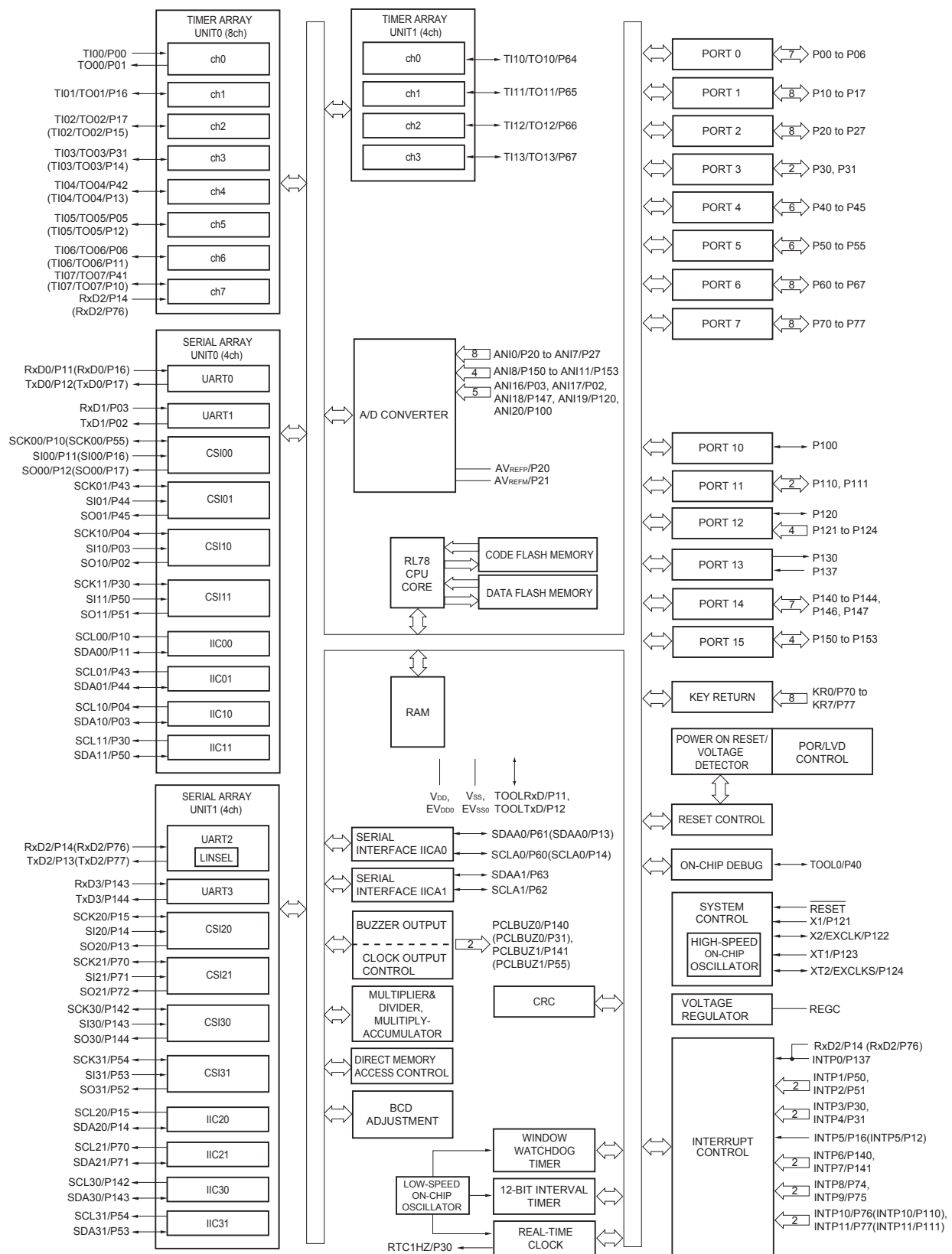
- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to Vss.

## 1.5 Block Diagram

### 1.5.1 20-pin products



## 1.5.12 80-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output	—		1		1		2		2		2	
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation)											
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface	[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I <sup>2</sup> C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I <sup>2</sup> C bus	—	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller	2 channels											
Vectored interrupt sources	Internal	23	24		24		27		27		27	
	External	3	5		5		6		6		6	
Key interrupt	—											
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector	• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function	Provided											
Power supply voltage	V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)											
Operating ambient temperature	T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications ) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)											

**Note** The illegal instruction is generated when instruction code FFH is executed.

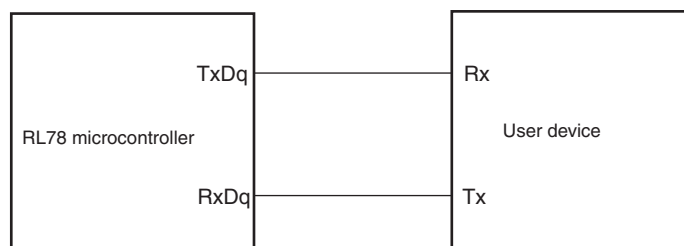
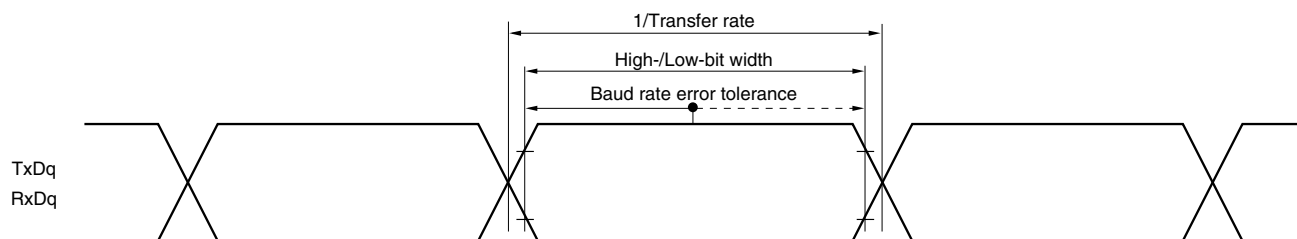
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

- Notes**
1. Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz
    - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

- Notes**
1. Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz
    - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
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  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**UART mode connection diagram (during communication at same potential)****UART mode bit width (during communication at same potential) (reference)**

**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

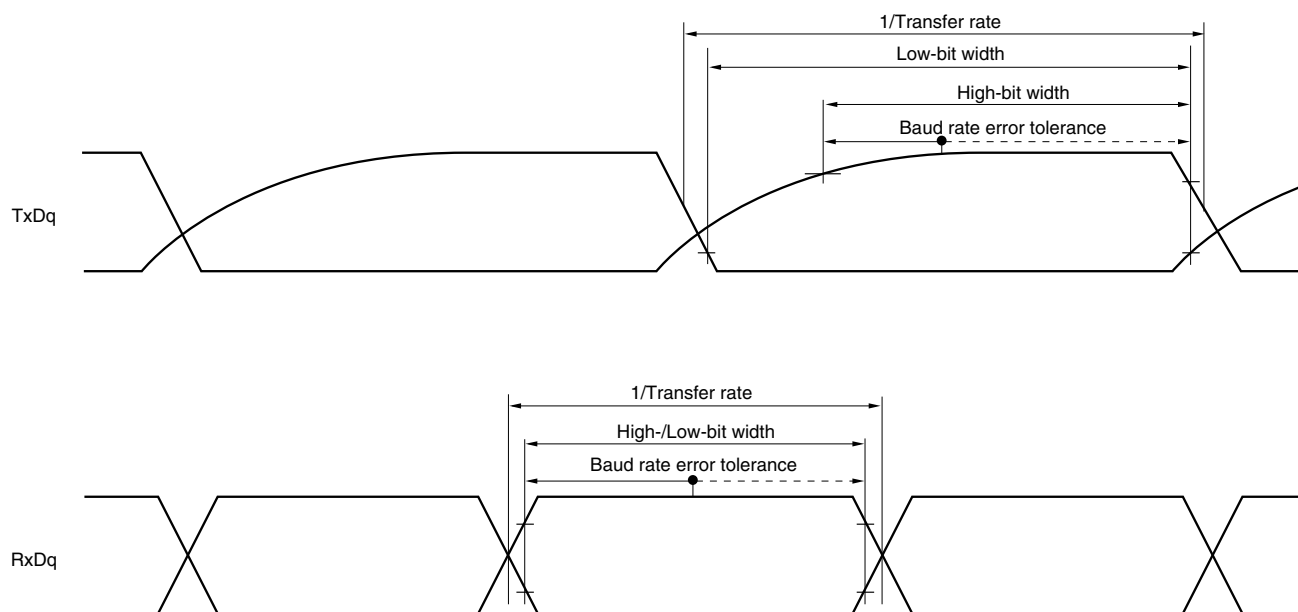


- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
- 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)**  
**(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

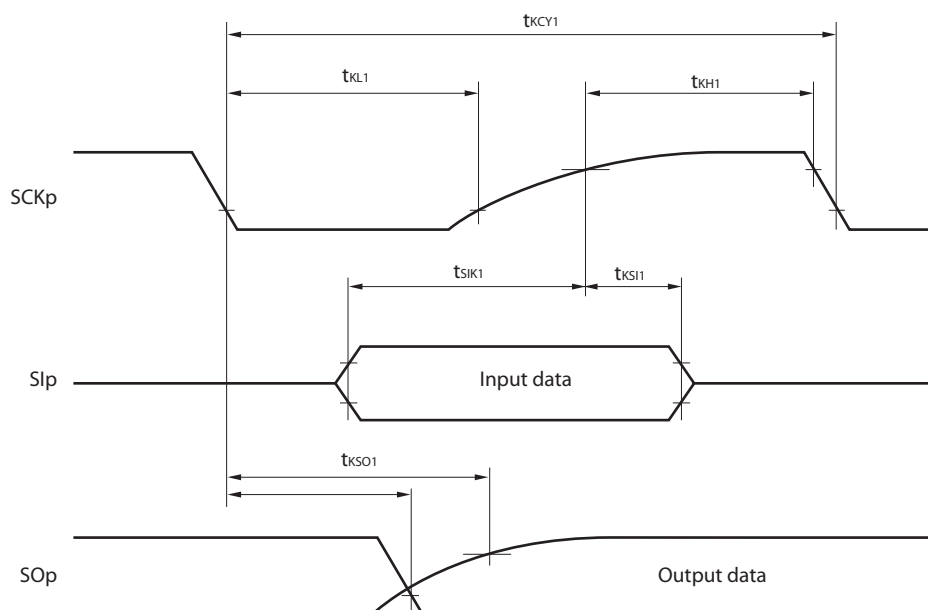
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <small>Note 5</small>	t <sub>KCY2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	20 MHz < f <sub>MCK</sub>	8/f <sub>MCK</sub>		—		—		ns
			f <sub>MCK</sub> ≤ 20 MHz	6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	16 MHz < f <sub>MCK</sub>	8/f <sub>MCK</sub>		—		—		ns
			f <sub>MCK</sub> ≤ 16 MHz	6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 500		6/f <sub>MCK</sub> and 500		6/f <sub>MCK</sub> and 500		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 750		6/f <sub>MCK</sub> and 750		6/f <sub>MCK</sub> and 750		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 7		t <sub>KCY2</sub> /2 – 7		t <sub>KCY2</sub> /2 – 7		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 8		t <sub>KCY2</sub> /2 – 8		t <sub>KCY2</sub> /2 – 8		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 18		t <sub>KCY2</sub> /2 – 18		t <sub>KCY2</sub> /2 – 18		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		ns

(Notes, Caution, and Remarks are listed on the next page.)

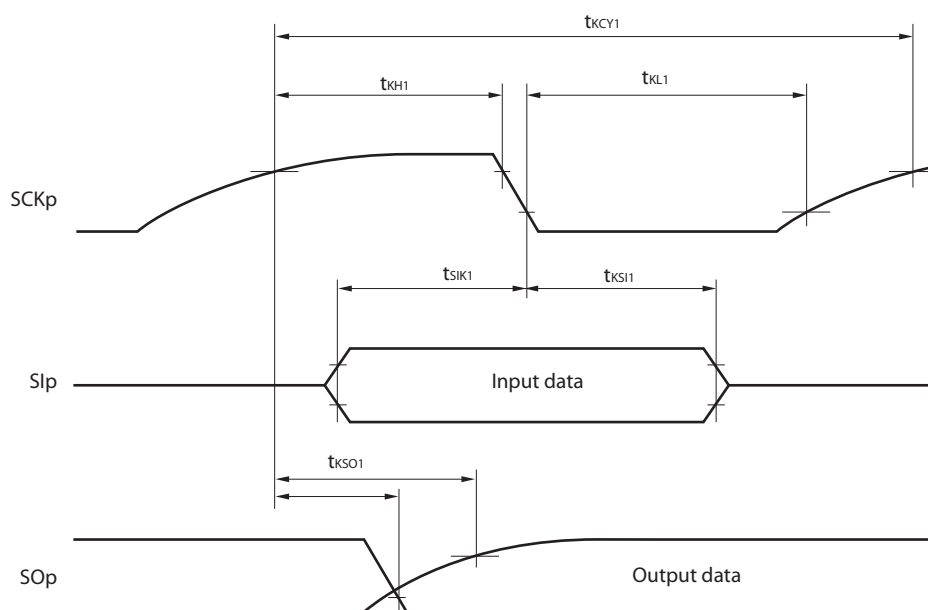
**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

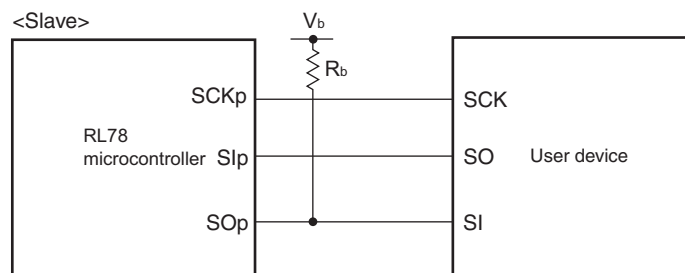
**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage
  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

## 2.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		VLVD1	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		VLVD2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVD3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVD4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVD5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVD6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVD8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVD9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVD10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVD11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		VLVD12	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		VLVD13	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

### 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products G: Industrial applications  $T_A = -40$  to  $+105^\circ\text{C}$   
R5F100xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $\text{EV}_{\text{DD0}}$ ,  $\text{EV}_{\text{DD1}}$ ,  $\text{EV}_{\text{SS0}}$ , or  $\text{EV}_{\text{SS1}}$  pin, replace  $\text{EV}_{\text{DD0}}$  and  $\text{EV}_{\text{DD1}}$  with  $V_{\text{DD}}$ , or replace  $\text{EV}_{\text{SS0}}$  and  $\text{EV}_{\text{SS1}}$  with  $V_{\text{SS}}$ .
  3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.
  4. Please contact Renesas Electronics sales office for derating of operation under  $T_A = +85^\circ\text{C}$  to  $+105^\circ\text{C}$ . Derating is the systematic reduction of load for the sake of improved reliability.

**Remark** When RL78/G13 is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$ , see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ( $T_A = -40$  to  $+85^\circ\text{C}$ )**.

There are following differences between the products "G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ )" and the products "A: Consumer applications, and D: Industrial applications".

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz}$ to $16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to $-20^\circ\text{C}$ $1.6\text{ V} \leq V_{\text{DD}} < 1.8\text{ V}$ $\pm 5.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\% @ T_A = -40$ to $-20^\circ\text{C}$	$2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 2.0\% @ T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to $-20^\circ\text{C}$
Serial array unit	UART CSI: $f_{\text{CLK}}/2$ (supporting $16\text{ Mbps}$ ), $f_{\text{CLK}}/4$ Simplified $\text{I}^2\text{C}$ communication	UART CSI: $f_{\text{CLK}}/4$ Simplified $\text{I}^2\text{C}$ communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: $1.67\text{ V}$ to $4.06\text{ V}$ (14 levels) Fall detection voltage: $1.63\text{ V}$ to $3.98\text{ V}$ (14 levels)	Rise detection voltage: $2.61\text{ V}$ to $4.06\text{ V}$ (8 levels) Fall detection voltage: $2.55\text{ V}$ to $3.98\text{ V}$ (8 levels)

(Remark is listed on the next page.)

### 3.2 Oscillator Characteristics

#### 3.2.1 X1, XT1 oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
XT1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>	Crystal resonator		32	32.768	35	kHz

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

#### 3.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Notes 1, 2</sup>	$f_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		$-20$ to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		+1.0	%
		$-40$ to $-20^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
		$+85$ to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	$f_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

**( $T_A = -40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (5/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I <sub>LH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>DD0</sub>			1	μA	
	I <sub>LH2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>DD</sub>			1	μA	
	I <sub>LH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub>			−1	μA	
	I <sub>LIL2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>SS</sub>			−1	μA	
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>	In input port or external clock input		−1	μA	
				In resonator connection		−10	μA	
On-chip pll-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub> , In input port		10	20	100	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
 HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
 HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
  8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

## (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T<sub>A</sub> =  $-40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

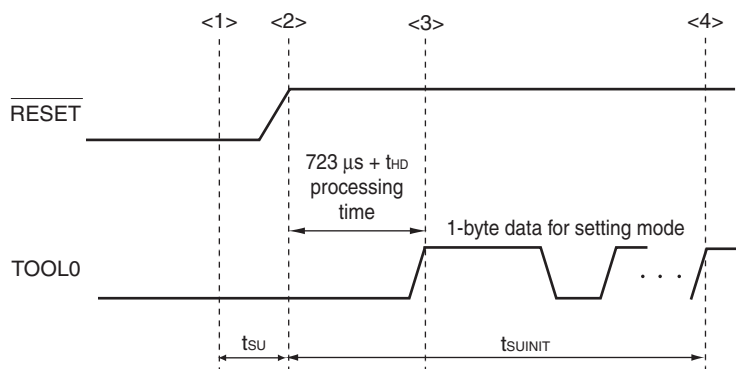
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time <sup>Note 1</sup>	t <sub>KCY2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$28/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$20/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$40/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$28/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$96/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$72/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$64/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$52/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$20/f_{\text{MCK}}$		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$t_{\text{KCY2}}/2 - 24$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$t_{\text{KCY2}}/2 - 36$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ <sup>Note 2</sup>		$t_{\text{KCY2}}/2 - 100$		ns
Slp setup time (to SCKp↑) <sup>Note 2</sup>	t <sub>SIK2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp↑) <sup>Note 3</sup>	t <sub>KSI2</sub>			$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp↓ to SOp output <sup>Note 4</sup>	t <sub>KSO2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 240$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$			$2/f_{\text{MCK}} + 428$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$			$2/f_{\text{MCK}} + 1146$	ns

(Notes, Caution and Remarks are listed on the next page.)

## 3.10 Timing of Entry to Flash Memory Programming Modes

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset must be released before the external reset is released.	1			ms



&lt;1&gt; The low level is input to the TOOL0 pin.

&lt;2&gt; The external reset is released (POR and LVD reset must be released before the external reset is released.).

&lt;3&gt; The TOOL0 pin is set to the high level.

&lt;4&gt; Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

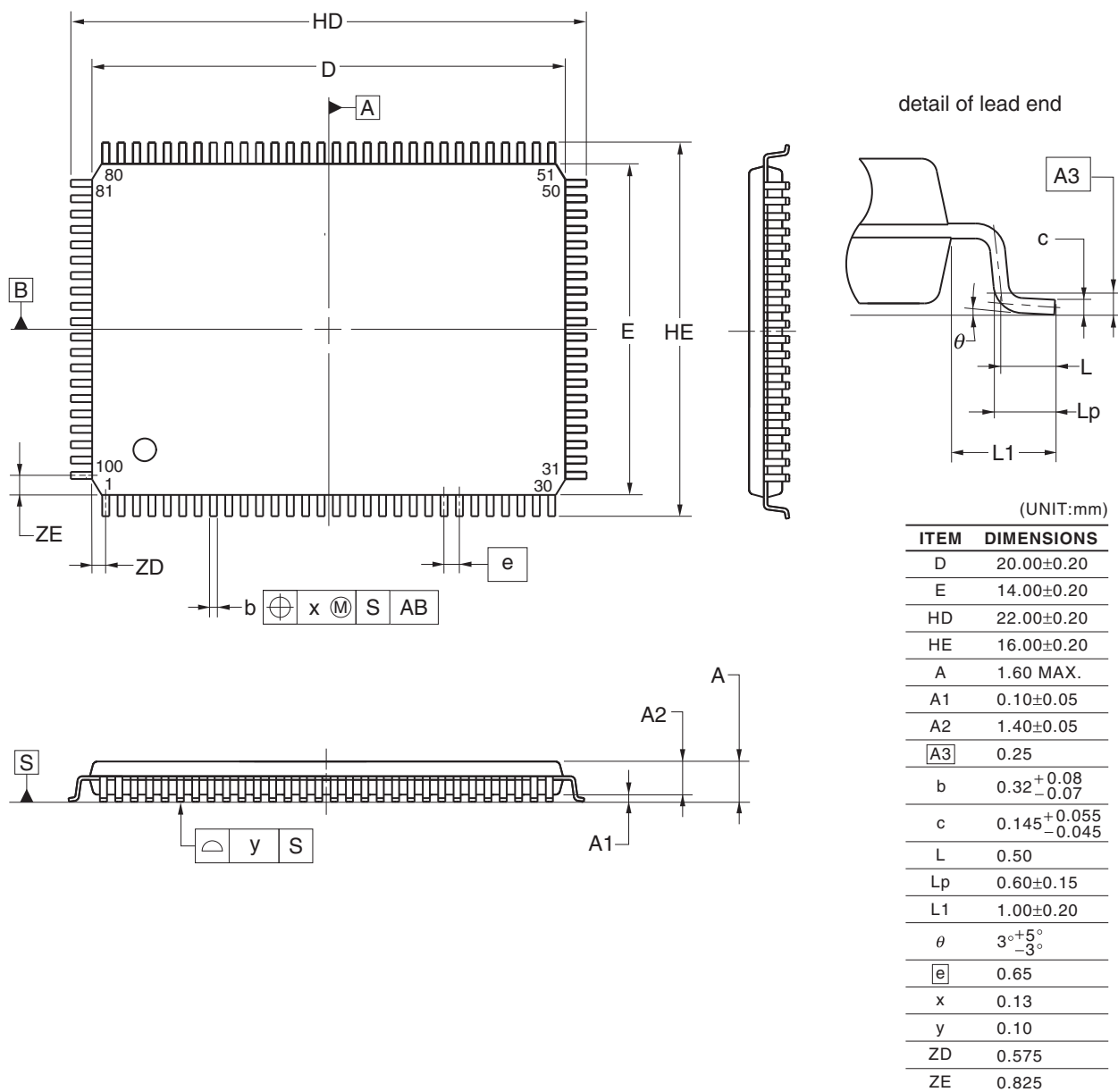
**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJFAFA, R5F100PKAFA, R5F100PLAFA  
 R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJFAFA, R5F101PKAFA, R5F101PLAFA  
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA  
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA  
 R5F100PFGFA, R5F100PGGFA, R5F100PHGFA, R5F100PJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



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