Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101mlafb-v0

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V$_{DD}$		−0.5 to +6.5	V
	EV$_{DD0}$, EV$_{DD1}$	EV$_{DD0}$ = EV$_{DD1}$	−0.5 to +6.5	V
	EV$_{SS0}$, EV$_{SS1}$	EV$_{SS0}$ = EV$_{SS1}$	−0.5 to +0.3	V
REGC pin input voltage	V$_{IREGC}$	REGC	−0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1]	V
Input voltage	V$_{I1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{I2}$	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V$_{I3}$	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Output voltage	V$_{O1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{O2}$	P20 to P27, P150 to P156	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Analog input voltage	V$_{AI1}$	ANI16 to ANI26	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V
	V$_{AI2}$	ANI0 to ANI14	−0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

    2. Must be 6.5 V or lower.

    3. Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

    2. AV$_{REF}$ (+) : + side reference voltage of the A/D converter.

    3. V$_{SS}$: Reference voltage

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)[Note]	Ceramic resonator/ crystal resonator	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	1.0		20.0	MHz
		2.4 V $\leq$ V$_{DD}$ < 2.7 V	1.0		16.0	MHz
		1.8 V $\leq$ V$_{DD}$ < 2.4 V	1.0		8.0	MHz
		1.6 V $\leq$ V$_{DD}$ < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f$_X$)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	f$_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	−1.0		+1.0	%
			1.6 V $\leq$ V$_{DD}$ < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	−1.5		+1.5	%
			1.6 V $\leq$ V$_{DD}$ < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

   2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			15.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			9.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			35.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			20.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P156				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$, EV$_{SS1}$ and V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −10.0 mA	EV$_{DD0}$ − 1.5			V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
			1.6 V $\leq$ EV$_{DD0}$ < 5.5 V, I$_{OH1}$ = −1.0 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 20 mA			1.3	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
			1.6 V $\leq$ EV$_{DD0}$ < 5.5 V, I$_{OL1}$ = 0.3 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V
			1.6 V $\leq$ EV$_{DD0}$ < 5.5 V, I$_{OL3}$ = 1.0 mA			0.4	V

Caution **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	1.86	mA
					V$_{DD}$ = 3.0 V		0.62	1.86	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	1.45	mA
					V$_{DD}$ = 3.0 V		0.50	1.45	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.11	mA
					V$_{DD}$ = 3.0 V		0.44	1.11	mA
			LS (low-speed main) mode [Note 7]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		290	620	μA
					V$_{DD}$ = 2.0 V		290	620	μA
			LV (low-voltage main) mode [Note 7]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		440	680	μA
					V$_{DD}$ = 2.0 V		440	680	μA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
			LS (low-speed main) mode [Note 7]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.19	0.52	μA
			T$_A$ = +25°C				0.25	0.52	μA
			T$_A$ = +50°C				0.32	2.21	μA
			T$_A$ = +70°C				0.55	3.94	μA
			T$_A$ = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

| Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD2} [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f_{IH} = 32 MHz [Note 4]	V_{DD} = 5.0 V		0.62	1.89	mA
					V_{DD} = 3.0 V		0.62	1.89	mA
				f_{IH} = 24 MHz [Note 4]	V_{DD} = 5.0 V		0.50	1.48	mA
					V_{DD} = 3.0 V		0.50	1.48	mA
				f_{IH} = 16 MHz [Note 4]	V_{DD} = 5.0 V		0.44	1.12	mA
					V_{DD} = 3.0 V		0.44	1.12	mA
			LS (low-speed main) mode [Note 7]	f_{IH} = 8 MHz [Note 4]	V_{DD} = 3.0 V		290	620	μA
					V_{DD} = 2.0 V		290	620	μA
			LV (low-voltage main) mode [Note 7]	f_{IH} = 4 MHz [Note 4]	V_{DD} = 3.0 V		460	700	μA
					V_{DD} = 2.0 V		460	700	μA
			HS (high-speed main) mode [Note 7]	f_{MX} = 20 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		0.31	1.14	mA
					Resonator connection		0.48	1.34	mA
				f_{MX} = 20 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		0.31	1.14	mA
					Resonator connection		0.48	1.34	mA
				f_{MX} = 10 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		0.21	0.68	mA
					Resonator connection		0.28	0.76	mA
				f_{MX} = 10 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		0.21	0.68	mA
					Resonator connection		0.28	0.76	mA
			LS (low-speed main) mode [Note 7]	f_{MX} = 8 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		110	390	μA
					Resonator connection		160	450	μA
				f_{MX} = 8 MHz [Note 3], V_{DD} = 2.0 V	Square wave input		110	390	μA
					Resonator connection		160	450	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz [Note 5] T_A = −40°C	Square wave input		0.31	0.66	μA
					Resonator connection		0.50	0.85	μA
				f_{SUB} = 32.768 kHz [Note 5] T_A = +25°C	Square wave input		0.38	0.66	μA
					Resonator connection		0.57	0.85	μA
				f_{SUB} = 32.768 kHz [Note 5] T_A = +50°C	Square wave input		0.47	3.49	μA
					Resonator connection		0.66	3.68	μA
				f_{SUB} = 32.768 kHz [Note 5] T_A = +70°C	Square wave input		0.80	6.10	μA
					Resonator connection		0.99	6.29	μA
				f_{SUB} = 32.768 kHz [Note 5] T_A = +85°C	Square wave input		1.52	10.46	μA
					Resonator connection		1.71	10.65	μA
	I_{DD3} [Note 6]	STOP mode [Note 8]	T_A = −40°C				0.19	0.54	μA
			T_A = +25°C				0.26	0.54	μA
			T_A = +50°C				0.35	3.37	μA
			T_A = +70°C				0.68	5.98	μA
			T_A = +85°C				1.40	10.34	μA

(**Notes** and **Remarks** are listed on the next page.)

Simplified I^{2}C mode mode connection diagram (during communication at same potential)
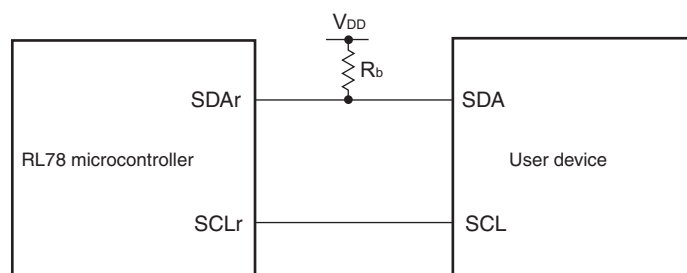
**Simplified I^{2}C mode serial transfer timing (during communication at same potential)**
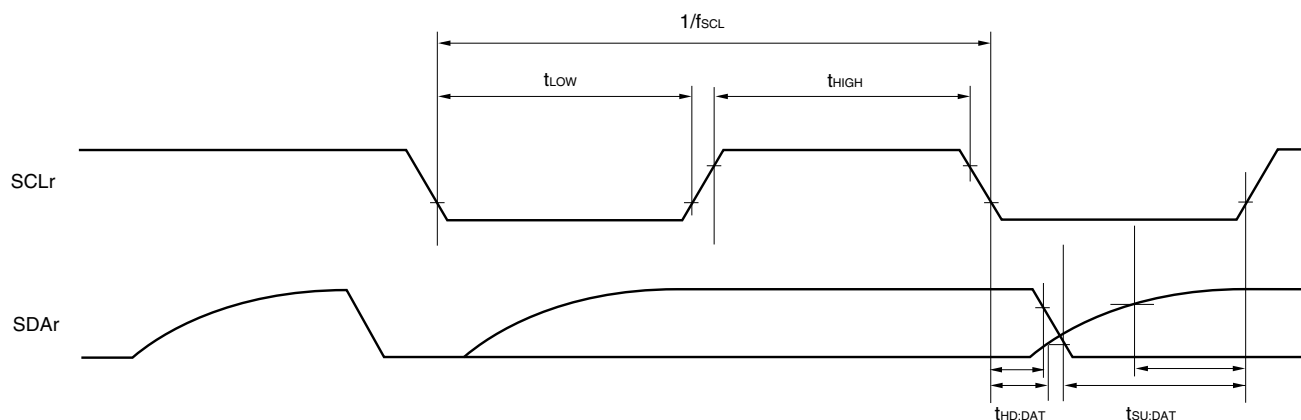
Remarks **1.** R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

    2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),

        h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

    3. f$_{MCK}$: Serial array unit operation clock frequency

        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m

        = 0, 1),

        n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
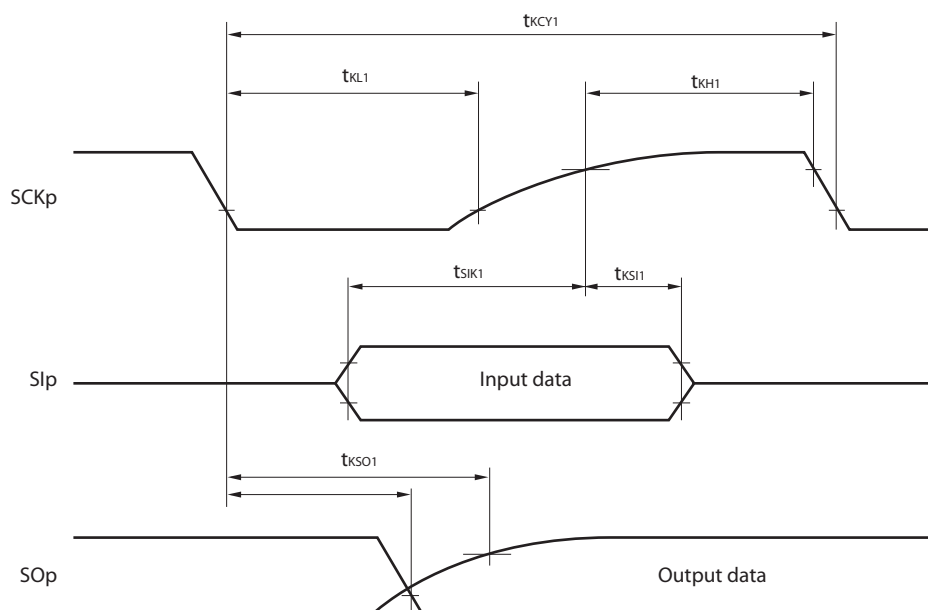
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
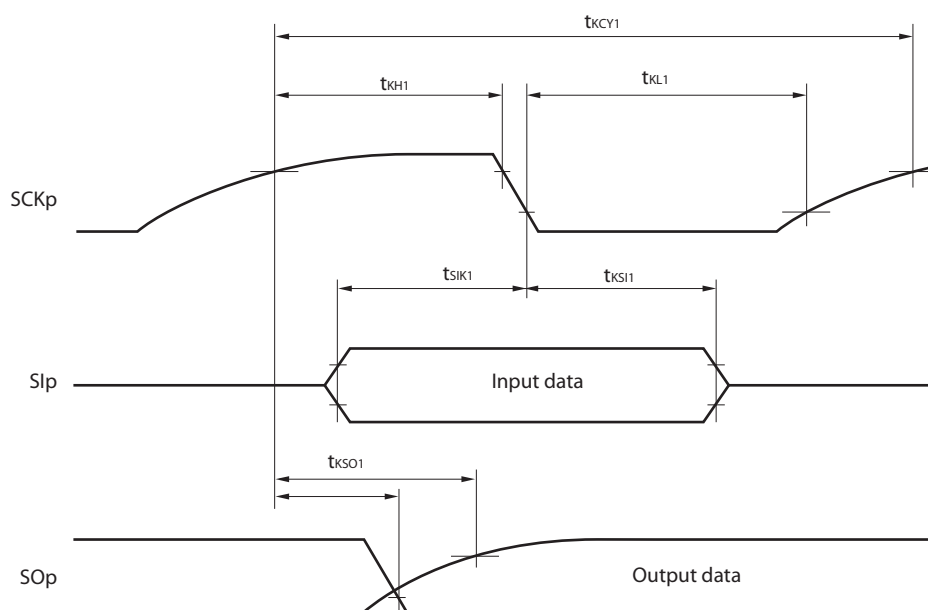
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

　　2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	610		610		610		ns

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI14	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI26	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		–

(1) When reference voltage (+)= AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	µs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	µs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	µs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.50	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.50	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±5.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$[Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$[Note 5]		V

(**Notes** are listed on the next page.)

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

   2. During HALT instruction execution by flash memory.

   3. When high-speed on-chip oscillator and subsystem clock are stopped.

   4. When high-speed system clock and subsystem clock are stopped.

   5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

   6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

   7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

   2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

   8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

   2. f$_{IH}$: High-speed on-chip oscillator clock frequency

   3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

   4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +105°C, 2.4 V $\le$ EV$_{DD0}$ = EV$_{DD1}$ $\le$ V$_{DD}$ $\le$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V $\le$ EV$_{DD0}$ $\le$ 5.5 V, 2.7 V $\le$ V$_b$ $\le$ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.6 **Note 2**	Mbps
			2.7 V $\le$ EV$_{DD0}$ < 4.0 V, 2.3 V $\le$ V$_b$ $\le$ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 **Note 4**	Mbps
			2.4 V $\le$ EV$_{DD0}$ < 3.3 V, 1.6 V $\le$ V$_b$ $\le$ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 **Note 6**	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V $\le$ EV$_{DD0}$ $\le$ 5.5 V and 2.7 V $\le$ V$_b$ $\le$ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\le$ EV$_{DD0}$ < 4.0 V and 2.4 V $\le$ V$_b$ $\le$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 24		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 36		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]		t$_{KCY2}$/2 − 100		ns
SIp setup time (to SCKp↑) [Note 2]	t$_{SIK2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		100 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		100 [Note 1]	kHz
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	4600		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	4600		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	620		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	500		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	2700		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	2400		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1830		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

3.5.2 Serial interface IICA

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f$_{CLK}$ ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>　　　2. The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode:　C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
Fast mode:　　　C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
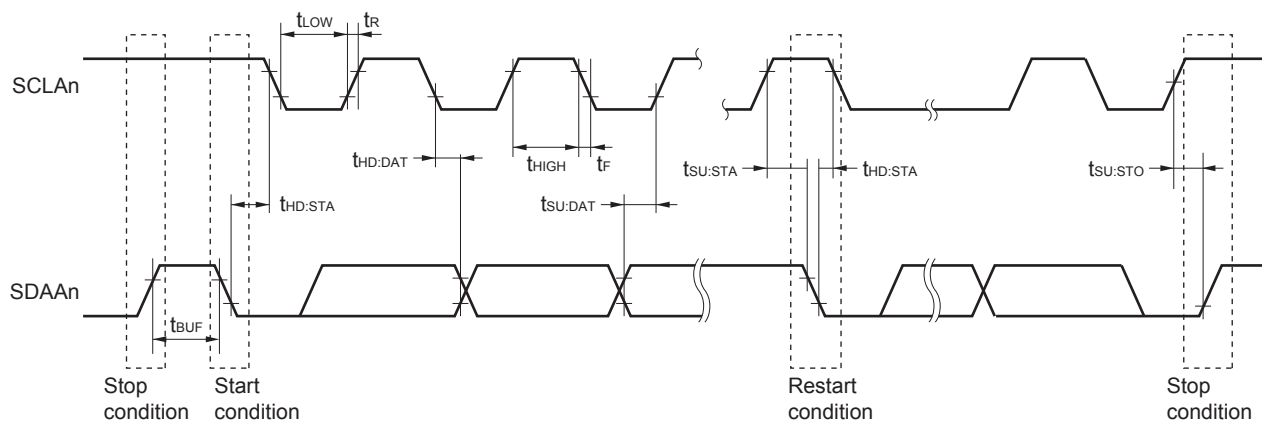
Remark　n = 0, 1

3.6.5 Power supply voltage rising slope characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution   **Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

3.7 RAM Data Retention Characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.44[Note]		5.5	V

Note   This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.
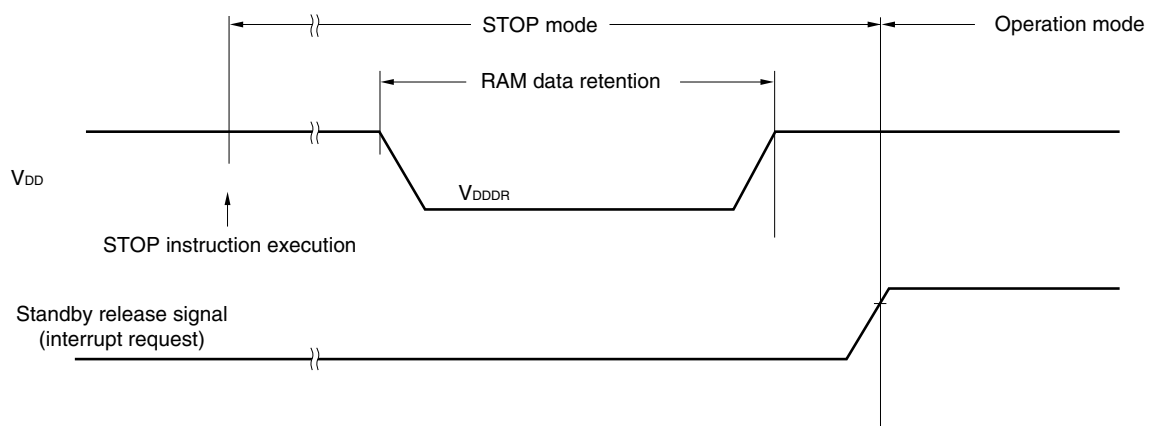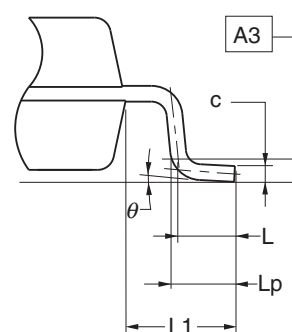
4.14 128-pin Products

R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB
R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB
R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92
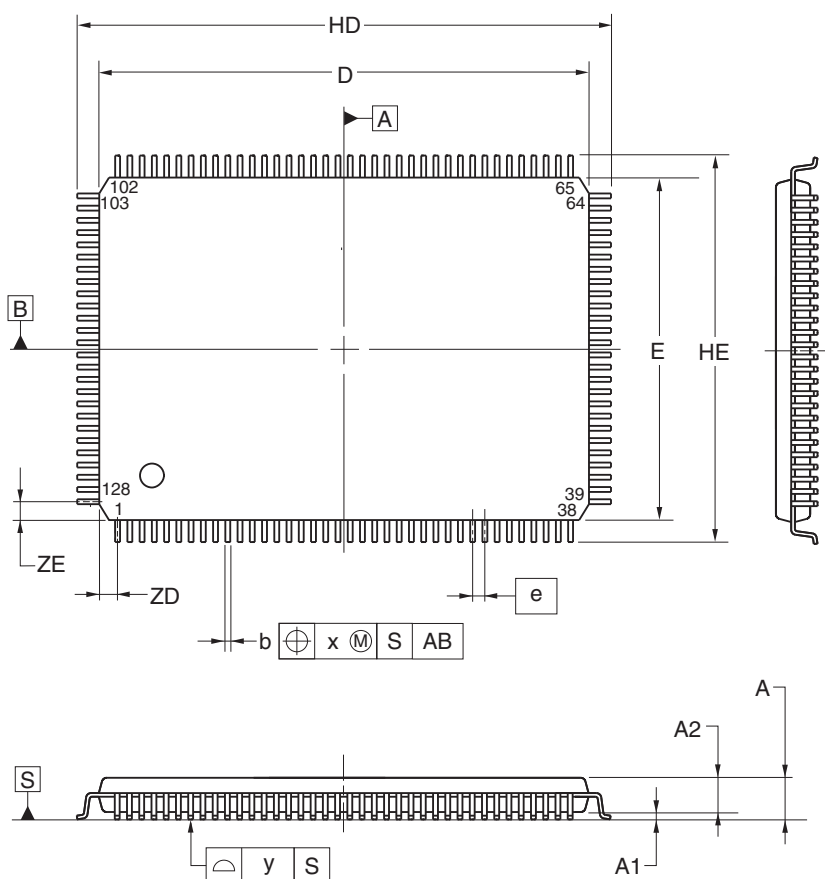
detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

Rev.	Date	Description	
		Page	**Summary**
1.00	Feb 29, 2012	-	First Edition issued
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.
		59, 63, 67	Descriptions of Note 8 in a table corrected.
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.
3.00	Aug 02, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4 to 15	Modification of Table 1-1. List of Ordering Part Numbers, note, and caution
		16 to 32	Modification of package type in 1.3.1 to 1.3.14
		33	Modification of description in 1.4 Pin Identification
		48, 50, 52	Modification of caution, table, and note in 1.6 Outline of Functions
		55	Modification of description in table of Absolute Maximum Ratings (T$_A$ = 25°C)
		57	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics
		57	Modification of table in 2.2.2 On-chip oscillator characteristics
		58	Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics
		59	Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics
		63	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		64	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		65	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		66	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		68	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		70	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		72	Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		74	Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		75	Modification of (4) Peripheral Functions (Common to all products)
		77	Modification of table in 2.4 AC Characteristics
		78, 79	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		80	Modification of figures of AC Timing Test Points and External System Clock Timing

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction.   If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction.   Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction.   CMOS devices behave differently than Bipolar or NMOS devices.   Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry.   Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin.   All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation.   Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate.   When it is dry, a humidifier should be used.   It is recommended to avoid using insulators that easily build up static electricity.   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material.   All test and measurement tools including work benches and floors should be grounded.   The operator should be grounded using a wrist strap.   Semiconductor devices must not be touched with bare hands.   Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device.   Immediately after the power source is turned ON, devices with reset functions have not yet been initialized.   Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers.   A device is not initialized until the reset signal is received.   A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply.   When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply.   Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.   The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE :   Do not input signals or an I/O pull-up power supply while the device is not powered.   The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.   Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.