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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101pgdfb-30

1.3.4 30-pin products
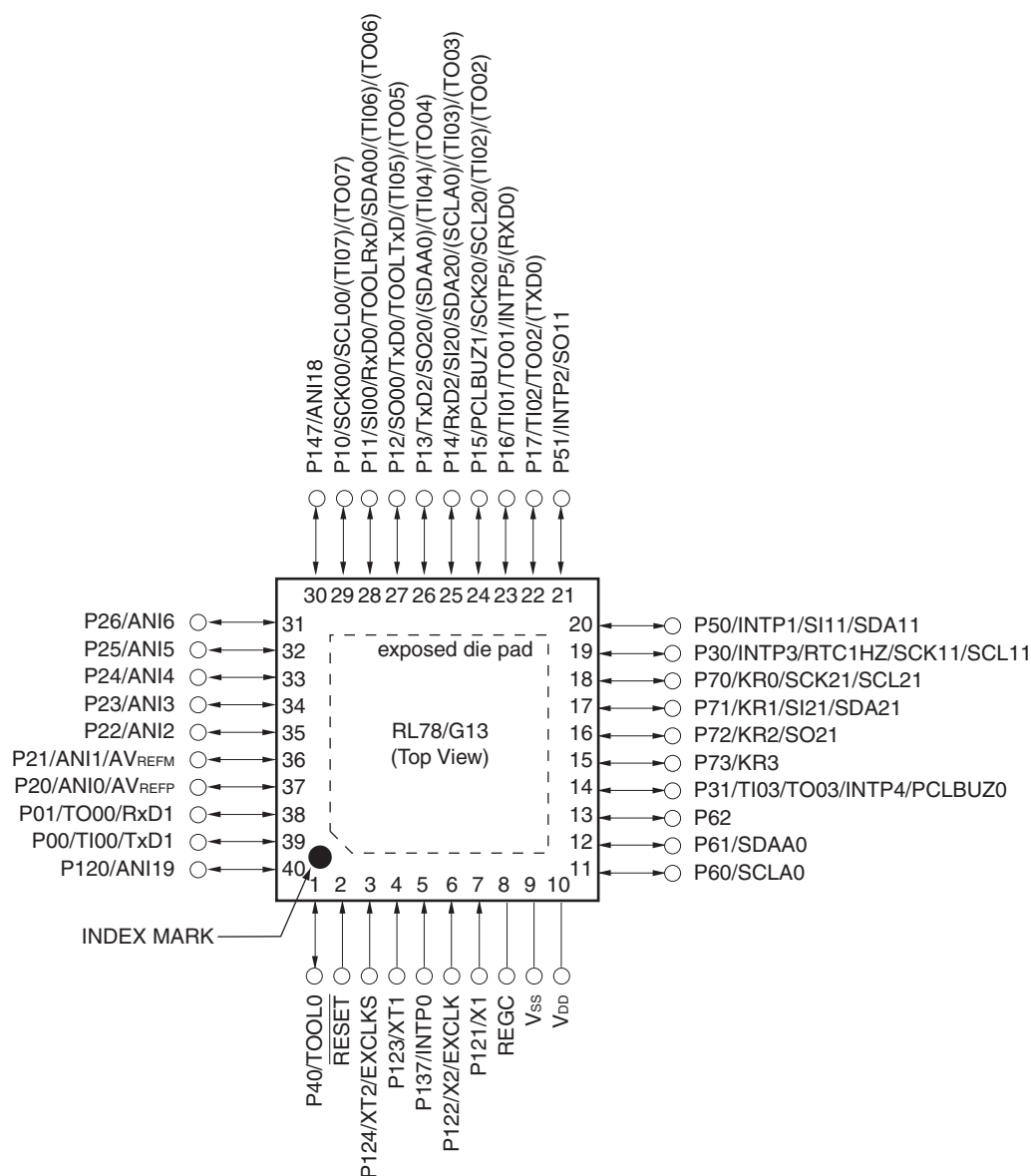
- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)
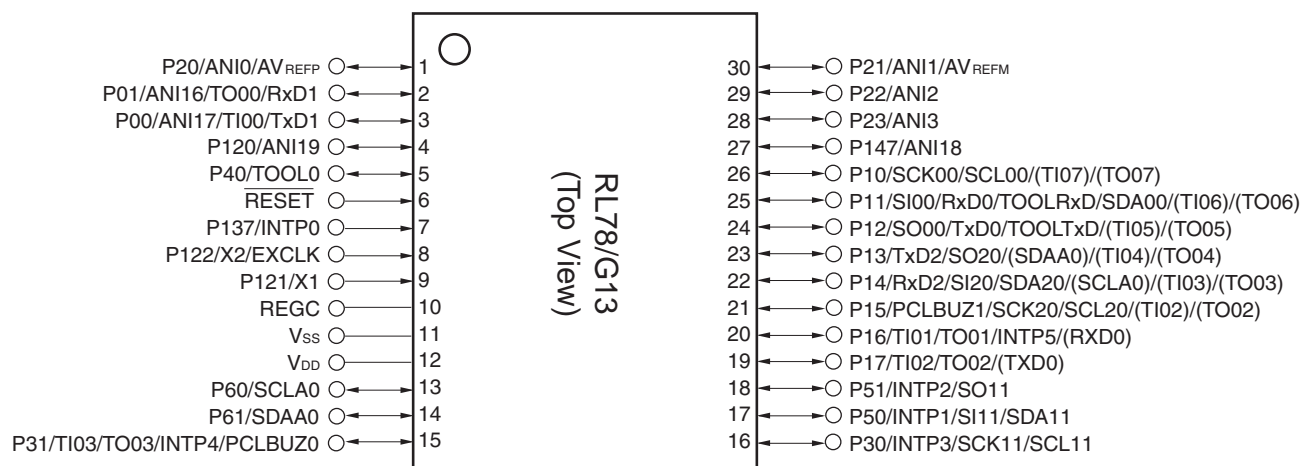
Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
  2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)

Top pins (left to right, pins 30–21):
- P147/ANI18
- P10/SCK00/SCL00/(TI07)/(TO07)
- P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- P16/TI01/TO01/INTP5/(RXD0)
- P17/TI02/TO02/(TXD0)
- P51/INTP2/SO11

Left side pins:
- P26/ANI6 — 31
- P25/ANI5 — 32
- P24/ANI4 — 33
- P23/ANI3 — 34
- P22/ANI2 — 35
- P21/ANI1/AV$_{REFM}$ — 36
- P20/ANI0/AV$_{REFP}$ — 37
- P01/TO00/RxD1 — 38
- P00/TI00/TxD1 — 39
- P120/ANI19 — 40

Right side pins:
- 20 — P50/INTP1/SI11/SDA11
- 19 — P30/INTP3/RTC1HZ/SCK11/SCL11
- 18 — P70/KR0/SCK21/SCL21
- 17 — P71/KR1/SI21/SDA21
- 16 — P72/KR2/SO21
- 15 — P73/KR3
- 14 — P31/TI03/TO03/INTP4/PCLBUZ0
- 13 — P62
- 12 — P61/SDAA0
- 11 — P60/SCLA0

exposed die pad

RL78/G13
(Top View)

INDEX MARK

Bottom pins (left to right, pins 1–10):
- P40/TOOL0
- RESET
- P124/XT2/EXCLKS
- P123/XT1
- P137/INTP0
- P122/X2/EXCLK
- P121/X1
- REGC
- V$_{SS}$
- V$_{DD}$

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to Vss.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3　Operation as multiple PWM output function** in the RL78/G13 User's Manual).

3. When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
	I²C bus	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access									
Power-on-reset circuit		• Power-on-reset:　　1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)									
Voltage detector		• Rising edge :　　　1.67 V to 4.06 V (14 stages) • Falling edge :　　　1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)									
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)									

<R>

Note　The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                                      2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

    LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

    LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @1 MHz to 32 MHz

   2.4 V ≤ V$_{DD}$ ≤ 5.5 V @1 MHz to 16 MHz

   LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V @1 MHz to 8 MHz

   LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V @1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
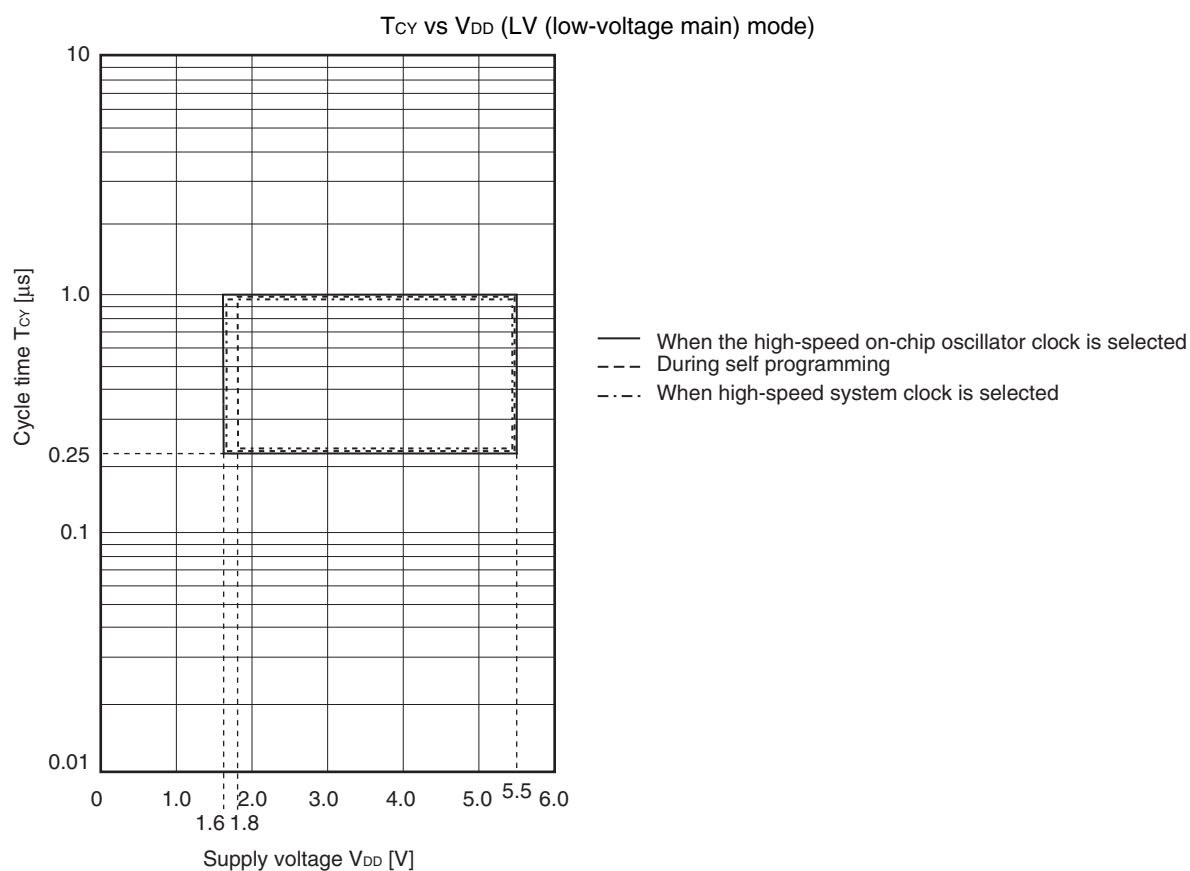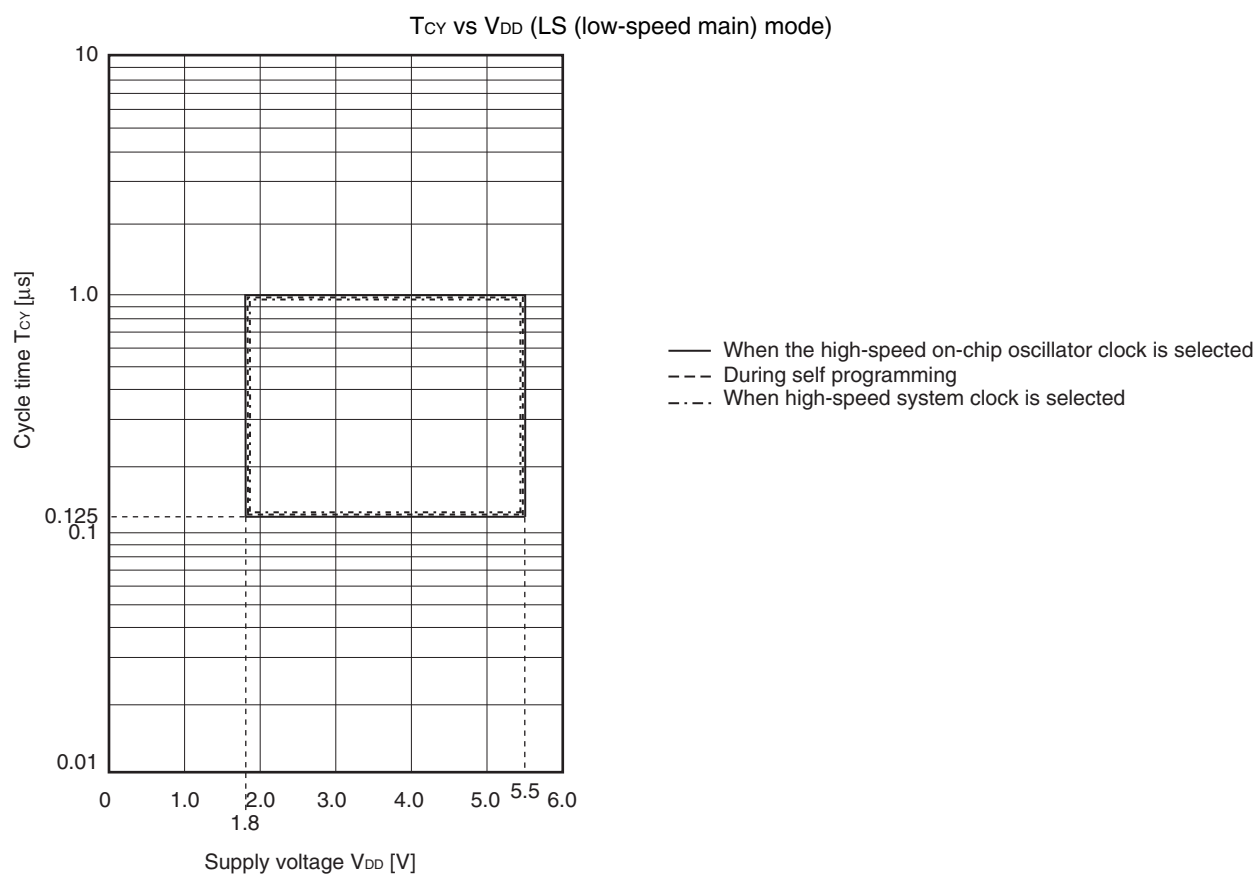
Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

2.4 AC Characteristics

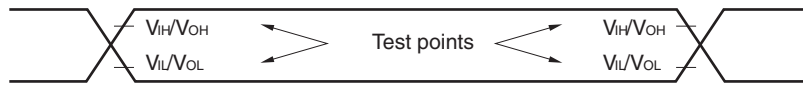**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	µs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	µs
			LV (low-voltage main) mode	1.6 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	µs
		Subsystem clock (f$_{SUB}$) operation		1.8 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	µs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	µs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	µs
			LV (low-voltage main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	µs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V$_{DD}$ < 1.8 V			1.0		4.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
		1.8 V ≤ V$_{DD}$ < 2.4 V			60			ns
		1.6 V ≤ V$_{DD}$ < 1.8 V			120			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			µs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns[Note]
TO00 to TO07, TO10 to TO17 output frequency	f$_{TO}$	HS (high-speed main) mode		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
				2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
				2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0		1.6 V ≤ V$_{DD}$ ≤ 5.5 V	1			µs
		INTP1 to INTP11		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V	1			µs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V	250			ns
				1.6 V ≤ EV$_{DD0}$ < 1.8 V	1			µs
RESET low-level width	t$_{RSL}$				10			µs

(**Note** and **Remark** are listed on the next page.)

T_{CY} vs V_{DD} (LS (low-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-.-. When high-speed system clock is selected

T_{CY} vs V_{DD} (LV (low-voltage main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-.-. When high-speed system clock is selected

2.5 Peripheral Functions Characteristics

AC Timing Test Points

2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note 1]		2.4 V≤ EV$_{DD0}$ ≤ 5.5 V			f$_{MCK}$/6 [Note 2]		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 3]		5.3		1.3		0.6	Mbps
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			f$_{MCK}$/6 [Note 2]		f$_{MCK}$/6		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 3]		5.3		1.3		0.6	Mbps
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V			f$_{MCK}$/6 [Note 2]		f$_{MCK}$/6 [Note 2]		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 3]		5.3		1.3		0.6	Mbps
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—			f$_{MCK}$/6 [Note 2]		f$_{MCK}$/6	bps
			Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note 3]	—			1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

    2. The following conditions are required for low voltage interface when EV$_{DD0}$ < V$_{DD}$.

        2.4 V ≤ EV$_{DD0}$ < 2.7 V : MAX. 2.6 Mbps

        1.8 V ≤ EV$_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

        1.6 V ≤ EV$_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

    3. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

        HS (high-speed main) mode: 32 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

                                 16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

        LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

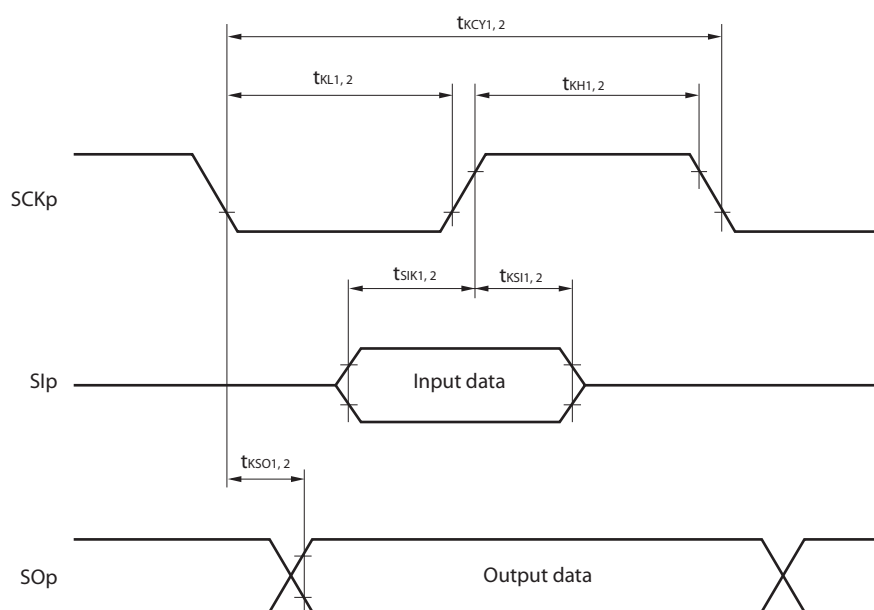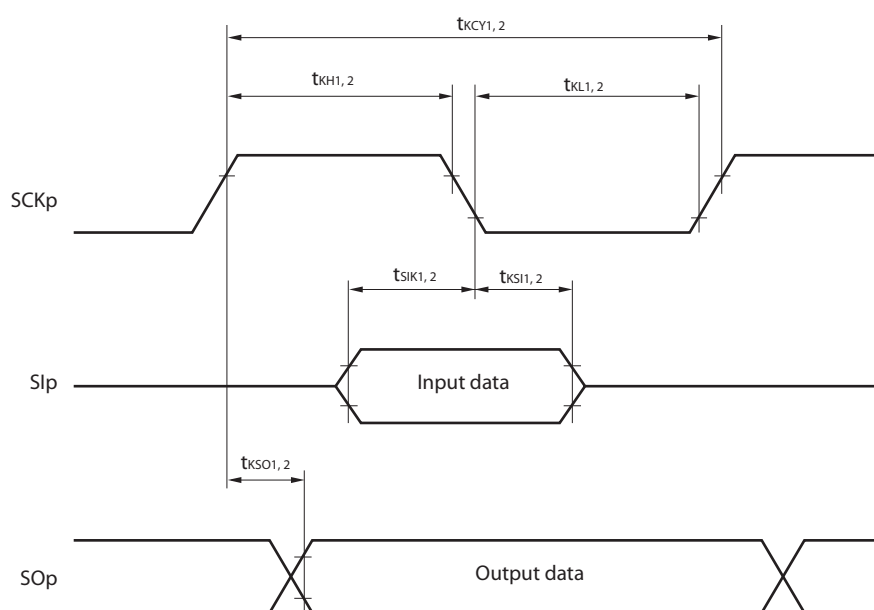   LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution   **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1.   p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

         g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2.   f$_{MCK}$: Serial array unit operation clock frequency

         (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

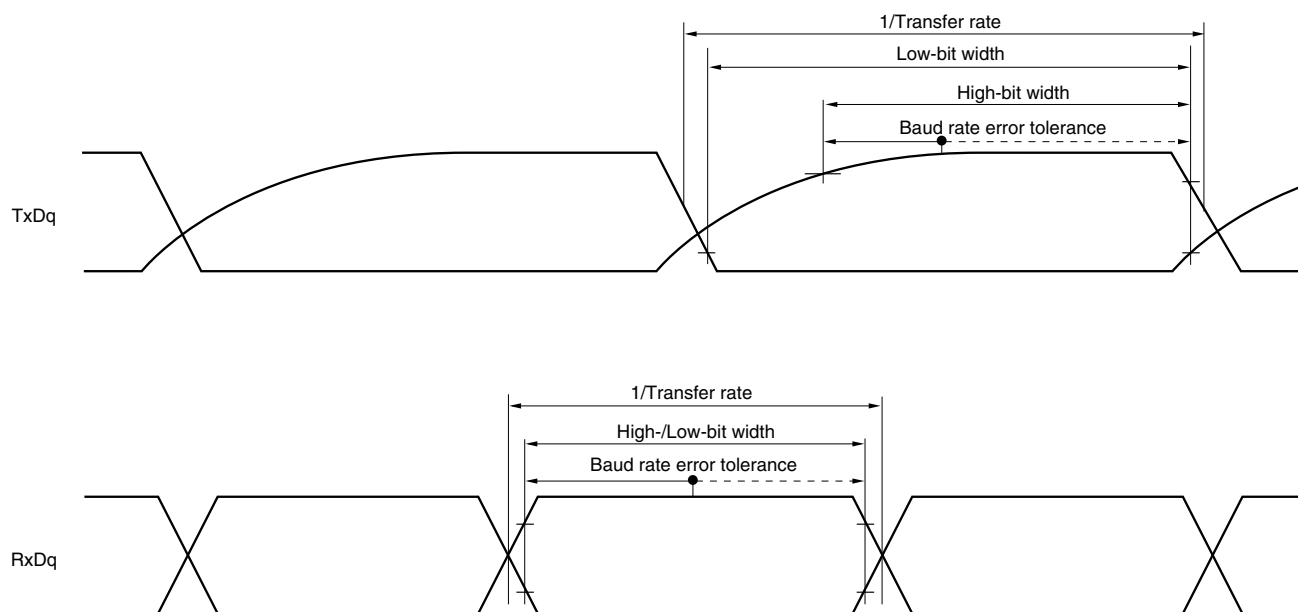   n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

     (T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at same potential)
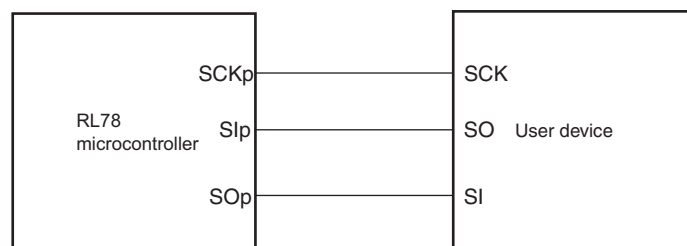
RL78 microcontroller — SCKp → SCK
SIp → SO   User device
SOp → SI

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

$t_{KCY1, 2}$

$t_{KL1, 2}$ $t_{KH1, 2}$

SCKp

$t_{SIK1, 2}$ $t_{KSI1, 2}$

SIp   Input data

$t_{KSO1, 2}$

SOp   Output data

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

$t_{KCY1, 2}$

$t_{KH1, 2}$ $t_{KL1, 2}$

SCKp

$t_{SIK1, 2}$ $t_{KSI1, 2}$

SIp   Input data

$t_{KSO1, 2}$

SOp   Output data

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
       2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

UART mode bit width (during communication at different potential) (reference)

1/Transfer rate

Low-bit width

High-bit width

Baud rate error tolerance

TxDq

1/Transfer rate

High-/Low-bit width

Baud rate error tolerance

RxDq

Remarks 1. R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection

register (PIOR) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T$_A$ = −40 to +85°C, 2.7 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200		1150		1150		ns
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t$_{KH1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		ns
SCKp low-level width	t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130		130	ns

(**Notes, Caution,** and **Remarks** are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

(T$_A$ = –40 to +85°C, 2.7 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 2]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) [Note 2]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output [Note 2]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1. R$_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)
 3. f$_{MCK}$: Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) [Note 1]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		25		25		25	ns

Notes   **1.**   When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2.   Use it with EV$_{DD0}$ ≥ V$_b$.

Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	610		610		610		ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)

(TA = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V $^{Note 2}$, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		1/f$_{MCK}$ + 190 $^{Note 3}$		kHz
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V $^{Note 2}$, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Use it with EV$_{DD0}$ ≥ V$_b$.

3. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(3) I²C fast mode plus

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode plus: f$_{CLK}$ ≥ 10 MHz	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	1000	—		—		kHz
Setup time of restart condition	t$_{SU:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Hold time[Note 1]	t$_{HD:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		50		—		—		μs
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	0.45	—		—		μs
Setup time of stop condition	t$_{SU:STO}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μs
Bus-free time	t$_{BUF}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C$_b$ = 120 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
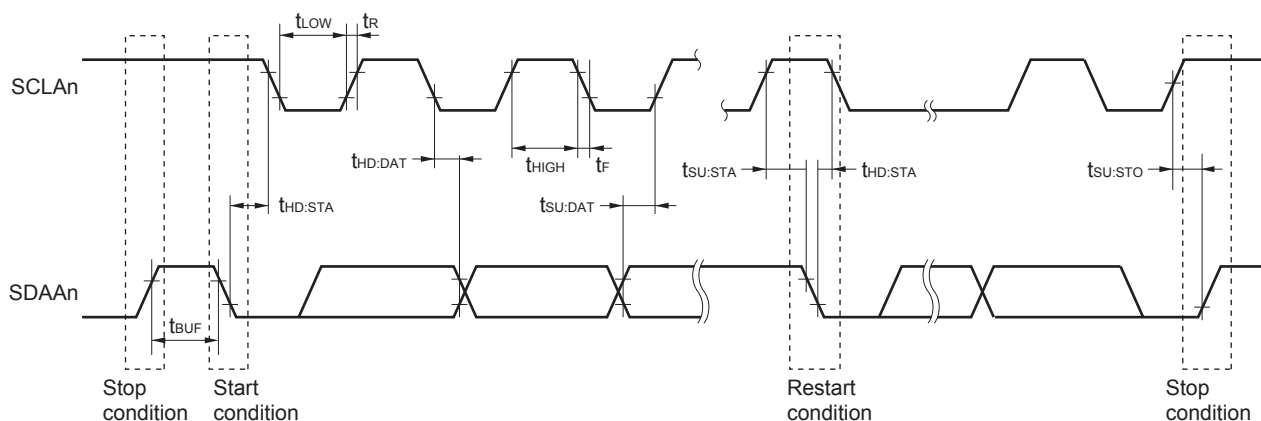
Remark n = 0, 1

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
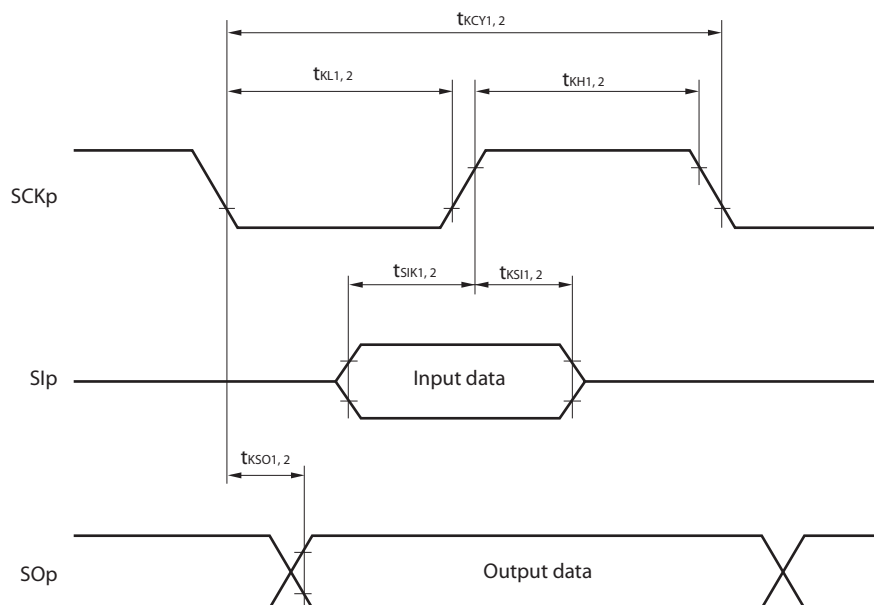
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
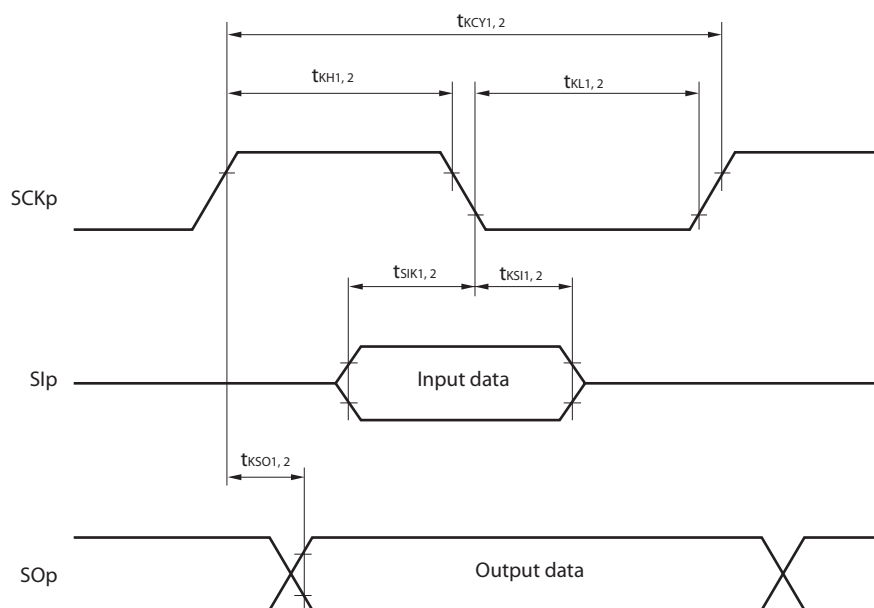
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(4) During communication at same potential (simplified I^{2}C mode)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

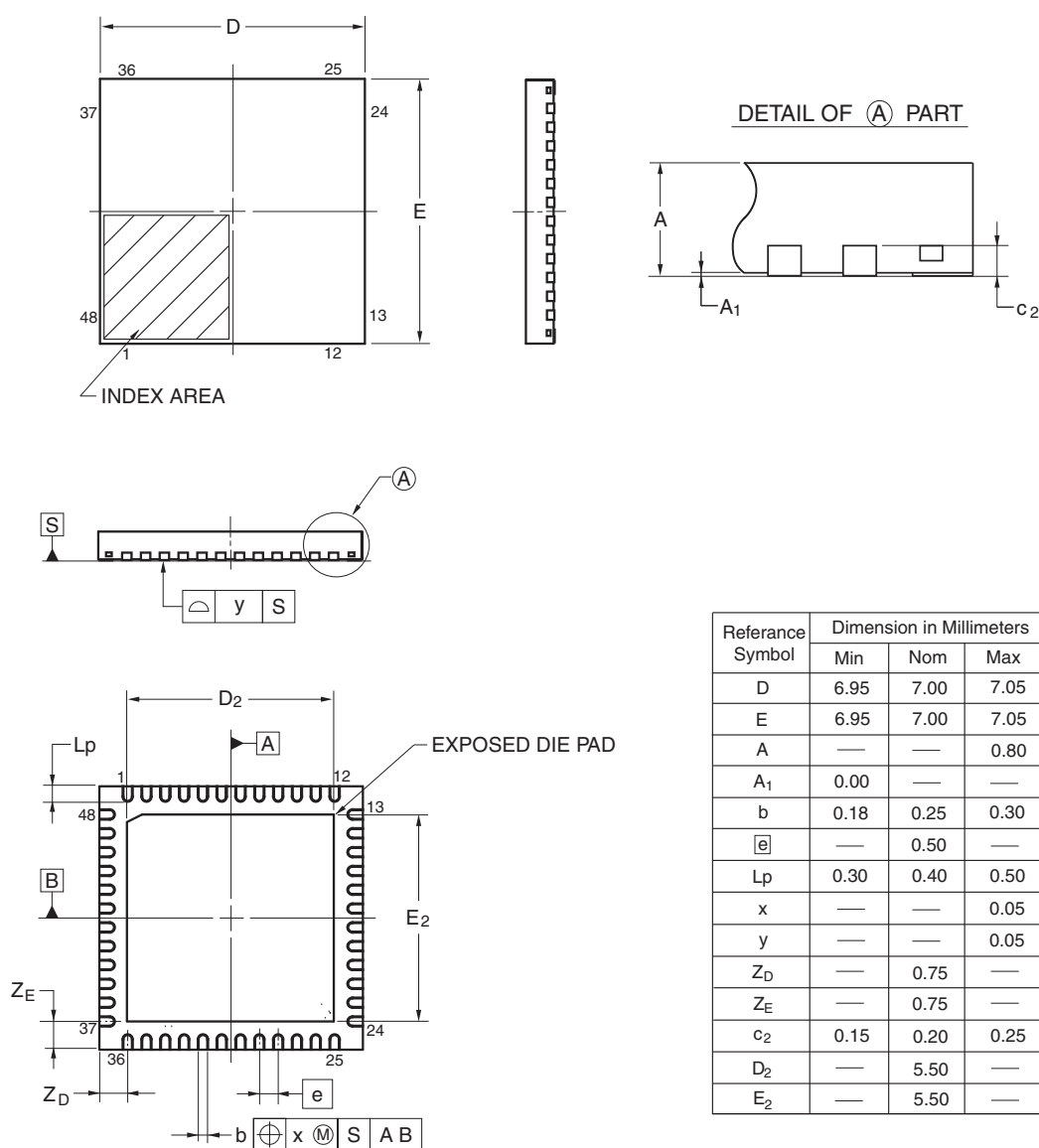| Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 ^{Note1}	kHz
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		100 ^{Note1}	kHz
Hold time when SCLr = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 220 ^{Note2}		ns
		2.4 V ≤ EV$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 580 ^{Note2}		ns
Data hold time (transmission)	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	―	―	0.80
A_1	0.00	―	―
b	0.18	0.25	0.30
e	―	0.50	―
Lp	0.30	0.40	0.50
x	―	―	0.05
y	―	―	0.05
Z_D	―	0.75	―
Z_E	―	0.75	―
c_2	0.15	0.20	0.25
D_2	―	5.50	―
E_2	―	5.50	―