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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

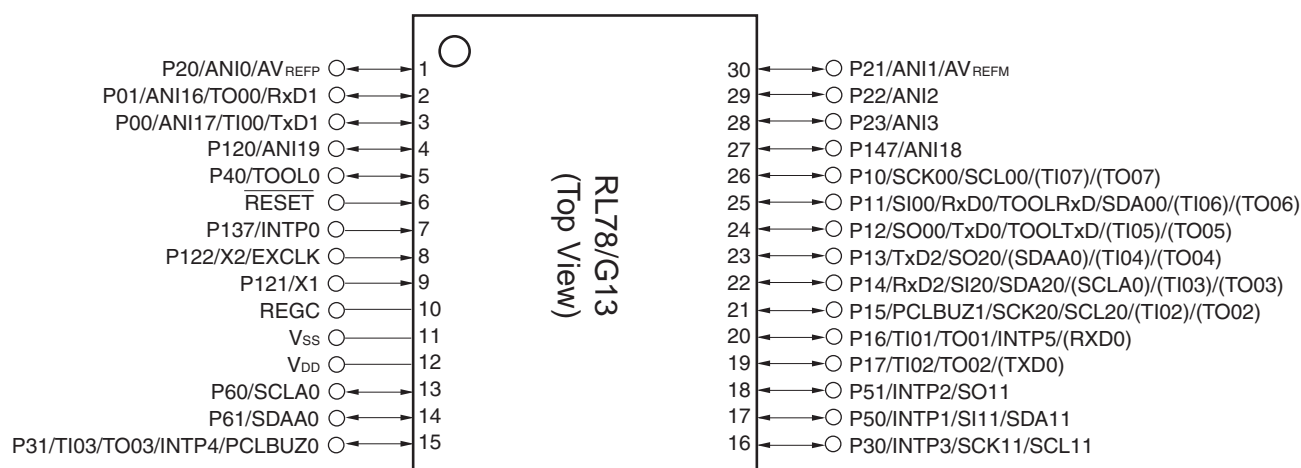
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	110
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 26x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101sjafb-v0

1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



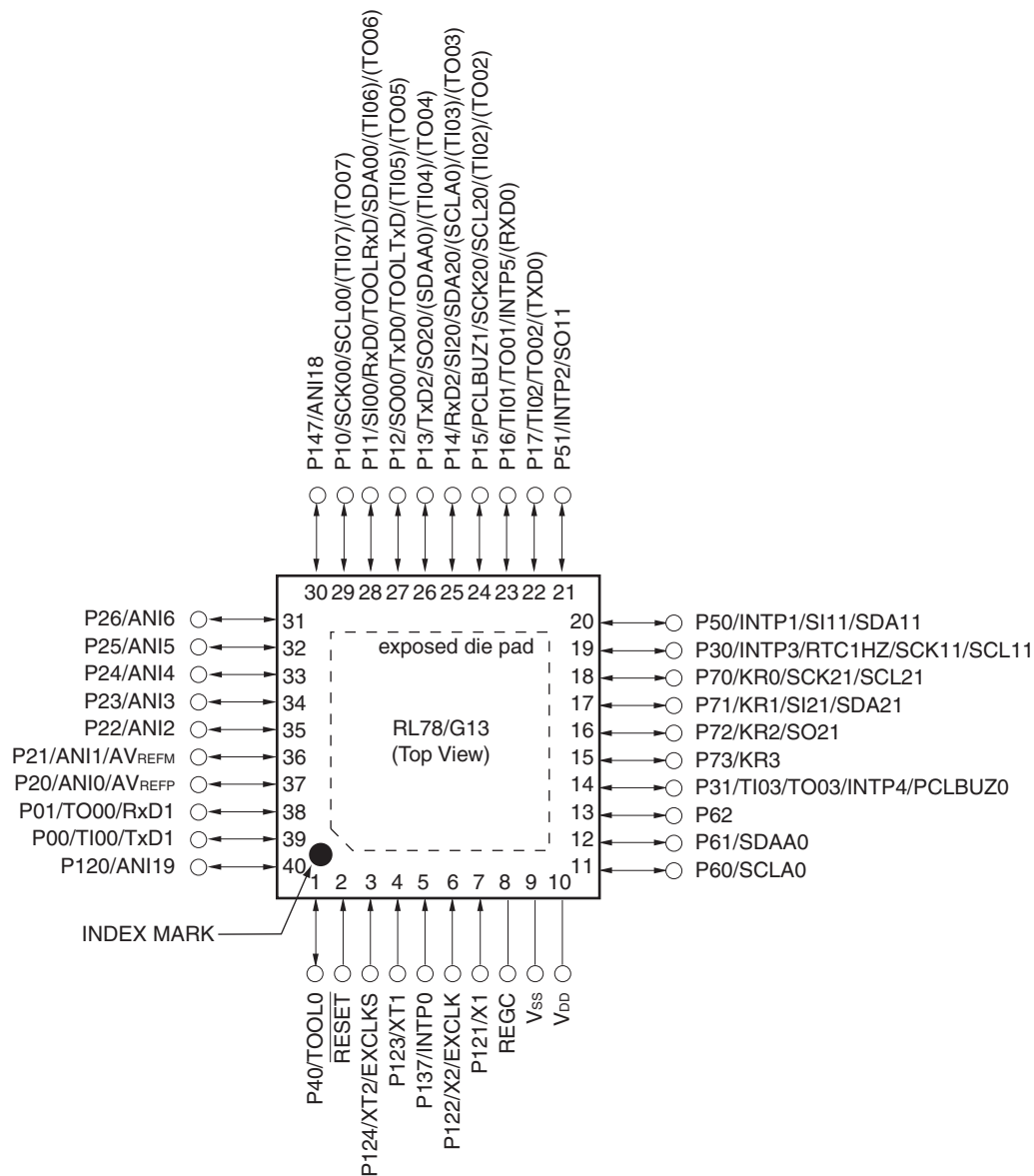
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



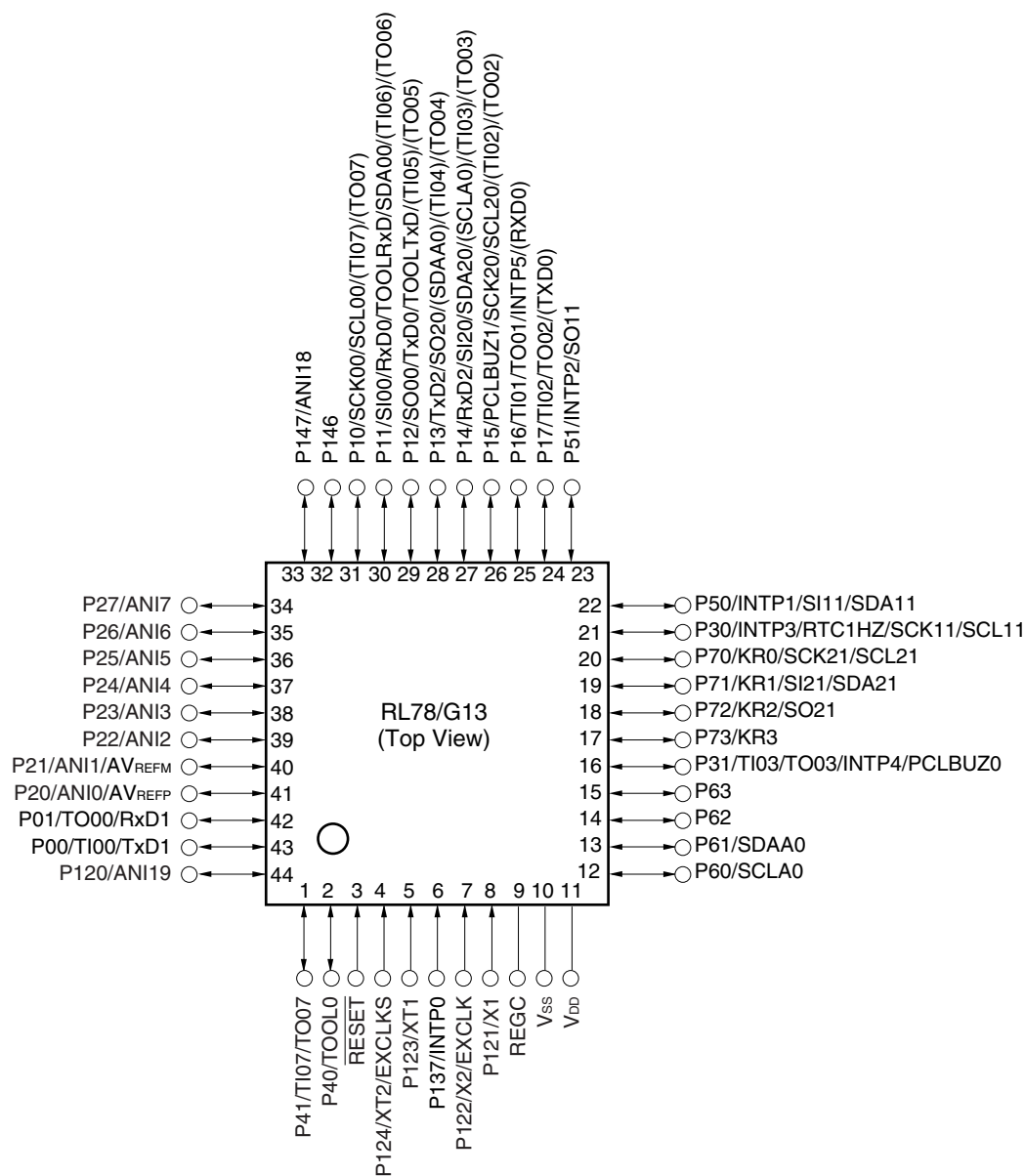
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to V_{ss}.

1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI26	-0.3 to EV _{DD0} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-10.0 ^{Note 2}	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-55.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-10.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-5.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-80.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-19.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-10.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-5.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-135.0 ^{Note 4}	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		-1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is -100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.54	1.63	mA	
					V _{DD} = 3.0 V		0.54	1.63	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.28	mA	
					V _{DD} = 3.0 V		0.44	1.28	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.40	1.00	mA	
					V _{DD} = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		260	530	μA
						V _{DD} = 2.0 V		260	530	μA
				LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		420	640	μA
						V _{DD} = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		95	330	μA
						Resonator connection		145	380	μA
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V		Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} , T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +50°C	Square wave input		0.37	1.17	μA	
					Resonator connection		0.56	1.36	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +70°C	Square wave input		0.53	1.97	μA	
					Resonator connection		0.72	2.16	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +85°C	Square wave input		0.82	3.37	μA	
					Resonator connection		1.01	3.56	μA	
	I _{DD3} Note 6	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.30	1.10	μA
			T _A = +70°C					0.46	1.90	μA
			T _A = +85°C					0.75	3.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)**

Parameter	Symbol				Conditions	MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.62	1.89	mA	
					V _{DD} = 3.0 V		0.62	1.89	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.50	1.48	mA	
					V _{DD} = 3.0 V		0.50	1.48	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.12	mA	
					V _{DD} = 3.0 V		0.44	1.12	mA	
			LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		290	620	μA	
					V _{DD} = 2.0 V		290	620	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		460	700	μA	
					V _{DD} = 2.0 V		460	700	μA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
			LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		110	390	μA	
					Resonator connection		160	450	μA	
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		110	390	μA	
					Resonator connection		160	450	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.31	0.66	μA	
					Resonator connection		0.50	0.85	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.38	0.66	μA	
					Resonator connection		0.57	0.85	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.47	3.49	μA	
					Resonator connection		0.66	3.68	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.80	6.10	μA	
					Resonator connection		0.99	6.29	μA	
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		1.52	10.46	μA		
				Resonator connection		1.71	10.65	μA		
	I _{DD3} Note 6	STOP mode Note 8	T _A = −40°C					0.19	0.54	μA
			T _A = +25°C					0.26	0.54	μA
			T _A = +50°C					0.35	3.37	μA
			T _A = +70°C					0.68	5.98	μA
			T _A = +85°C					1.40	10.34	μA

(Notes and Remarks are listed on the next page.)

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125	1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25	1	μs
		Subsystem clock (f _{SUB}) operation		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3 μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125	1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125	1	μs
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25	1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V		1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V		1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V		1.0		4.0	MHz
	f _{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V		24			ns
		2.4 V ≤ V _{DD} < 2.7 V		30			ns
		1.8 V ≤ V _{DD} < 2.4 V		60			ns
		1.6 V ≤ V _{DD} < 1.8 V		120			ns
	t _{EXHS} , t _{EXLS}			13.7			μs
Ti00 to Ti07, Ti10 to Ti17 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}
TO00 to TO07, TO10 to TO17 output frequency	f _{TO}	HS (high-speed main) mode		4.0 V ≤ EV _{DD0} ≤ 5.5 V		16	MHz
				2.7 V ≤ EV _{DD0} < 4.0 V		8	MHz
				1.8 V ≤ EV _{DD0} < 2.7 V		4	MHz
				1.6 V ≤ EV _{DD0} < 1.8 V		2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV _{DD0} ≤ 5.5 V		4	MHz
				1.6 V ≤ EV _{DD0} < 1.8 V		2	MHz
		LV (low-voltage main) mode		1.6 V ≤ EV _{DD0} ≤ 5.5 V		2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode		4.0 V ≤ EV _{DD0} ≤ 5.5 V		16	MHz
				2.7 V ≤ EV _{DD0} < 4.0 V		8	MHz
				1.8 V ≤ EV _{DD0} < 2.7 V		4	MHz
				1.6 V ≤ EV _{DD0} < 1.8 V		2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV _{DD0} ≤ 5.5 V		4	MHz
				1.6 V ≤ EV _{DD0} < 1.8 V		2	MHz
		LV (low-voltage main) mode		1.8 V ≤ EV _{DD0} ≤ 5.5 V		4	MHz
				1.6 V ≤ EV _{DD0} < 1.8 V		2	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP11	1.6 V ≤ EV _{DD0} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR7	1.8 V ≤ EV _{DD0} ≤ 5.5 V	250			ns
			1.6 V ≤ EV _{DD0} < 1.8 V	1			μs
RESET low-level width	t _{RSL}			10			μs

(Note and Remark are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI14	Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI26	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V	1.2	±3.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}	1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57	95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{zs}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Full-scale error ^{Notes 1, 2}	E _{fs}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±2.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±1.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±2.0	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI14	0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 5}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	V_{OH2}	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	V_{OL2}	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	V_{OL3}	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

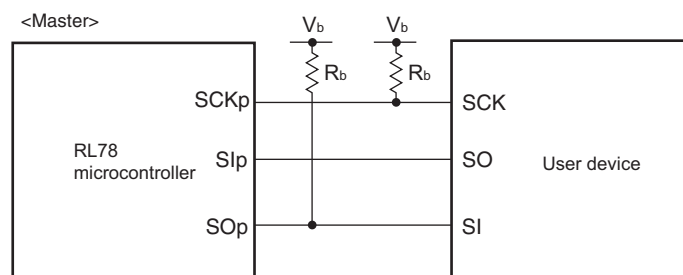
Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{DD0}		1	μA		
	I _{LH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}		1	μA		
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0}		−1	μA		
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R _U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

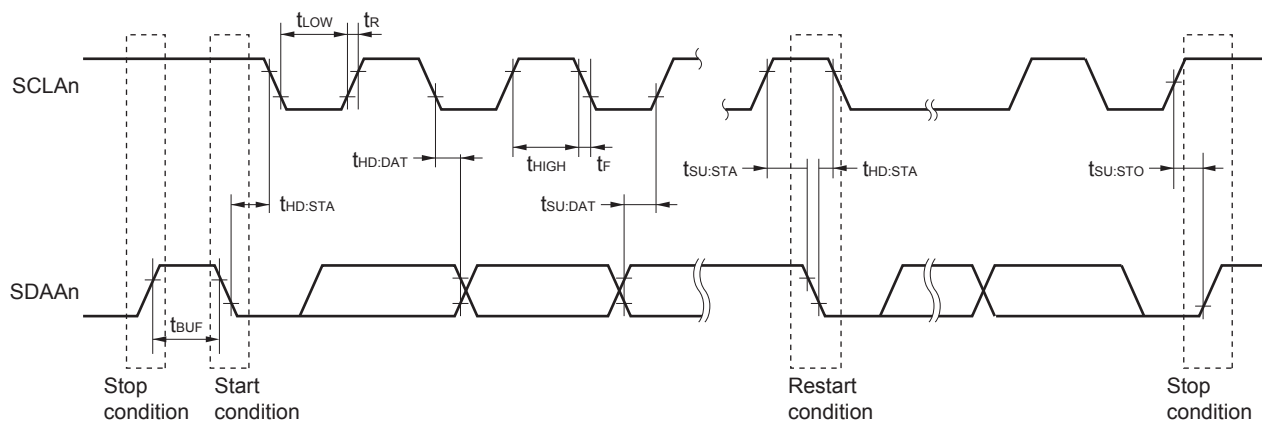
Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing

**Remark** n = 0, 1

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

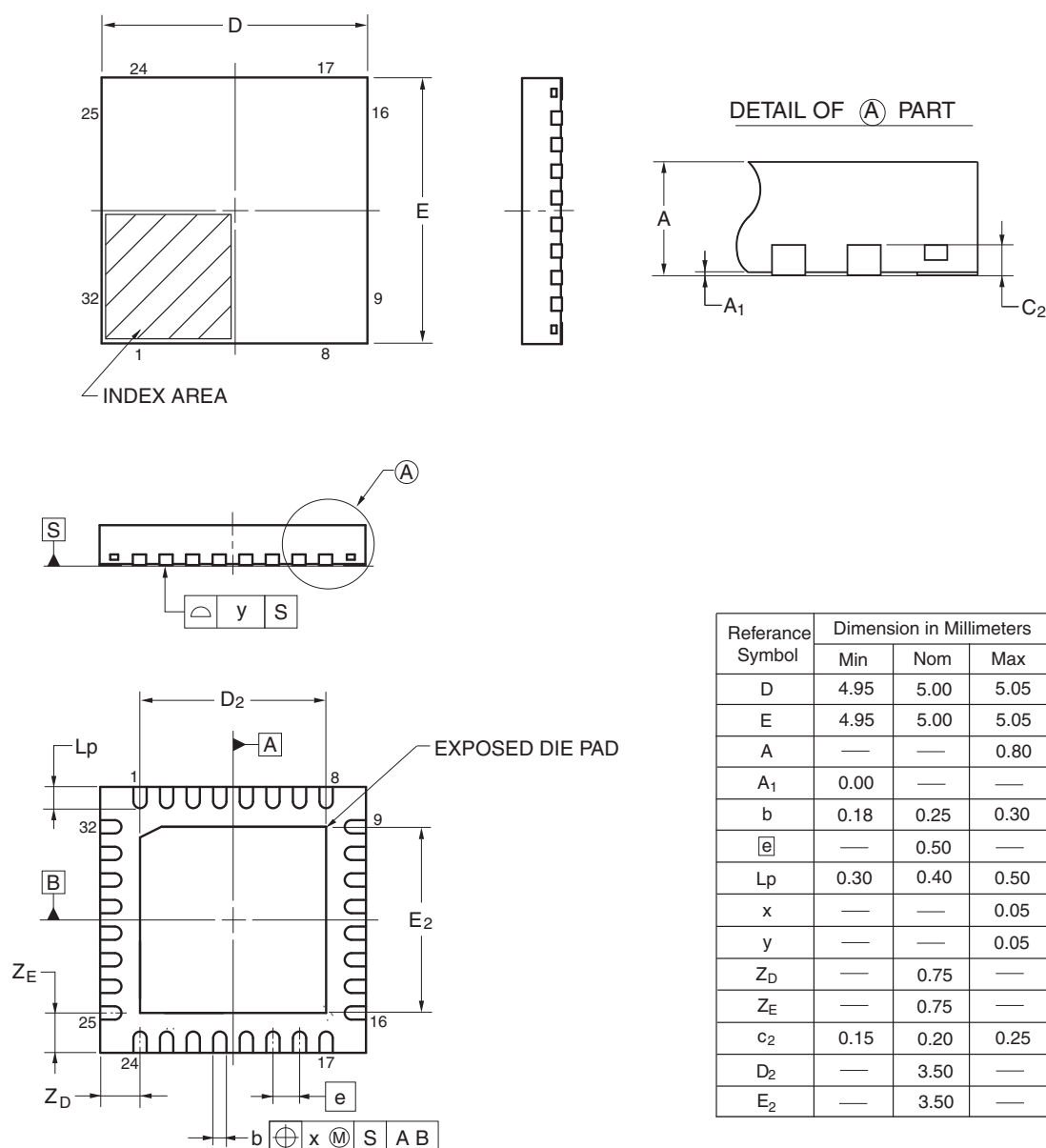
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

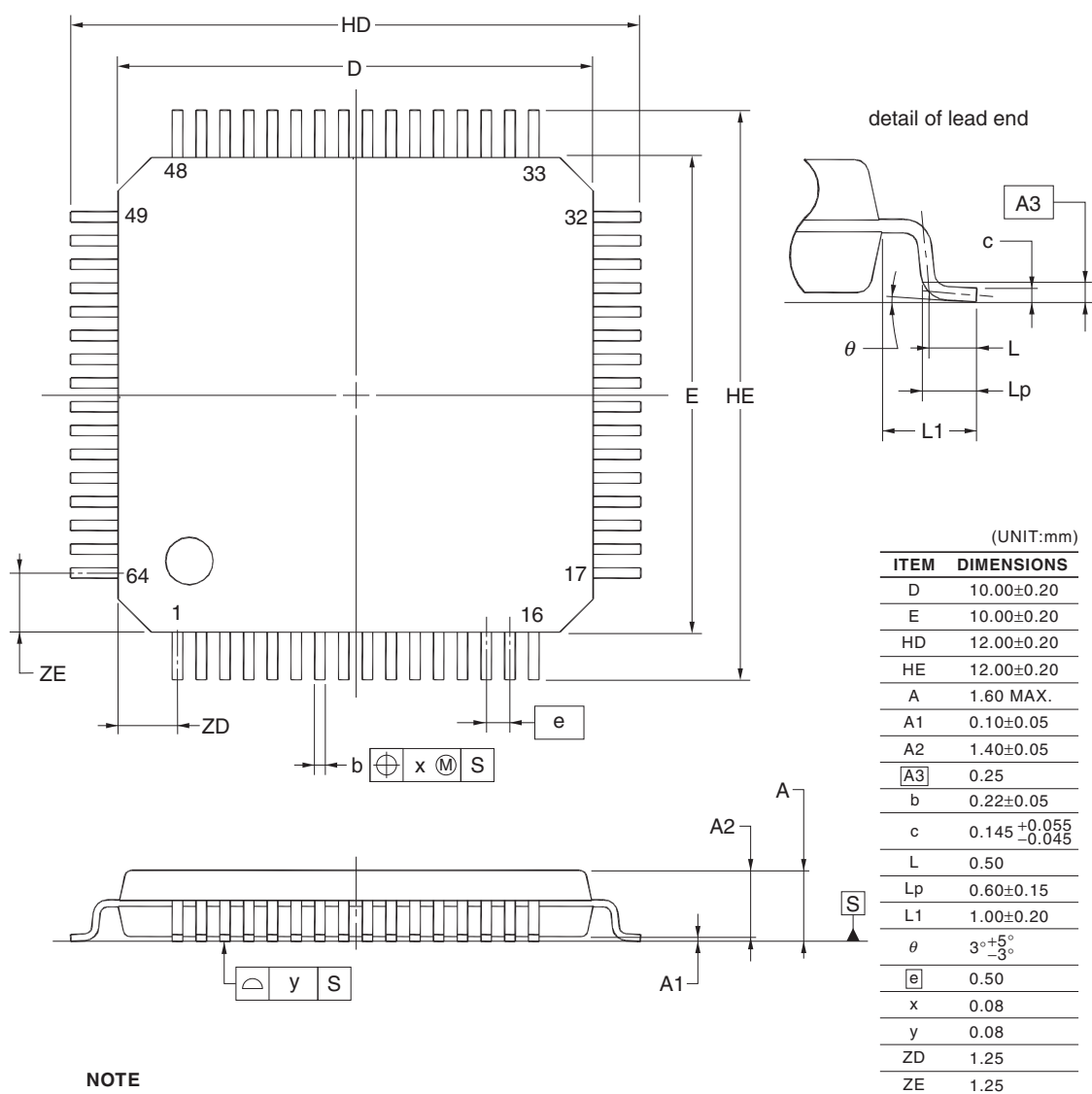
JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



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R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,
 R5F100LKAFB, R5F100LLAFB
 R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB,
 R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
 R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,
 R5F100LKDFB, R5F100LLDFB
 R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LDFB, R5F101LGDFB, R5F101LHDFB,
 R5F101LJDFB, R5F101LKDFB, R5F101LLDFB
 R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGF, R5F100LJGFB

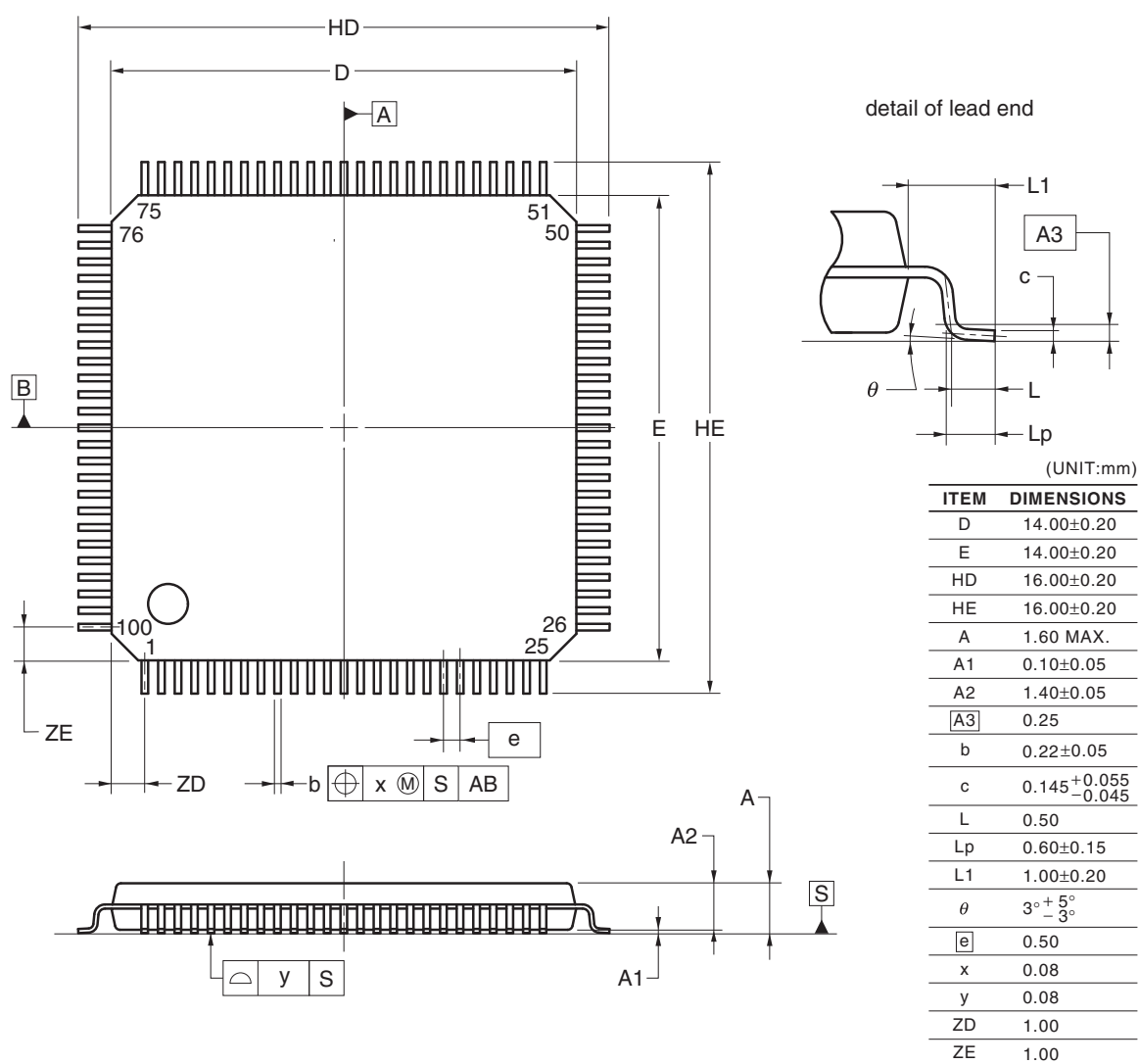
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDDB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
 R5F101PFDDB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I ² C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I ² C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		109	Addition of (1) I ² C standard mode
		111	Addition of (2) I ² C fast mode
		112	Addition of (3) I ² C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{\text{ACK}}$ corrected to ACK
			$\overline{\text{ACK}}$ corrected to ACK

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