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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	120MHz
Non-Volatile Memory	ROM (240kB)
On-Chip RAM	69kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56366ag120

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage*
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

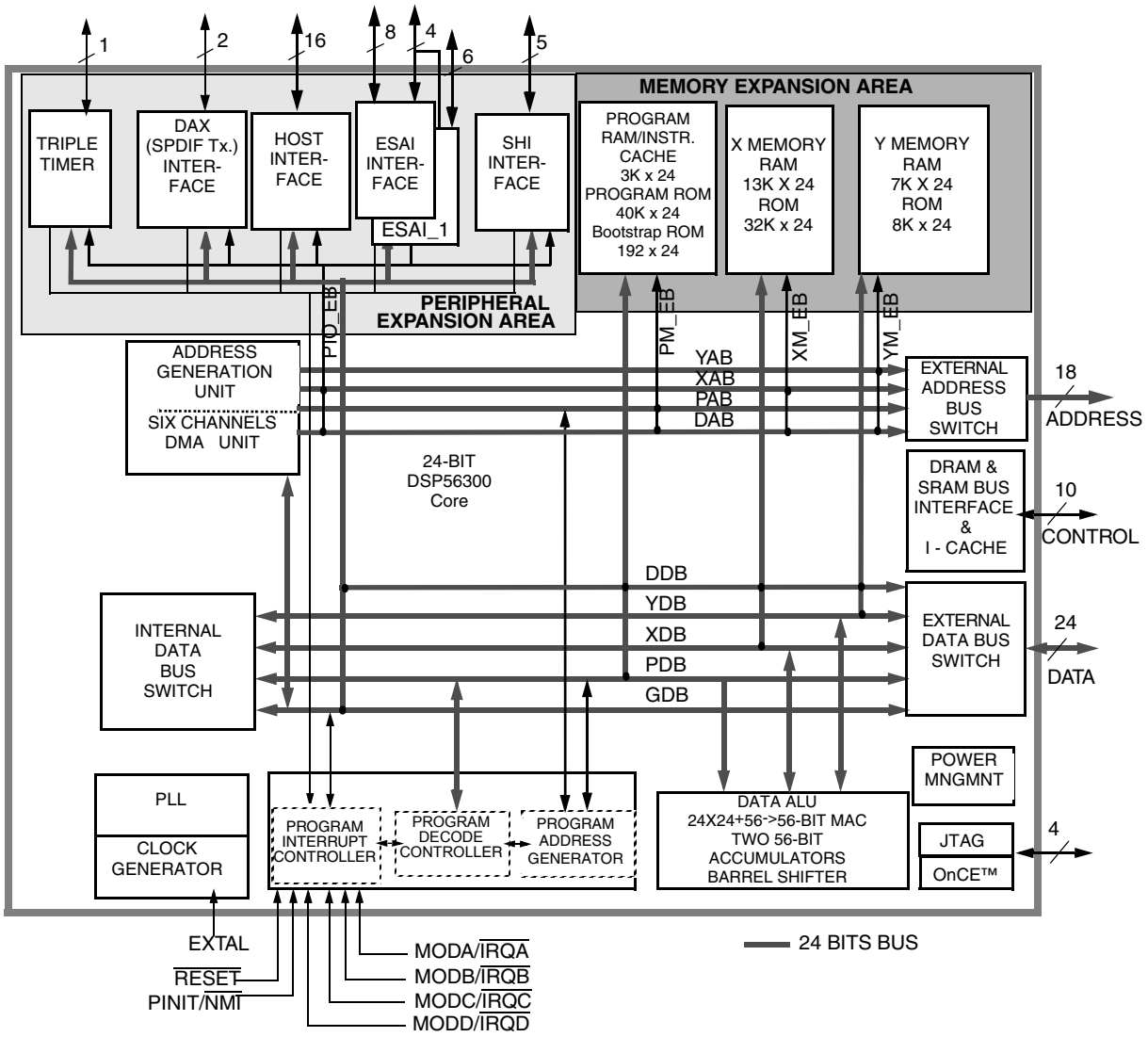


Figure 1-1 DSP56366 Block Diagram

- Serial Host Interface (SHI): SPI and I^2C protocols, multi master capability, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Byte-wide parallel Host Interface (HDI08) with DMA support.
- Triple Timer module (TEC).
- Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
- Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

1.1.5 Packaging

- 144-pin plastic LQFP package.

1.2 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56366 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56366 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56366 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56366UM
DSP56366 Product Brief	Brief description of the chip	DSP56366P
DSP56366 Technical Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56366
IBIS Model	Input Output Buffer Information Specification.	For software or simulation models, contact sales or go to www.freescale.com.

2.10 Enhanced Serial Audio Interface_1

Table 2-12 Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	**Frame Sync for Receiver_1**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected	GPIO disconnected	**Port E 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
FST_1	Input or output	GPIO disconnected	**Frame Sync for Transmitter_1**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PE4	Input, output, or disconnected	GPIO disconnected	**Port E 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SCKR_1	Input or output	GPIO disconnected	**Receiver Serial Clock_1**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.

Table 2-12 Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
PE0	Input, output, or disconnected	GPIO disconnected	**Port E 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SCKT_1	Input or output	GPIO disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected	GPIO disconnected	**Port E 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SDO5_1	Output	GPIO disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input	GPIO disconnected	**Serial Data Input 0_1**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected	GPIO disconnected	**Port E 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SDO4_1	Output	GPIO disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input	GPIO disconnected	**Serial Data Input 1_1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected	GPIO disconnected	**Port E 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

NOTES

3.4 DC Electrical Characteristics

Table 3-3 DC Electrical Characteristics[1]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.14	3.3	3.46	V
Input high voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1$_{(except\ SDO4_1)}$ • MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1$_{(only\ SDO4_1)}$/SHI$_{(SPI\ mode)}$ • SHI$_{(I2C\ mode)}$ • EXTAL[3]	 V_{IH} V_{IHP} V_{IHP} V_{IHX}	 2.0 2.0 1.5 0.8 × V_{CC}	 — — — —	 V_{CC} + 3.95 V_{CC} + 3.95 V_{CC}	V
Input low voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1$_{(except\ SDO4_1)}$ • MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1$_{(only\ SDO4_1)}$/SHI$_{(SPI\ mode)}$ • SHI$_{(I2C\ mode)}$ • EXTAL[3]	 V_{IL} V_{ILP} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3 –0.3	 — — — —	 0.8 0.8 0.3 x V_{CC} 0.2 x V_{CC}	V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[4,5] • CMOS (I_{OH} = –10 µA)[4]	 V_{OH} V_{OH}	 2.4 V_{CC} – 0.01	 — —	 — —	V
Output low voltage • TTL (I_{OL} = 3.0 mA, open-drain pins I_{OL} = 6.7 mA)[4,5] • CMOS (I_{OL} = 10 µA)[4]	 V_{OL} V_{OL}	 — —	 — —	 0.4 0.01	V
Internal supply current[6] at internal clock of 120MHz • In Normal mode • In Wait mode • In Stop mode[7]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 116 7.3 1	 200 25 10	mA
PLL supply current		—	1	2.5	mA
Input capacitance[4]	C_{IN}	—	—	10	pF

1 V_{CC} = 3.3 V ± .16 V; T_J = – 40°C to +110°C, C_L = 50 pF

2 Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$,and MODD/$\overline{IRQD}$ pins.

3 Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

4 Periodically sampled and not 100% tested.

5 This characteristic does not apply to PCAP.

Table 3-4 Internal Clocks

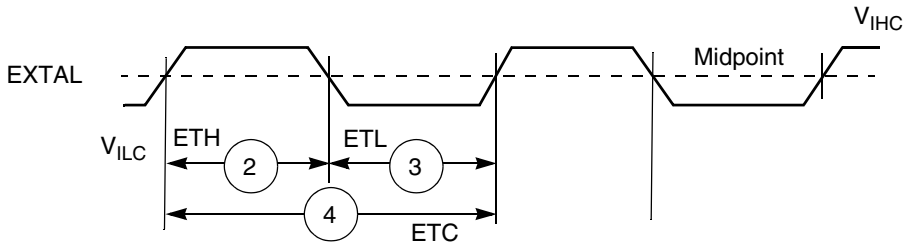
Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal clock cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

1 DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle

2 See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

3.7 EXTERNAL CLOCK OPERATION

The DSP56366 system clock is an externally supplied square wave voltage source connected to EXTAL (See Figure 3-1).



Notes The midpoint is 0.5 (V_{IHC} + V_{ILC}).

Figure 3-1 External Clock Timing

Table 3-5 Clock Operation

No.	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	120.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_H	 3.89 ns 3.54 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_L	 3.89 ns 3.54 ns	 ∞ 157.0 µs

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression	Min	Max	Unit
27	Interrupt Requests Rate				
	• HDI08, ESAI, ESAI_1, SHI, DAX, Timer	$12T_C$	—	100.0	ns
	• DMA	$8T_C$	—	66.7	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8T_C$	—	66.7	ns
	• $\overline{\text{IRQ}}$ (level trigger)	$12T_C$	—	100.0	ns
28	DMA Requests Rate				
	• Data read from HDI08, ESAI, ESAI_1, SHI, DAX	$6T_C$	—	50.0	ns
	• Data write to HDI08, ESAI, ESAI_1, SHI, DAX	$7T_C$	—	58.0	ns
	• Timer	$2T_C$		16.7	
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3T_C$	—	25.0	ns
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	37.4	—	ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to + 110°C, C_L = 50 pF

2 Periodically sampled and not 100% tested.

3 $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid. When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

4 If PLL does not lose lock.

5 When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

6 WS = number of wait states (measured in clock cycles, number of T_C). Use expression to compute maximum value.

7 This timing depends on several settings:

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs: the stop delay counter completes count or PLL lock procedure completion.

PLC value for PLL disable is 0.

The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 120 MHz it is 4096/120 MHz = 34.1 μs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.

Table 3-8 SRAM Read and Write Accesses[1] (continued)

No.	Characteristics	Symbol	Expression[2]	Min	Max	Unit
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	$0.25 \times T_C - 2.0$ [WS = 1]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [WS ≥ 4]	8.4	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.0$ [WS = 1]	8.5	—	ns
			All frequencies: $WS \times T_C - 4.0$ [2 ≤ WS ≤ 3]	12.7	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [WS ≥ 4]	25.2	—	ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	8.4	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	16.7	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	6.4	—	ns
			$2.25 \times T_C - 4.0$ [WS ≥ 8]	14.7	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	$(WS + 0.75) \times T_C - 7.0$ [WS ≥ 1]	—	7.6	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	$(WS + 0.25) \times T_C - 7.0$ [WS ≥ 1]	—	3.4	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[3]	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ [WS ≥ 1]	10.6	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	$(WS - 0.25) \times T_C - 3.0$ [WS ≥ 1]	3.2	—	ns

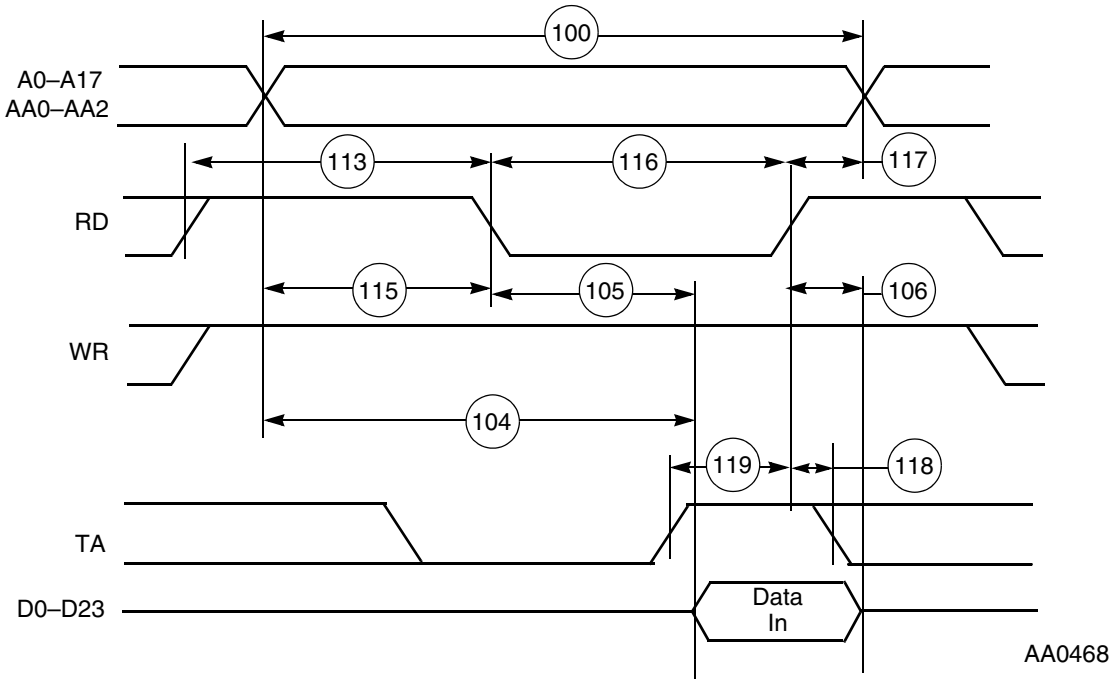


Figure 3-9 SRAM Read Access

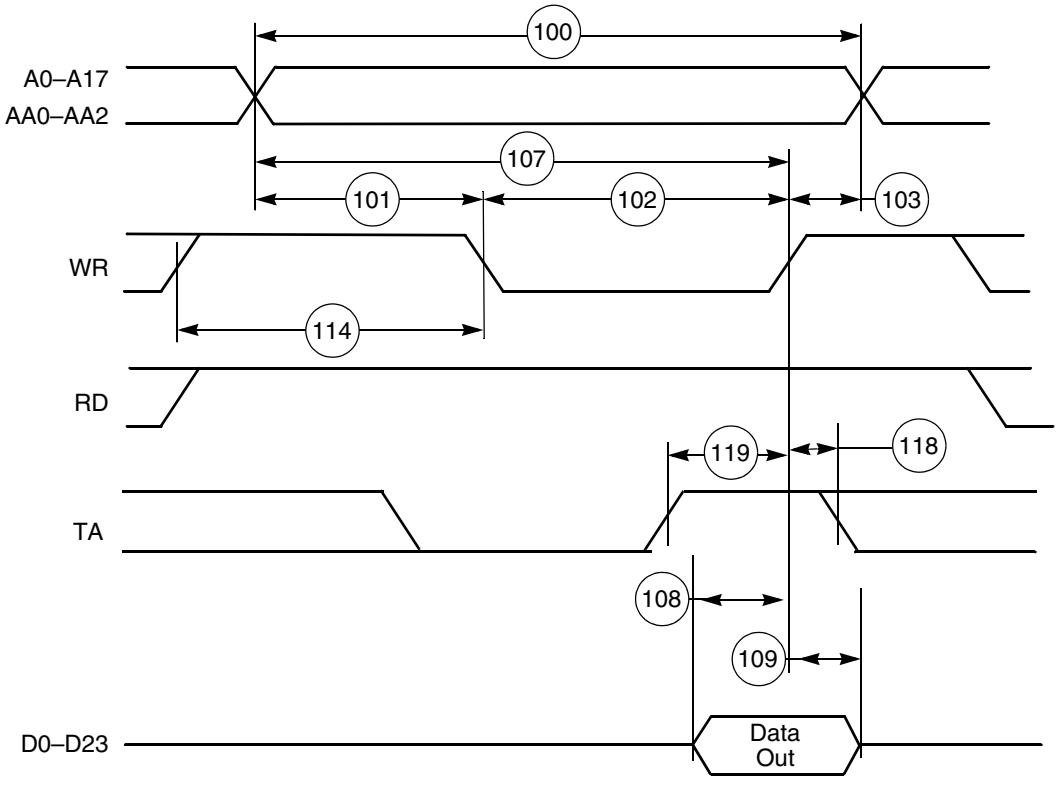


Figure 3-10 SRAM Write Access

5 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).

6 BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

7 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses	t_{PC}	$2 \times T_C$ $1.25 \times T_C$	40.0 35.0	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 7.0$	—	13.0	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 7.0$	—	23.0	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.25 \times T_C - 6.0$ $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — — 41.5 61.5	 — — — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	ns

Table 3-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	4.3	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	25.2	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	37.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	6.4	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 4.0$	6.4	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	22.9	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	33.0	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	35.3	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	26.9	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	25.2	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	6.1	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	33.5	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$3.25 \times T_C - 7.0$	—	20.1	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	5.9	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.1	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56366.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

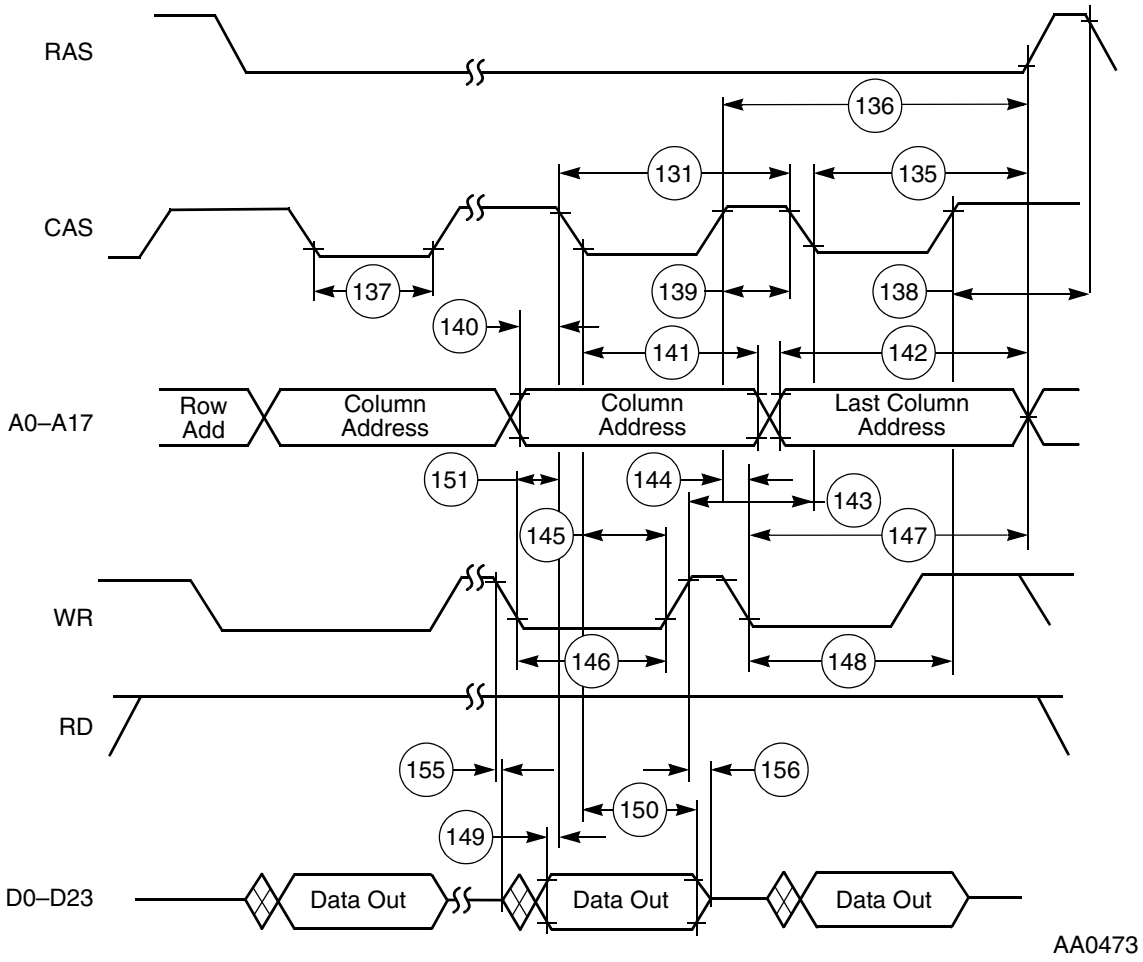


Figure 3-12 DRAM Page Mode Write Accesses

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	114.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	68.9	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	48.1	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	77.2	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	74.9	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	8.5	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	35.6	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	125.2	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$14 \times T_C - 5.7$	—	111.0	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	5.9	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.1	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

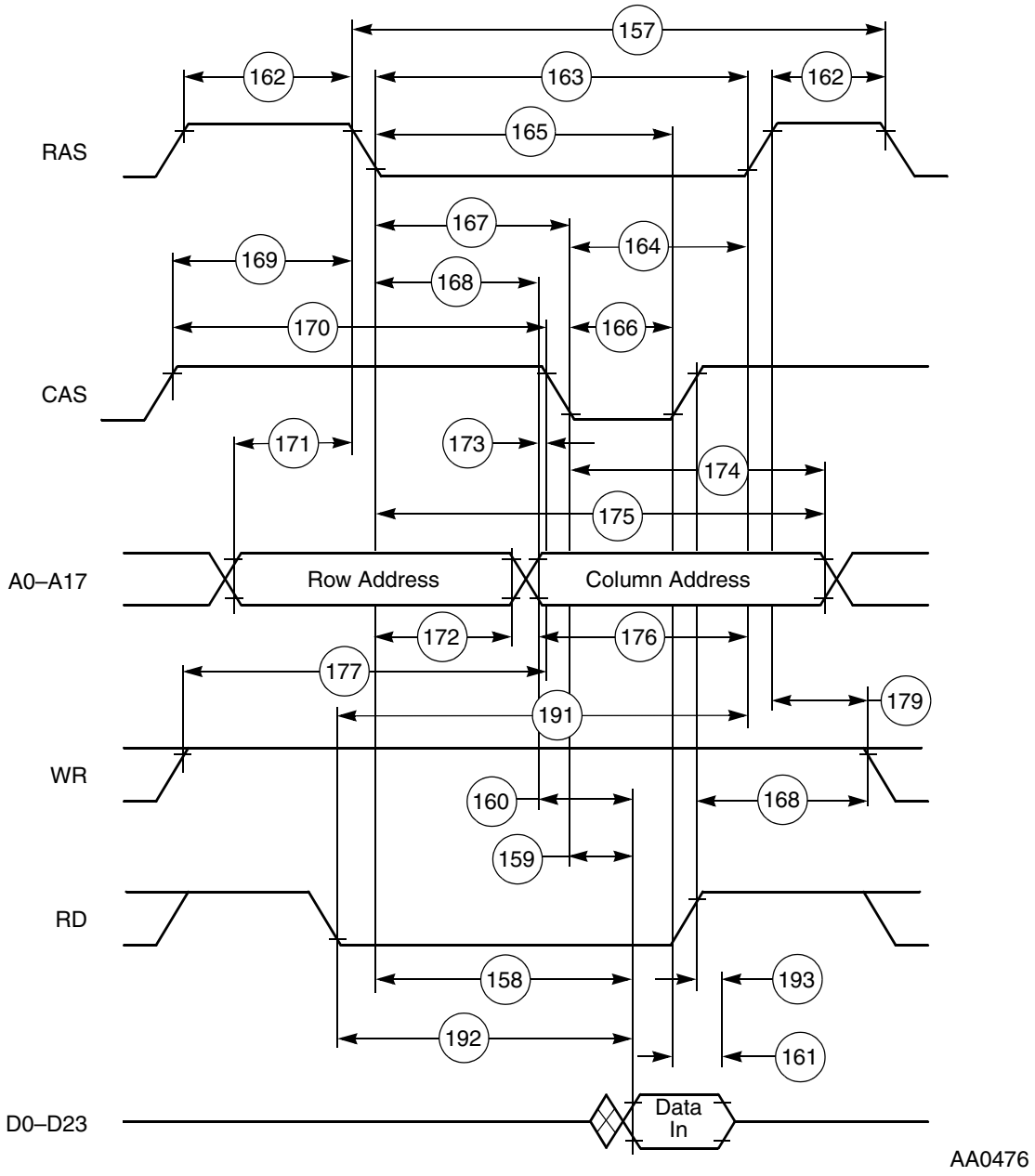


Figure 3-15 DRAM Out-of-Page Read Access

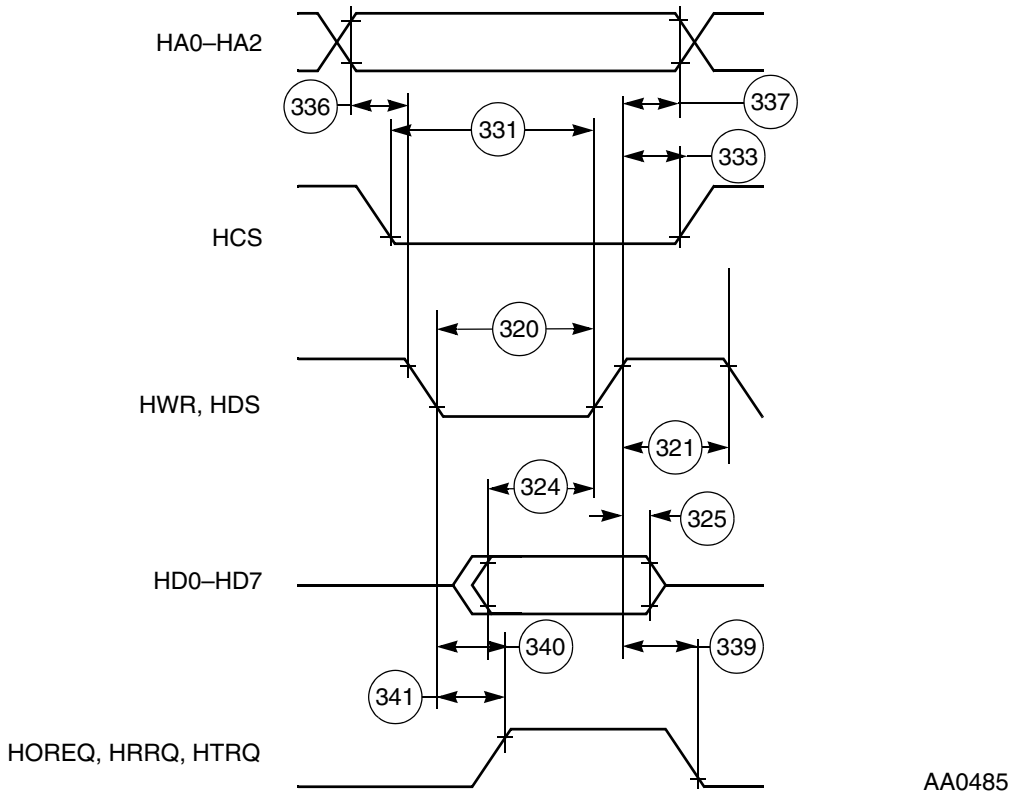
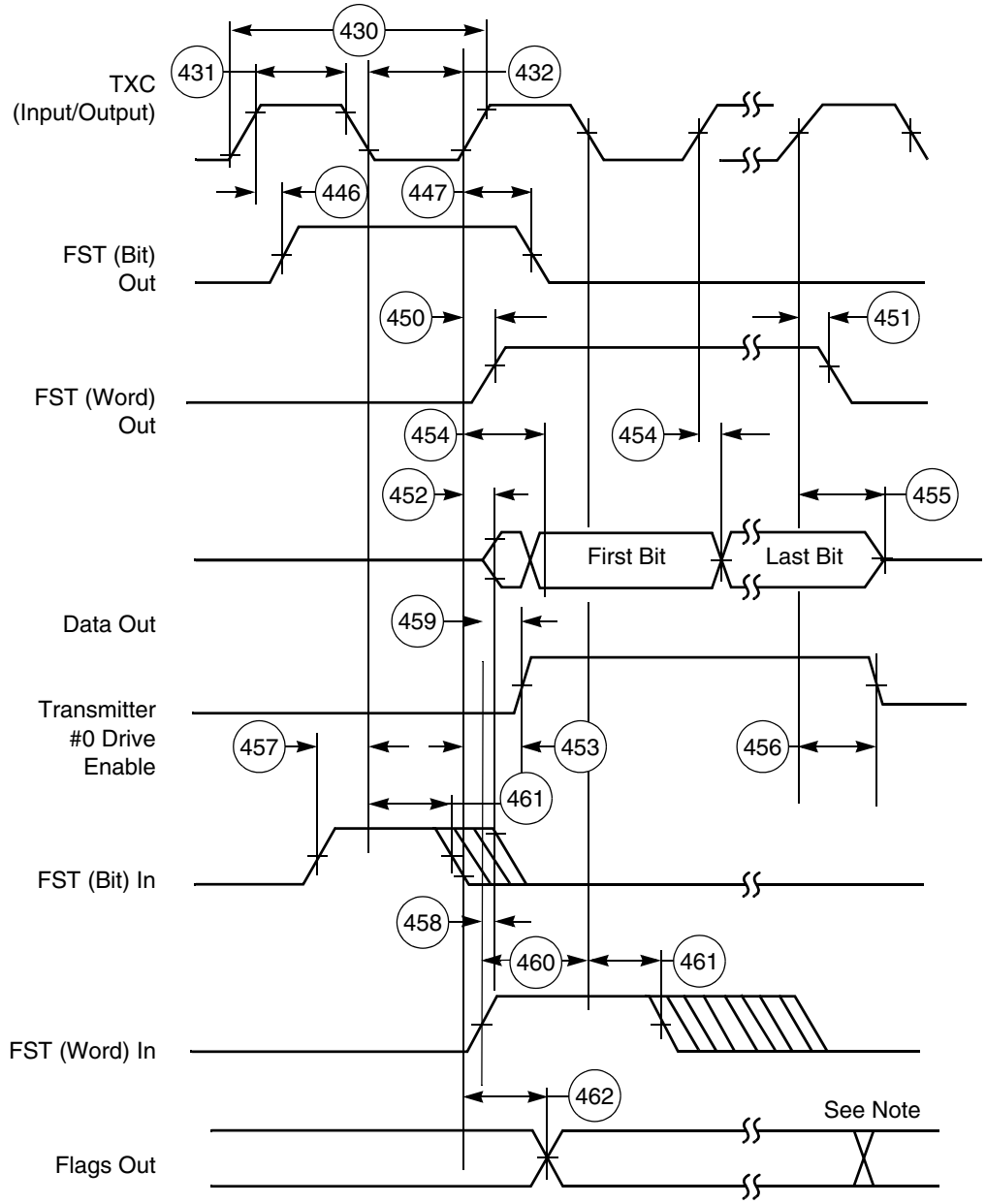


Figure 3-22 Write Timing Diagram, Non-Multiplexed Bus

3.13 Serial Host Interface (SHI) I²C Protocol Timing

Table 3-20 SHI I²C Protocol Timing

No.	Characteristics[1,2,3]	Symbol/ Expression	Standard Mode[4]		Fast Mode[5]		Unit
			Min	Max	Min	Max	
	Tolerable spike width on SCL or SDA						
	Filters bypassed	—	—	0	—	0	ns
	Narrow filters enabled		—	50	—	50	ns
	Wide filters enabled		—	100	—	100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
171	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
175	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
176	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
177	SCL and SDA rise time	T_R	—	1000	$20 + 0.1 \times C_b$	300	ns
178	SCL and SDA fall time	T_F	—	300	$20 + 0.1 \times C_b$	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
180	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
181	DSP clock frequency	F_{DSP}					MHz
	Filters bypassed		10.6	—	28.5	—	
	Narrow filters enabled		11.8	—	39.7	—	
	Wide filters enabled		13.1	—	61.0	—	
182	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
183	Stop condition set-up time	$T_{SU;STO}$	4.0	—	0.6	—	µs
184	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns



Notes In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

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Figure 3-32 ESAI Transmitter Timing

3.16 Timer Timing

Table 3-24 Timer Timing

No.	Characteristics	Expression	120 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	18.7	—	ns
481	TIO High	$2 \times T_C + 2.0$	18.7	—	ns
Note: V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF					

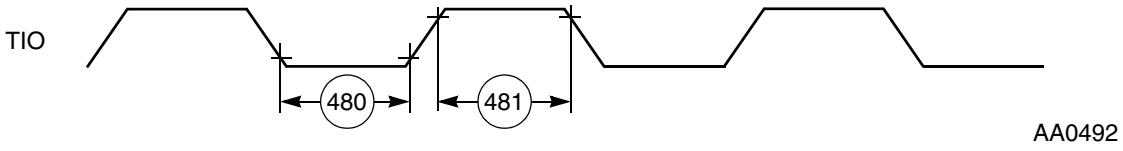

Figure 3-37 TIO Timer Event Input Restrictions

3.17 GPIO Timing

Table 3-25 GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
490[2]	EXTAL edge to GPIO out valid (GPIO out delay time)		—	32.8	ns
491	EXTAL edge to GPIO out not valid (GPIO out hold time)		4.8	—	ns
492	GPIO In valid to EXTAL edge (GPIO in set-up time)		10.2	—	ns
493	EXTAL edge to GPIO in not valid (GPIO in hold time)		1.8	—	ns
494[2]	Fetch to EXTAL edge before GPIO change	$6.75 \times T_C$-1.8	54.5	—	ns
495	GPIO out rise time	—	—	13	ns
496	GPIO out fall time	—	—	13	ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF
2 Valid only when PLL enabled with multiplication factor equal to one.

NOTES