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#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0113pj005ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Table 3.	Signal	Descriptions	(Continued)	
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Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	I	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD.
		<b>Caution:</b> The DBG pin is open-drain and requires an external pull- up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V <sub>DD</sub>	Ι	Digital Power Supply.
AV <sub>DD</sub>	I	Analog Power Supply.
V <sub>SS</sub>	I	Digital Ground.
AV <sub>SS</sub>	Ι	Analog Ground.
Note: The AV <sub>DD</sub> and A PB7 on 28-pin pa	.V <sub>SS</sub> sigr ackages	nals are available only in 28-pin packages with ADC. They are replaced by PB6 and without ADC.

# **Pin Characteristics**

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

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# **Address Space**

The eZ8 CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more detailed information regarding the eZ8 CPU and its address space, refer to eZ8 CPU Core User Manual (UM0128) available for download at www.zilog.com.

# **Register File**

The Register File address space in the Z8 Encore! XP<sup>®</sup> MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. Z8 Encore! XP F0823 Series devices contain 256 B-1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

# **Program Memory**

The eZ8 CPU supports 64 KB of Program Memory address space. Z8 Encore! XP F0823 Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space. Reading from Program Memory addresses outside the available Flash

	<b>Reset Characteristics and Latency</b>						
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)				
System Reset	Reset (as applicable)	Reset	66 Internal Precision Oscillator Cycles				
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	66 Internal Precision Oscillator Cycles + IPO startup time				

#### Table 9. Reset and Stop Mode Recovery Characteristics and Latency

During a System Reset or Stop Mode Recovery, the IPO requires 4 µs to start up. Then the Z8 Encore! XP F0823 Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer, and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

When the control registers are re-initialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

## **Reset Sources**

Table 10 lists the possible sources of a System Reset.

tions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see On-Chip Debugger on page 151.

# **Crystal Oscillator Override**

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see Oscillator Control Register Definitions on page 167), the GPIO settings are overridden and PA0 and PA1 are disabled.

# **5 V Tolerance**

All six I/O pins on the 8-pin devices are 5 V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than  $V_{DD}$  are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

**Note:** In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0], and PC[2:0]. All other signal pins are 5 V-tolerant, and can safely handle inputs higher than  $V_{DD}$  even with the pull-ups enabled.

# **External Clock Setup**

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see Oscillator Control Register Definitions on page 167) such that the external oscillator is selected as the system clock. For 8-pin devices use PA1 instead of PB3.

# Port A–C Address Registers

The Port A–C Address registers select the GPIO Port functionality accessible through the Port A–C Control registers. The Port A–C Address and Control registers combine to provide access to all GPIO Port controls (Table 18).

## Table 18. Port A–C GPIO Address Registers (PxADDR)

BITS	7	6	5	4	3	2	1	0	
FIELD	PADDR[7:0]								
RESET		00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR		FD0H, FD4H, FD8H							

PADDR[7:0]—Port Address

The Port Address selects one of the sub-registers accessible through the Port Control register.

PADDR[7:0]	Port Control Sub-register Accessible Using the Port A–C Control Registers
00H	No function. Provides some protection against accidental Port reconfiguration.
01H	Data Direction.
02H	Alternate Function.
03H	Output Control (Open-Drain).
04H	High Drive Enable.
05H	Stop Mode Recovery Source Enable.
06H	Pull-up Enable.
07H	Alternate Function Set 1.
08H	Alternate Function Set 2.
09H–FFH	No function.

# Port A–C Control Registers

The Port A–C Control registers set the GPIO port operation. The value in the corresponding Port A–C Address register determines which sub-register is read from or written to by a Port A–C Control register transaction (Table 19).

# **Interrupt Control Register Definitions**

For all interrupts other than the Watchdog Timer interrupt, the Primary Oscillator Fail Trap, and the Watchdog Timer Oscillator Fail Trap, the interrupt control registers enable individual interrupts, set interrupt priorities, and indicate interrupt requests.

## **Interrupt Request 0 Register**

The Interrupt Request 0 (IRQ0) register (Table 34) stores the interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ0 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 0 register to determine if any interrupt requests are pending.

BITS	7	6	5	4	3	2	1	0			
FIELD	Reserved	T1I	ТОІ	U0RXI	U0TXI	Reserved	Reserved	ADCI			
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		FC0H									

Table 34. Interrupt Request 0 Register (IRQ0)

Reserved—Must be 0

T1I—Timer 1 Interrupt Request

- 0 = No interrupt request is pending for Timer 1
- 1 = An interrupt request from Timer 1 is awaiting service

T0I—Timer 0 Interrupt Request

- 0 = No interrupt request is pending for Timer 0
- 1 = An interrupt request from Timer 0 is awaiting service

U0RXI-UART 0 Receiver Interrupt Request

- 0 = No interrupt request is pending for the UART 0 receiver
- 1 = An interrupt request from the UART 0 receiver is awaiting service

U0TXI-UART 0 Transmitter Interrupt Request

- 0 = No interrupt request is pending for the UART 0 transmitter
- 1 = An interrupt request from the UART 0 transmitter is awaiting service

ADCI—ADC Interrupt Request

- 0 = No interrupt request is pending for the ADC
- 1 = An interrupt request from the ADC is awaiting service

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#### Table 43. IRQ2 Enable and Priority Encoding (Continued)

IRQ2ENH[x]	IRQ2ENL[	c] Priority	Description
1	1	Level 3	High

where x indicates the register bits from 0–7.

#### Table 44. IRQ2 Enable High Bit Register (IRQ2ENH)

BITS	7	6	5	4	3	2	1	0		
FIELD	Reserved				C3ENH	C2ENH	C1ENH	C0ENH		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR		FC7H								

Reserved—Must be 0

C3ENH—Port C3 Interrupt Request Enable High Bit C2ENH—Port C2 Interrupt Request Enable High Bit C1ENH—Port C1 Interrupt Request Enable High Bit C0ENH—Port C0 Interrupt Request Enable High Bit

#### Table 45. IRQ2 Enable Low Bit Register (IRQ2ENL)

BITS	7	6	5	4	3	2	1	0	
FIELD	Reserved				C3ENL	C2ENL	C1ENL	C0ENL	
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	FC8H								

Reserved-Must be 0

C3ENL—Port C3 Interrupt Request Enable Low Bit C2ENL—Port C2 Interrupt Request Enable Low Bit C1ENL—Port C1 Interrupt Request Enable Low Bit C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 46) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin.

timer value is not reset to 0001H). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon Compare.

If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting. Follow the steps below to configure a timer for COMPARE mode and to initiate the count:

- 1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for Compare mode.
  - Set the prescale value.
  - Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate.
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer and initiate counting.

In COMPARE mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

 $COMPARE Mode Time (s) = \frac{(Compare Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$ 

#### GATED Mode

In GATED mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer Reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

- Configure the timer for CAPTURE/COMPARE mode
- Set the prescale value
- Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input Capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control register to enable the timer.
- 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) =  $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$ 

## **Reading the Timer Count Values**

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte register is read, the contents of the Timer Low Byte register are placed in a holding register. A subsequent read from the Timer Low Byte register returns the value in the hold-ing register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte register returns the actual value in the counter.

## **Timer Pin Signal Operation**

Timer Output is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO Alternate Function Registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT mode. For this mode, there is no timer input available.

## Watchdog Timer Refresh

When first enabled, the WDT is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the down counter to be reloaded with the WDT Reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When Z8 Encore! XP<sup>®</sup> F0823 Series devices are operating in DEBUG Mode (using the OCD), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

## Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT\_RES Flash Option Bit determines the time-out response of the Watchdog Timer. For information on programming of the WDT\_RES Flash Option Bit, see Flash Option Bits on page 141.

#### WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watchdog Timer Control register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

The Reset Status Register (see Reset Status Register on page 28) must be read before clearing the WDT interrupt. This read clears the WDT time-out Flag and prevents further WDT interrupts for immediately occurring.

#### WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and Z8 Encore! XP F0823 Series are in STOP mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watchdog Timer Control register are set to 1 following a WDT time-out in STOP mode. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

# Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. The features of UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two STOP bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit baud rate generator (BRG)
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes
- BRG can be configured and used as a basic 16-bit timer
- Driver Enable output for external bus transceivers

## Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 displays the UART architecture.

## **Software Compensation Procedure**

The value read from the ADC high and low byte registers are uncompensated. The user mode software must apply gain and offset correction to this uncompensated value for maximum accuracy. The following formula yields the compensated value:

 $ADC_{comp} = (ADC_{uncomp} - OFFCAL) + ((ADC_{uncomp} - OFFCAL) * GAINCAL)/2^{16}$ 

where GAINCAL is the gain calibration byte, OFFCAL is the offset calibration byte and  $ADC_{uncomp}$  is the uncompensated value read from the ADC. The OFFCAL value is in two's complement format, as are the compensated and uncompensated ADC values.

- **Note:** The offset compensation is performed first, followed by the gain compensation. One bit of resolution is lost because of rounding on both the offset and gain computations. As a result the ADC registers read back 13 bits: 1 sign bit, two calibration bits lost to rounding and 10 data bits. Also note that in the second term, the multiplication must be performed before the division by 2<sup>16</sup>. Otherwise, the second term evaluates to zero incorrectly.
- **Caution:** Although the ADC can be used without the gain and offset compensation, it does exhibit non-unity gain. Designing the ADC with sub-unity gain reduces noise across the ADC range but requires the ADC results to be scaled by a factor of 8/7.

# **ADC Control Register Definitions**

The following sections define the ADC control registers.

## **ADC Control Register 0**

The ADC Control register selects the analog input channel and initiates the analog-to-digital conversion.

BITS	7	6	5	4	3	2	1	0			
FIELD	CEN	REFSELL	REFEXT	CONT	ANAIN[3:0]						
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F70H									

Table 72. ADC Control Register 0 (ADCCTL0)

CEN—Conversion Enable

0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete.

1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete.

# Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

The Flowchart in Figure 21 displays basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase, and Mass Erase) displayed in Figure 21.

## Table 95. Serialization Data Locations

Info Page Address	Memory Address	Usage
1C	FE1C	Serial Number Byte 3 (most significant)
1D	FE1D	Serial Number Byte 2
1E	FE1E	Serial Number Byte 1
1F	FE1F	Serial Number Byte 0 (least significant)

## **Randomized Lot Identifier**

## Table 96. Lot Identification Number (RAND\_LOT)

BITS	7	6	5	4	3	2	1	0	
FIELD	RAND_LOT								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	DR Interspersed throughout Information Page Memory								
Note: U = Unchanged by Reset. R/W = Read/Write.									

RAND LOT-Randomized Lot ID

The randomized lot ID is a 32 byte binary value that changes for each production lot.

#### Table 97. Randomized Lot ID Locations

Info Page Address	Memory Address	Usage
3C	FE3C	Randomized Lot ID Byte 31 (most significant)
3D	FE3D	Randomized Lot ID Byte 30
3E	FE3E	Randomized Lot ID Byte 29
3F	FE3F	Randomized Lot ID Byte 28
58	FE58	Randomized Lot ID Byte 27
59	FE59	Randomized Lot ID Byte 26
5A	FE5A	Randomized Lot ID Byte 25
5B	FE5B	Randomized Lot ID Byte 24

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Accombly		Addre	Address Mode		Flags					Eatab	Inetr	
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	z	S	v	D	Н	Cycles	Cycles
COM dst	$dst \leftarrow \simdst$	R		60	_	*	*	0	_	_	2	2
		IR		61	-						2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	-	_	2	3
		r	lr	A3	-						2	4
		R	R	A4	_						3	3
		R	IR	A5	_						3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	-	_	3	3
		r	lr	1F A3	_						3	4
		R	R	1F A4	_						4	3
		R	IR	1F A5	_						4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	-	_	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	-	-	4	3
		ER	IM	A9	_						4	3
DA dst	$dst \gets DA(dst)$	R		40	*	*	*	Х	-	-	2	2
		IR		41							2	3
DEC dst	dst ← dst - 1	R		30	_	*	*	*	-	_	2	2
		IR		31							2	3
DECW dst	dst ← dst - 1	RR		80	_	*	*	*	-	-	2	5
		IRR		81	_						2	6
DI	IRQCTL[7] ← 0			8F	_	_	_	-	-	-	1	2
DJNZ dst, RA	dst        ← dst	r		0A-FA	-	-	-	-	-	_	2	3
EI	IRQCTL[7] ← 1			9F	_	_	_	_	-	_	1	2
Flags Notation:	* = Value is a function of f – = Unaffected X = Undefined	he resu	It of the o	peration.	0 = 1 =	= Re = Se	eset et to	to 1	0			

## Table 115. eZ8 CPU Instruction Summary (Continued)

# **On-Chip Peripheral AC and DC Electrical Characteristics**

# Table 122. Power-On Reset and Voltage Brownout Electrical Characteristics and Timing

		T <sub>A</sub> = -40 °C to +105 °C						
Symbol	Parameter	Minimum	Typical <sup>1</sup>	Maximum	Units	Conditions		
V <sub>POR</sub>	Power-On Reset Voltage Threshold	2.20	2.45	2.70	V	V <sub>DD</sub> = V <sub>POR</sub>		
V <sub>VBO</sub>	Voltage Brownout Reset Voltage Threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$		
	$V_{POR}$ to $V_{VBO}$ hysteresis		50	75	mV			
	Starting V <sub>DD</sub> voltage to ensure valid Power-On Reset.	_	V <sub>SS</sub>	-	V			
T <sub>ANA</sub>	Power-On Reset Analog Delay	-	70	-	μs	V <sub>DD</sub> > V <sub>POR</sub> ; T <sub>POR</sub> Digital Reset delay follows T <sub>ANA</sub>		
T <sub>POR</sub>	Power-On Reset Digital Delay		16		μs	66 Internal Precision Oscillator cycles + IPO startup time (T <sub>IPOST</sub> )		
T <sub>SMR</sub>	Stop Mode Recovery		16		μs	66 Internal Precision Oscillator cycles		
T <sub>VBO</sub>	Voltage Brownout Pulse Rejection Period	_	10	-	μs	Period of time in which $V_{DD}$ < $V_{VBO}$ without generating a Reset.		
T <sub>RAMP</sub>	Time for $V_{DD}$ to transition from $V_{SS}$ to $V_{POR}$ to ensure valid Reset	0.10	_	100	ms			
T <sub>SMP</sub>	Stop Mode Recovery pin pulse rejection period		20		ns	For any SMR pin or for the Reset pin when it is asserted in STOP mode.		
<sup>1</sup> Data in the typical column is from characterization at 3.3 V and 30 °C. These values are provided for design guidance only and are not tested in production.								

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		V <sub>DD</sub> = 3.0 V to 3.6 V T <sub>A</sub> = 0 °C to +70 °C (unless otherwise stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
	Resolution	10		-	bits	
	Differential Nonlinearity (DNL)	-1.0	_	1.0	LSB <sup>3</sup>	External V <sub>REF</sub> = 2.0 V; R <sub>S</sub> $\leftarrow$ 3.0 k $\Omega$
	Integral Nonlinearity (INL)	-3.0	_	3.0	LSB <sup>3</sup>	External V <sub>REF</sub> = 2.0 V; R <sub>S</sub> $\leftarrow$ 3.0 k $\Omega$
	Offset Error with Calibration		<u>+</u> 1		LSB <sup>3</sup>	
	Absolute Accuracy with Calibration		<u>+</u> 3		LSB <sup>3</sup>	
V <sub>REF</sub>	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
V <sub>REF</sub>	Internal Reference Variation with Temperature		<u>+</u> 1.0		%	Temperature variation with V <sub>DD</sub> = 3.0
V <sub>REF</sub>	Internal Reference Voltage Variation with V <sub>DD</sub>		<u>+</u> 0.5		%	Supply voltage variation with T <sub>A</sub> = 30 °C
R <sub>REFOUT</sub>	Reference Buffer Output Impedance		850		Ω	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)
	Single-Shot Conversion Time	_	5129	_	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement
	Continuous Conversion Time	_	256	_	System clock cycles	All measurements but temperature sensor
			512			Temperature sensor measurement
	Signal Input Bandwidth	_	10		kHz	As defined by -3 dB point
R <sub>S</sub>	Analog Source Impedance <sup>4</sup>	_	_	10	kΩ	In unbuffered mode

## Table 125. Analog-to-Digital Converter Electrical Characteristics and Timing

## UART Timing

Figure 32 and Table 130 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the transmit data register has been loaded with data prior to CTS assertion.



Figure 32. UART Timing With CTS

		De	Delay (ns)				
Parameter	Abbreviation	Minimum	Maximum				
UART							
T <sub>1</sub>	CTS Fall to DE output delay	2 * XIN period	2 * XIN period + 1 bit time				
T <sub>2</sub>	DE assertion to TXD falling edge (start bit) dela	ay ± 5					
T <sub>3</sub>	End of Stop Bit(s) to DE deassertion delay	± 5					

### Table 130. UART Timing With CTS

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reset in STOP mode 89 time-out response 88 Watchdog Timer Control Register (WDTCTL) 90 WDTCTL register 90, 128, 167 WDTH register 91 WDTL register 91 WDTU register 91 working register 173 working register pair 173

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X 173 XOR 178 XORX 178

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