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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-QFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0113qb005ec

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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- 2.7 V to 3.6 V operating voltage
- Up to thirteen 5 V-tolerant input pins
- 8-, 20-, and 28-pin packages
- 0 °C to +70 °C and -40 °C to +105 °C for operating temperature ranges

Part Selection Guide

Table 1 lists the basic features and package styles available for each device within the Z8 Encore! XP[®] F0823 Series product line.

Table 1.	Z8 Encore!	XP F0823	Series	Family	Part	Selection	Guide
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Part Number	Flash (KB)	RAM (B)	I/O	ADC Inputs	Packages
Z8F0823	8	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0813	8	1024	6–24	0	8-, 20-, and 28-pins
Z8F0423	4	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0413	4	1024	6–24	0	8-, 20-, and 28-pins
Z8F0223	2	512	6–22	4–8	8-, 20-, and 28-pins
Z8F0213	2	512	6–24	0	8-, 20-, and 28-pins
Z8F0123	1	256	6–22	4–8	8-, 20-, and 28-pins
Z8F0113	1	256	6–24	0	8-, 20-, and 28-pins

memory addresses returns FFH. Writing to these unimplemented Program Memory addresses produces no effect. Table 6 describes the Program Memory maps for the Z8 Encore! XP[®] F0823 Series products.

Program Memory Address (Hex)	Function
Z8F0823 and Z8F0813 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–003D	Oscillator Fail Traps*
003E-0FFF	Program Memory
Z8F0423 and Z8F0413 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–003D	Oscillator Fail Traps*
003E-0FFF	Program Memory
Z8F0223 and Z8F0213 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–003D	Oscillator Fail Traps*
003E-07FF	Program Memory
Z8F0123 and Z8F0113 Products	
0000–0001	Flash Option Bits

 Table 6. Z8 Encore! XP F0823 Series Program Memory Maps

Reset and Stop Mode Recovery

The Reset Controller within the Z8 Encore! XP[®] F0823 Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brownout (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash Option Bit to initiate a reset)
- External RESET pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-chip Debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP mode, a Stop Mode Recovery is initiated by either of the following:

- Watchdog Timer time-out
- GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device performs the following function:

• Generates the VBO reset when the supply voltage drops below a minimum safe level

Reset Types

Z8 Encore! XP F0823 Series provides several different types of Reset operation. Stop Mode Recovery is considered a form of Reset. Table 9 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

Low-Power Modes

Z8 Encore! XP[®] F0823 Series products contain power-saving features. The highest level of power reduction is provided by the STOP mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in ACTIVE mode (defined as being in neither STOP nor HALT mode).

STOP Mode

Executing the eZ8 CPU's Stop instruction places the device into STOP mode, powering down all peripherals except the Voltage Brownout detector, and the Watchdog Timer. These two blocks may also be disabled for additional power savings. In STOP mode, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; XIN and XOUT (if previously enabled) are disabled, and PA0/PA1 revert to the states programmed by the GPIO registers.
- System clock is stopped.
- eZ8 CPU is stopped.
- Program counter (PC) stops incrementing.
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control Register.
- If enabled, the Watchdog Timer logic continues to operate.
- If enabled for operation in STOP mode by the associated Flash Option Bit, the Voltage Brownout protection circuit continues to operate.
- All other on-chip peripherals are idle.

To minimize current in STOP mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails (V_{CC} or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP mode using Stop Mode Recovery. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.



Figure 7. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins are used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The port A–D Alternate Function sub-registers configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. Table 15 on page 39 lists the alternate functions possible with each port pin. The alternate function associated at a pin is defined through Alternate Function Sets sub-registers AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

Table 19. Port A–C Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0		
FIELD		PCTL								
RESET				00	ЭH					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR				FD1H, FD	5H, FD9H					

PCTL[7:0]—Port Control

The Port Control register provides access to all sub-registers that configure the GPIO Port operation.

Port A-C Data Direction Sub-Registers

The Port A–C Data Direction sub-register is accessed through the Port A–C Control register by writing 01H to the Port A–C Address register (Table 20).

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 01H i	n Port A–C	Address Reg	gister, acces	sible throug	n the Port A-	-C Control F	Register

Table 20. Port A–C Data Direction Sub-Registers (PxDD)

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–C Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–C Input Data Register. The output driver is tristated.

Port A–C Alternate Function Sub-Registers

The Port A–C Alternate Function sub-register (Table 21) is accessed through the Port A–C Control register by writing 02H to the Port A–C Address register. The Port A–C Alternate Function sub-registers enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the Port A–C Alternate Function Set 1 Sub-Registers on page 48 and Port A–C Alternate Function Set 2 Sub-Registers on

Table 30. LED Drive Enable (LEDEN)

BITS	7	6	5	4	3	2	1	0
FIELD				LEDE	N[7:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				F8	2H			

LEDEN[7:0]—LED Drive Enable

These bits determine which Port C pins are connected to an internal current sink.

0 = Tristate the Port C pin.

1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 31). These two bits select between four programmable drive levels. Each pin is individually programmable.

Table 31. LED Drive Level High Register (LEDLVLH)

BITS	7	6	5	4	3	2	1	0	
FIELD		LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR				F8	3H				

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA01 = 7 mA10 = 13 mA

10 10 mA11 = 20 mA

LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 32). These two bits select between four programmable drive levels. Each pin is individually programmable.

BITS	7	6	5	4	3	2	1	0
FIELD	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	DH			

Table 46. Interrupt Edge Select Register (IRQES)

IES*x*—Interrupt Edge Select *x*

0 = An interrupt request is generated on the falling edge of the PAx input or PDx

1 = An interrupt request is generated on the rising edge of the PAx input PDx where x indicates the specific GPIO port pin number (0 through 7)

Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) register (Table 47) determines the source of the PADxS interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Table 47. Shared Interrupt Select Register (IRQSS)

BITS	7	6	5	4	3	2	1	0	
FIELD	Reserved	PA6CS		Reserved					
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR				FC	EH				

PA6CS—PA6/Comparator Selection

0 = PA6 is used for the interrupt for PA6CS interrupt request

1 = The Comparator is used for the interrupt for PA6CS interrupt request

Reserved-Must be 0

Interrupt Control Register

The Interrupt Control (IRQCTL) register (Table 48) contains the master enable bit for all interrupts.

COMPARATOR COUNTER Mode

In COMPARATOR COUNTER mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPARATOR COUNTER mode, the prescaler is disabled.

Caution: *The frequency of the comparator output signal must not exceed one-fourth the system clock frequency.*

After reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Follow the steps below for configuring a timer for COMPARATOR COUNTER mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARATOR COUNTER mode.
 - Select either the rising edge or falling edge of the comparator output signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This action only affects the first pass in COMPARATOR COUNTER mode. After the first timer Reload in COMPARATOR COUNTER mode, counting always begins at the reset value of 0001H. Generally, in COMPARATOR COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer.

In COMPARATOR COUNTER mode, the number of comparator output transitions since the timer start is given by the following equation:

Comparator Output Transitions = Current Count Value – Start Value

Reserved—R/W bits must be 0 during writes; 0 when read.

NEWFRM—Status bit denoting the start of a new frame. Reading the UART Receive Data register resets this bit to 0.

0 = The current byte is not the first data byte of a new frame

1 = The current byte is the first data byte of a new frame

MPRX—Multiprocessor Receive

Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data register resets this bit to 0.

UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 registers (Table 66 and Table 67) configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

Table 66. UART Control 0 Register (U0CTL0)

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F42H							

TEN—Transmit Enable

This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is low and the CTSE bit is 1, the transmitter is enabled.

0 = Transmitter disabled

1 = Transmitter enabled

REN—Receive Enable

This bit enables or disables the receiver.

- 0 =Receiver disabled
- 1 =Receiver enabled

CTSE—CTS Enable

 $0 = \text{The }\overline{\text{CTS}}$ signal has no effect on the transmitter

1 = The UART recognizes the $\overline{\text{CTS}}$ signal as an enable control from the transmitter

PEN—Parity Enable

This bit enables or disables parity. Even or odd is determined by the PSEL bit.

0 =Parity is disabled

1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0	0	0	0	0	0	0	0
R/W	R/W R/W							
ADDR	F45H							

Table 68. UART Address Compare Register (U0ADDR)

COMP ADDR—Compare Address

This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (Table 69 and Table 70) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 69. UART Baud Rate High Byte Register (U0BRH)

BITS	7	6	5	4	3	2	1	0	
FIELD	BRH								
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	F46H								

Table 70. UART Baud Rate Low Byte Register (U0BRL)

BITS	7	6	5	4	3	2	1	0		
FIELD	BRL									
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR	F47H									

The UART data rate is calculated using the following equation:

UART Baud Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

For a given UART data rate, calculate the integer baud rate divisor value using the following equation:

UART Baud Rate Divisor Value (BRG) = Round $\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$

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Figure 19. Analog-to-Digital Converter Block Diagram

Operation

Data Format

The output of the ADC is an 11-bit, signed, two's complement digital value. The output generally ranges from 0 to +1023, but offset errors can cause small negative values.

The ADC registers return 13 bits of data, but the two LSBs are intended for compensation use only. When the compensation routine is performed on the 13 bit raw ADC value, two

ADC Data Low Bits Register

The ADC Data Low Byte register contains the lower bits of the ADC output as well as an overflow status bit. The output is a 11-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte register is read-only. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

Table 75. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD		ADCDL			OVF			
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
ADDR	F73H							

ADCDL—ADC Data Low Bits

These bits are the least significant three bits of the 11-bits of the ADC output. These bits are undefined after a Reset.

Reserved—Undefined when read

OVF—Overflow Status

0= An overflow did not occur in the digital filter for the current sample

1= An overflow did occur in the digital filter for the current sample

On-Chip Debugger

Z8 Encore! XP[®] F0823 Series devices contain an integrated On-Chip Debugger (OCD) that provides advanced debugging features that include:

- Single pin interface
- Reading and writing of the register file
- Reading and writing of program and data memory
- Setting of breakpoints and watchpoints
- Executing eZ8 CPU instructions
- Debug pin sharing with general-purpose input-output function to maximize the pins available

Architecture

The on-chip debugger consists of four primary functional blocks: transmitter, receiver, auto-baud detector/generator, and debug controller. Figure 22 displays the architecture of the OCD.



Figure 22. On-Chip Debugger Block Diagram

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description		
Z8 Encore! XP with 2	KB Flash	n, 10-Bit A	Analog	g-to-D	igital C	onve	erter			
Standard Temperature: 0 °C to 70 °C										
Z8F0223PB005SC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package		
Z8F0223QB005SC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package		
Z8F0223SB005SC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package		
Z8F0223SH005SC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package		
Z8F0223HH005SC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package		
Z8F0223PH005SC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package		
Z8F0223SJ005SC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package		
Z8F0223HJ005SC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package		
Z8F0223PJ005SC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package		
Extended Temperatur	re: -40 °C	to 105 °C	2							
Z8F0223PB005EC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package		
Z8F0223QB005EC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package		
Z8F0223SB005EC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package		
Z8F0223SH005EC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package		
Z8F0223HH005EC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package		
Z8F0223PH005EC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package		
Z8F0223SJ005EC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package		
Z8F0223HJ005EC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package		
Z8F0223PJ005EC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package		
Replace C with G for Lead-Free Packaging										

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Part Number Suffix Designations



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