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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0123ph005sc">https://www.e-xfl.com/product-detail/zilog/z8f0123ph005sc</a>

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# Overview

Zilog's Z8 Encore! XP<sup>®</sup> microcontroller unit (MCU) family of products are the first Zilog<sup>®</sup> microcontroller products based on the 8-bit eZ8 CPU core. Z8 Encore! XP F0823 Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8<sup>®</sup> instructions. The rich peripheral set of Z8 Encore! XP F0823 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

## Features

The key features of Z8 Encore! XP F0823 Series include:

- 5 MHz eZ8 CPU
- 1 KB, 2 KB, 4 KB, or 8 KB Flash memory with in-circuit programming capability
- 256 B, 512 B, or 1 KB register RAM
- 6 to 24 I/O pins depending upon package
- Internal precision oscillator (IPO)
- Full-duplex UART
- The universal asynchronous receiver/transmitter (UART) baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared data association (IrDA)-compliant infrared encoder/decoders, integrated with UART
- Two enhanced 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- On-Chip Debugger (OCD)
- Optional 8-channel, 10-bit Analog-to-Digital Converter (ADC)
- On-Chip analog comparator
- Up to 20 vectored interrupts
- Direct LED drive with programmable drive strengths
- Voltage Brownout (VBO) protection
- Power-On Reset (POR)

# Interrupt Controller

The interrupt controller on the Z8 Encore! XP<sup>®</sup> F0823 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 unique interrupt vectors
  - 12 GPIO port pin interrupt sources (two are shared)
  - 8 on-chip peripheral interrupt sources (two are shared)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information on interrupt servicing by the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Interrupt Vector Listing

Table 33 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

► **Note:** *Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.*

**Table 33. Trap and Interrupt Vectors in Order of Priority**

Priority	Program Memory Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer on page 87)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Timer Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3 or Port D Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2 or Port D Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges

Watchdog Timer Reload Byte registers (WDTU, WDTL, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

This register address is shared with the read-only Reset Status Register.

**Table 58. Watchdog Timer Control Register (WDTCTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
ADDR	FF0H							

WDTUNLK—Watchdog Timer Unlock

The software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer reload registers.

## Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTL, WDTL) registers (Tables 59 through Table 61) form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value is {WDTU[7:0], WDTL[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate Reload Value. Reading from these registers returns the current Watchdog Timer count value.

**! Caution:** *The 24-bit WDT Reload Value must not be set to a value less than 000004H.*

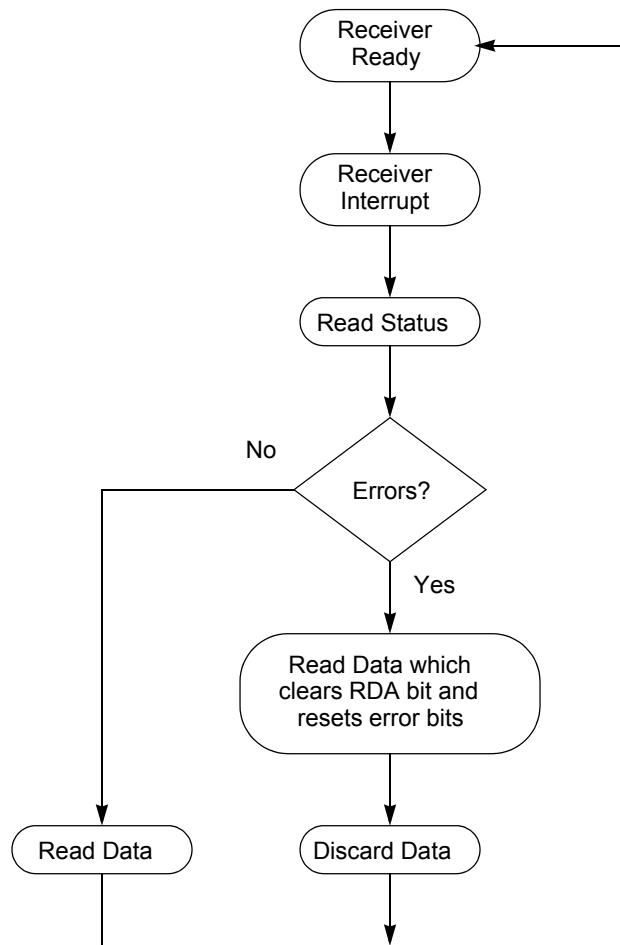
# Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. The features of UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two STOP bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit baud rate generator (BRG)
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes
- BRG can be configured and used as a basic 16-bit timer
- Driver Enable output for external bus transceivers

## Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 displays the UART architecture.



**Figure 15. UART Receiver Interrupt Service Routine Flow**

### Baud Rate Generator Interrupts

If the Baud Rate Generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

### UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value



baud rate clocks to plus eight baud rate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window this process is repeated. If the incoming data is a logical 1 (no pulse), the Endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the Endec clock counter is reset, resynchronizing the Endec to the incoming signal, allowing the Endec to tolerate jitter and baud rate errors in the incoming datastream. Resynchronizing the Endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

## Infrared Encoder/Decoder Control Register Definitions

All Infrared Endec configuration and status information is set by the UART control registers as defined in Universal Asynchronous Receiver/Transmitter on page 93.

**!** **Caution:** *To prevent spurious signals during IrDA data transmission, set the IREN bit in the UART Control 1 register to 1 to enable the Infrared Encoder/Decoder before enabling the GPIO port alternate function for the corresponding pin.*

bits of resolution are lost because of a rounding error. As a result, the final value is an 11-bit number.

## **Automatic Powerdown**

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered down. From this powerdown state, the ADC requires 40 system clock cycles to powerup. The ADC powers up when a conversion is requested by the ADC Control register.

## **Single-Shot Conversion**

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. Follow the steps below for setting up the ADC and initiating a single-shot conversion:

1. Enable the acceptable analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
2. Write the ADC Control/Status Register 1 to configure the ADC
  - Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
3. Write to the ADC Control Register 0 to configure the ADC and begin the conversion. The bit fields in the ADC Control register can be written simultaneously:
  - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
  - Clear CONT to 0 to select a single-shot conversion.
  - If the internal voltage reference must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
  - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in the ADC Control Register 0.
  - Set CEN to 1 to start the conversion.
4. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power-up before beginning the 5129 cycle conversion.

## ADC Data Low Bits Register

The ADC Data Low Byte register contains the lower bits of the ADC output as well as an overflow status bit. The output is a 11-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte register is read-only. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

**Table 75. ADC Data Low Bits Register (ADCD\_L)**

BITS	7	6	5	4	3	2	1	0
FIELD	ADCDL			Reserved				OVF
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F73H							

ADCDL—ADC Data Low Bits

These bits are the least significant three bits of the 11-bits of the ADC output. These bits are undefined after a Reset.

Reserved—Undefined when read

OVF—Overflow Status

0= An overflow did not occur in the digital filter for the current sample

1= An overflow did occur in the digital filter for the current sample

## **Operation**

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

The Flowchart in Figure 21 displays basic Flash Controller operation. The following sub-sections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase, and Mass Erase) displayed in Figure 21.

► **Note:** *This bit only enables the crystal oscillator. Its selection as system clock must be done manually.*  
*0 = Crystal oscillator is enabled during reset, resulting in longer reset timing*  
*1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing*

⚡ **Warning:** *Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin. This is due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.*

## Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 89 through Table 91.

### Trim Bit Address 0000H—Reserved

Table 89. Trim Options Bits at Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 0020H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Reserved—Altering this register may result in incorrect device operation.

### Trim Bit Address 0001H—Reserved

Table 90. Trim Option Bits at 0001H

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 0021H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Flash Read Protect Option Bit
Stuff Instruction	11H	–	Disabled.
Execute Instruction	12H	–	Disabled.
Reserved	13H–FFH	–	–

In the following list of OCD Commands, data and commands sent from the host to the OCD are identified by 'DBG ← Command/Data'. Data sent from the OCD back to the host is identified by 'DBG → Data'.

- Read OCD Revision (00H)**—The Read OCD Revision command determines the version of the OCD. If OCD commands are added, removed, or changed, this revision number changes.
 

DBG ← 00H  
 DBG → OCDRev[15:8] (Major revision number)  
 DBG → OCDRev[7:0] (Minor revision number)
- Read OCD Status Register (02H)**—The Read OCD Status register command reads the OCDSTAT register.
 

DBG ← 02H  
 DBG → OCDSTAT[7:0]
- Read Runtime Counter (03H)**—The Runtime Counter counts system clock cycles in between breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the Write Memory, Read Memory, Write Register, Read Register, Read Memory CRC, Step Instruction, Stuff Instruction, and Execute Instruction commands.
 

DBG ← 03H  
 DBG → RuntimeCounter[15:8]  
 DBG → RuntimeCounter[7:0]
- Write OCD Control Register (04H)**—The Write OCD Control Register command writes the data that follows to the OCDCTL register. When the Flash Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of returning the device to normal operating mode is to reset the device.
 

DBG ← 04H  
 DBG ← OCDCTL[7:0]
- Read OCD Control Register (05H)**—The Read OCD Control Register command reads the value of the OCDCTL register.
 

DBG ← 05H  
 DBG → OCDCTL[7:0]

**Table 110. CPU Control Instructions (Continued)**

Mnemonic	Operands	Instruction
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

**Table 111. Load Instructions**

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

**Table 112. Logical Instructions**

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR

**Table 116. Opcode Map Abbreviations**

<b>Abbreviation</b>	<b>Description</b>	<b>Abbreviation</b>	<b>Description</b>
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair



**Table 121. Internal Precision Oscillator Electrical Characteristics**

Symbol	Parameter	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$ $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ (unless otherwise stated)			Units	Conditions
		Minimum	Typical	Maximum		
$F_{IPO}$	Internal Precision Oscillator Frequency (High Speed)		5.53		MHz	$V_{DD} = 3.3\text{ V}$ $T_A = 30\text{ }^{\circ}\text{C}$
$F_{IPO}$	Internal Precision Oscillator Frequency (Low Speed)		32.7		kHz	$V_{DD} = 3.3\text{ V}$ $T_A = 30\text{ }^{\circ}\text{C}$
$F_{IPO}$	Internal Precision Oscillator Error		$\pm 1$	$\pm 4$	%	
$T_{IPOST}$	Internal Precision Oscillator Startup Time		3		$\mu\text{s}$	

**Table 125. Analog-to-Digital Converter Electrical Characteristics and Timing**

Symbol	Parameter	V <sub>DD</sub> = 3.0 V to 3.6 V T <sub>A</sub> = 0 °C to +70 °C (unless otherwise stated)			Units	Conditions
		Minimum	Typical	Maximum		
	Resolution	10		–	bits	
	Differential Nonlinearity (DNL)	-1.0	–	1.0	LSB <sup>3</sup>	External V <sub>REF</sub> = 2.0 V; R <sub>S</sub> ← 3.0 kΩ
	Integral Nonlinearity (INL)	-3.0	–	3.0	LSB <sup>3</sup>	External V <sub>REF</sub> = 2.0 V; R <sub>S</sub> ← 3.0 kΩ
	Offset Error with Calibration		±1		LSB <sup>3</sup>	
	Absolute Accuracy with Calibration		±3		LSB <sup>3</sup>	
V <sub>REF</sub>	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
V <sub>REF</sub>	Internal Reference Variation with Temperature		±1.0		%	Temperature variation with V <sub>DD</sub> = 3.0
V <sub>REF</sub>	Internal Reference Voltage Variation with V <sub>DD</sub>		±0.5		%	Supply voltage variation with T <sub>A</sub> = 30 °C
R <sub>REFOUT</sub>	Reference Buffer Output Impedance		850		Ω	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement
	Continuous Conversion Time	–	256	–	System clock cycles	All measurements but temperature sensor
			512			Temperature sensor measurement
	Signal Input Bandwidth	–	10		kHz	As defined by -3 dB point
R <sub>S</sub>	Analog Source Impedance <sup>4</sup>	–	–	10	kΩ	In unbuffered mode

Figure 33 and Table 131 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.

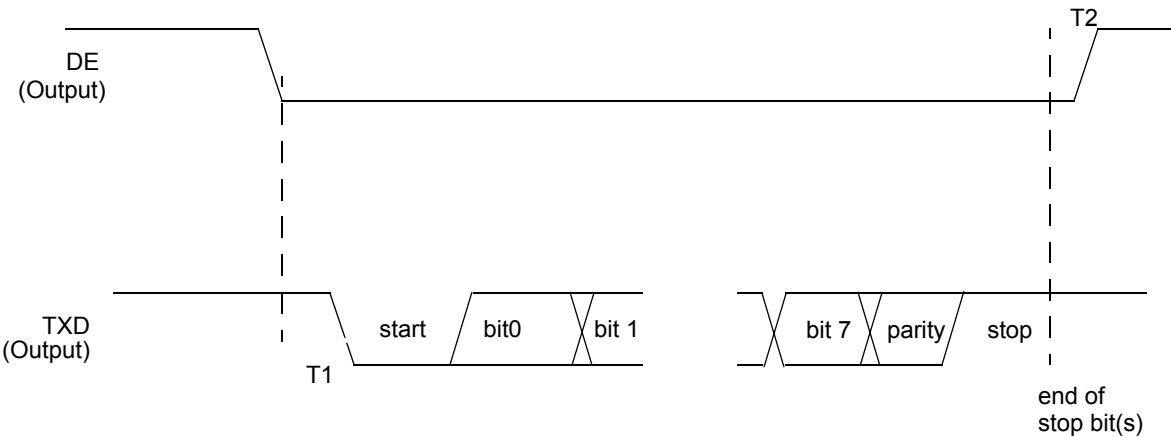


Figure 33. UART Timing Without CTS

Table 131. UART Timing Without CTS

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
UART			
T <sub>1</sub>	DE assertion to TXD falling edge (start bit) delay	1 * XIN period	1 bit time
T <sub>2</sub>	End of Stop Bit(s) to DE deassertion delay (Tx data register is empty)	± 5	

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
<b>Z8 Encore! XP with 4 KB Flash, 10-Bit Analog-to-Digital Converter</b>								
<b>Standard Temperature: 0 °C to 70 °C</b>								
Z8F0423PB005SC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005SC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005SC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005SC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005SC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005SC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005SC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005SC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005SC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>								
Z8F0423PB005EC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005EC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005EC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005EC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005EC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005EC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005EC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005EC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005EC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
<b>Z8 Encore! XP with 2 KB Flash</b>								
<b>Standard Temperature: 0 °C to 70 °C</b>								
Z8F0213PB005SC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005SC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005SC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005SC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005SC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005SC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005SC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005SC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005SC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>								
Z8F0213PB005EC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005EC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005EC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005EC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005EC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005EC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005EC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005EC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005EC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								