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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0123sb005ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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CPU and Peripheral Overview

eZ8 CPU Features

The eZ8 CPU, Zilog's latest 8-bit central processing unit (CPU), meets the continuing demand for faster and code-efficient microcontrollers. The eZ8 CPU executes a superset of the original $Z8^{\text{(R)}}$ instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory.
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks.
- Compatible with existing Z8 code.
- Expanded internal Register File allows access of up to 4 KB.
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C.
- Pipelined instruction fetch and execution.
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL.
- New instructions support 12-bit linear addressing of the Register file.
- Up to 10 MIPS operation.
- C-Compiler friendly.
- 2 to 9 clock cycles per instruction.

For more information on eZ8 CPU, refer to eZ8 CPU Core User Manual (UM0128) available for download at <u>www.zilog.com</u>.

General-Purpose I/O

Z8 Encore! XP F0823 Series features 6 to 24 port pins (Ports A–C) for general-purpose I/O (GPIO). The number of GPIO pins available is a function of package. Each pin is individually programmable. 5 V tolerant input pins are available on all I/Os on 8-pin devices, most I/Os on other package types.

Flash Controller

The Flash Controller programs and erases Flash memory. The Flash Controller supports protection against accidental program and erasure, as well as factory serialization and read protection.

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Table 10	Reset Sources	and Resulting	Reset Type
		and Resulting	

Operating Mode	Reset Source	Special Conditions				
NORMAL or HALT modes	Power-On Reset/Voltage Brownout	Reset delay begins after supply voltage exceeds POR level.				
	Watchdog Timer time-out when configured for Reset	None.				
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.				
	OCD initiated Reset (OCDCTL[0] set to 1)	System Reset, except the OCD is unaffected by the reset.				
STOP mode	Power-On Reset/Voltage Brownout	Reset delay begins after supply voltage exceeds POR level.				
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Electrical Characteristics on page 193.				
	DBG pin driven Low	None.				

Power-On Reset

Each device in the Z8 Encore! XP F0823 Series contains an internal POR circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F0823 Series device exits the POR state, the eZ8 CPU fetches the Reset vector. Following the POR, the POR status bit in Watchdog Timer Control (WDTCTL) register is set to 1.

Figure 5 displays POR operation. For the POR threshold voltage (V_{POR}), see Electrical Characteristics on page 193.

tions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see On-Chip Debugger on page 151.

Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see Oscillator Control Register Definitions on page 167), the GPIO settings are overridden and PA0 and PA1 are disabled.

5 V Tolerance

All six I/O pins on the 8-pin devices are 5 V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than V_{DD} are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

Note: In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0], and PC[2:0]. All other signal pins are 5 V-tolerant, and can safely handle inputs higher than V_{DD} even with the pull-ups enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see Oscillator Control Register Definitions on page 167) such that the external oscillator is selected as the system clock. For 8-pin devices use PA1 instead of PB3.

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT mode, the timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer Reload. If it is appropriate to have the Timer Output make a state change at a One-Shot time-out (rather than a single cycle pulse), first set the TPOL bit in the Timer Control register to the start value before enabling ONE-SHOT mode. After starting the timer, set TPOL to the opposite bit value.

Follow the steps below for configuring a timer for ONE-SHOT mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer
 - Configure the timer for ONE-SHOT mode
 - Set the prescale value
 - Set the initial output level (High or Low) if using the Timer Output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.

of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in TxCTL1 register is set to indicate the timer interrupt is because of an input capture event.

The timer continues counting up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt and continues counting. The INPCAP bit in TxCTL1 register clears indicating the timer interrupt is not because of an input capture event.

Follow the steps below for configuring a timer for CAPTURE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer
 - Configure the timer for CAPTURE mode
 - Set the prescale value
 - Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a Capture or a Reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
- 5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

CAPTURE RESTART Mode

In CAPTURE RESTART mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is

Watchdog Timer Refresh

When first enabled, the WDT is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the down counter to be reloaded with the WDT Reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When Z8 Encore! XP[®] F0823 Series devices are operating in DEBUG Mode (using the OCD), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT_RES Flash Option Bit determines the time-out response of the Watchdog Timer. For information on programming of the WDT_RES Flash Option Bit, see Flash Option Bits on page 141.

WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watchdog Timer Control register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

The Reset Status Register (see Reset Status Register on page 28) must be read before clearing the WDT interrupt. This read clears the WDT time-out Flag and prevents further WDT interrupts for immediately occurring.

WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and Z8 Encore! XP F0823 Series are in STOP mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watchdog Timer Control register are set to 1 following a WDT time-out in STOP mode. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. The features of UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two STOP bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit baud rate generator (BRG)
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes
- BRG can be configured and used as a basic 16-bit timer
- Driver Enable output for external bus transceivers

Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 displays the UART architecture.





Operation

Data Format

The UART always transmits and receives data in an 8-bit data format, least-significant bit (lsb) first. An even or odd parity bit can be added to the data stream. Each character begins with an active Low Start bit and ends with either 1 or 2 active High Stop bits. Figure 11 and Figure 12 display the asynchronous data format employed by the UART without parity and with parity, respectively.

Flash Control Register Definitions

Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FTCTL) register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL. Page Erase applies only to the active page selected in Flash Page Select register. Mass Erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

BITS	7	6	5	4	3	2	1	0			
FIELD	FCMD										
RESET	0	0	0	0	0	0	0	0			
R/W	W	W	W	W	W	W	W	W			
ADDR	FF8H										

Table 79. Flash Control Register (FCTL)

FCMD—Flash Command

73H = First unlock command

8CH = Second unlock command

95H = Page Erase command (must be third command in sequence to initiate Page Erase) 63H = Mass Erase command (must be third command in sequence to initiate Mass Erase)

5EH = Enable Flash Sector Protect Register Access

Flash Status Register

The Flash Status register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the write-only Flash Control Register.

Table 80. Flash Status Register (FSTAT)	Table	80.	Flash	Status	Register	(FSTAT)
-----------------------------------------	-------	-----	-------	--------	----------	---------

BITS	7	6	5	4	3	2	1	0	
FIELD	Rese	Reserved FSTAT							
RESET	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	
ADDR	FF8H								



Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)

DEBUG Mode

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP mode
- All enabled on-chip peripherals operate unless in STOP mode
- Automatically exits HALT mode
- Constantly refreshes the Watchdog Timer, if enabled.

Entering DEBUG Mode

The device enters DEBUG mode following the operations below:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (breakpoint) instruction
- If the DBG pin is held Low during the most recent clock cycle of System Reset, the part enters DEBUG mode upon exiting System Reset

Note: Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see OCD Auto-Baud Detector/Generator on page 154).

• If the PA2/RESET pin is held Low while a 32-bit key sequence is issued to the PA0/DBG pin, the DBG feature is unlocked. After releasing PA2/RESET, it is pulled high. At this

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Assombly		Addres	ss Mode	Opcodo(s)	Fla	igs					Fotob	Instr
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	z	S	v	D	Н	Cycles	Cycles
LDC dst, src	$dst \gets src$	r	Irr	C2	_	_	_	_	-	-	2	5
		lr	Irr	C5	-						2	9
		Irr	r	D2	-						2	5
LDCI dst, src	dst ← src	lr	Irr	C3	_	_	_	_	-	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	Ir	D3							2	9
LDE dst, src	$dst \gets src$	r	Irr	82	-	-	-	-	-	_	2	5
		Irr	r	92	-						2	5
LDEI dst, src	dst ← src	lr	Irr	83	-	-	-	-	-	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	93							2	9
LDWX dst, src	$dst \gets src$	ER	ER	1FE8	_	_	_	_	_	_	5	4
LDX dst, src	$dst \gets src$	r	ER	84	-	-	-	-	-	_	3	2
		lr	ER	85	-						3	3
		R	IRR	86	-						3	4
		IR	IRR	87	-						3	5
		r	X(rr)	88	-						3	4
		X(rr)	r	89	-						3	4
		ER	r	94	-						3	2
		ER	lr	95							3	3
		IRR	R	96	_						3	4
		IRR	IR	97	_						3	5
		ER	ER	E8	_						4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$dst \gets src + X$	r	X(r)	98		-	-	-	-	-	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	-	-	-	-	-	-	2	8
NOP	No operation			0F	_	_	_	_	_	_	1	2
Flags Notation:	* = Value is a function of f – = Unaffected X = Undefined	he resul	t of the o	peration.	0 = 1 =	= Re = Se	eset et to	to 1	0			

Table 115. eZ8 CPU Instruction Summary (Continued)

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										,						
	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0	1.1 BRK	2.2 SRP	2.3 ADD	2.4 ADD	3.3 ADD	3.4 ADD	3.3 ADD	3.4 ADD	4.3 ADDX	4.3 ADDX	2.3 DJNZ	2.2 JR	2.2 LD	3.2 JP	1.2 INC	1.2 NOP
		IM	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1	r1,X	cc,X	r1,IM	cc,DA	r1	
1	2.2 RLC R1	2.3 RLC IR1	2.3 ADC r1 r2	2.4 ADC r1 lr2	3.3 ADC B2 B1	3.4 ADC	3.3 ADC R1 IM	3.4 ADC	4.3 ADCX FR2 FR1	4.3 ADCX						See 2nd Opcode Map
2	2.2 INC	2.3 INC	2.3 SUB	2.4 SUB	3.3 SUB	3.4 SUB	3.3 SUB	3.4 SUB	4.3 SUBX	4.3 SUBX						1, 2 ATM
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
3	2.2 DEC	2.3 DEC	2.3 SBC r1 r2	2.4 SBC	3.3 SBC R2 R1	3.4 SBC	3.3 SBC R1 IM	3.4 SBC	4.3 SBCX	4.3 SBCX						
4	2.2 DA	2.3 DA	2.3 OR	2.4 OR	3.3 OR	3.4 OR	3.3 OR	3.4 OR	4.3 ORX	4.3 ORX						
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
5	2.2 POP	2.3 POP	2.3 AND	2.4 AND	3.3 AND	3.4 AND	3.3 AND	3.4 AND	4.3 ANDX	4.3 ANDX						1.2 WDT
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
6	2.2 COM	2.3 COM	2.3 TCM	2.4 TCM	3.3 TCM	3.4 TCM	3.3 TCM	3.4 TCM	4.3 TCMX	4.3 TCMX						1.2 STOP
0	R1	IR1	r1.r2	r1.lr2	R2.R1	IR2.R1	R1.IM	IR1.IM	ER2.ER1	IM.ER1						0101
7	2.2 PUSH	2.3 PUSH	2.3 TM	2.4 TM	3.3 TM	3.4 TM	3.3 TM	3.4 TM	4.3 TMX	4.3 TMX						1.2 HALT
	R2	IR2	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
8	2.5 DECW	2.6 DECW	2.5 LDE	2.9 LDEI	3.2 LDX	3.3 LDX	3.4 LDX	3.5 LDX	3.4 LDX	3.4 LDX						1.2 DI
	22		2.5	2.0	11,ERZ	111,ER2	2.4	2.5	2.2	2.5						1.2
9	R1	2.3 RL IR1	LDE r2,lrr1	LDEI Ir2,Irr1	LDX r2,ER1	LDX Ir2,ER1	LDX R2,IRR1	LDX IR2,IRR1	LEA r1,r2,X	LEA rr1,rr2,X						EI
А	2.5 INCW	2.6 INCW	2.3 CP	2.4 CP	3.3 CP	3.4 CP	3.3 CP	3.4 CP	4.3 CPX	4.3 CPX						1.4 RET
	RR1	IRR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
В	2.2 CLR	2.3 CLR	2.3 XOR	2.4 XOR	3.3 XOR	3.4 XOR	3.3 XOR	3.4 XOR	4.3 XORX	4.3 XORX						1.5 IRET
	22	23	2.5	29	23	29	151,110	3.4	3.2	wi,∟i×1						12
С	RRC R1	RRC IR1	LDC	LDCI	JP IRR1	LDC		LD r1.r2.X	PUSHX ER2							RCF
	2.2	2.3	2.5	2.9	2.6	2.2	3.3	3.4	3.2							1.2
D	SRA	SRA	LDC	LDCI		BSWAP			POPX							SCF
	22	23	22	23	3.2	33	32	33	42	42						12
Е	RR	RR	BIT	LD	LD	LD	LD	LD	LDX	LDX						CCF
-	R1	IR1	p,b,r1	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
F	2.2 SWAP	2.3 SWAP	2.6 TRAP	2.3 LD	2.8 MULT	3.3 LD	3.3 BTJ	3.4 BTJ				♦				

Figure 27. First Opcode Map

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Upper Nibble (Hex)

Table 117. Absolute Maximum Ratings (Continued)

Parameter	Minimum Maximum	Units	Notes
Maximum current into V_{DD} or out of V_{SS}	125	mA	

Operating temperature is specified in DC Characteristics.

- This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.
- This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

DC Characteristics

Table 118 lists the DC characteristics of the Z8 Encore! $XP^{\ensuremath{\mathbb{R}}}$ F0823 Series products. All voltages are referenced to V_{SS}, the primary system ground.

Table 118. DC Characteristics

		T _A = -40 °C to +105 °C (unless otherwise specified)		T _A = -40 °C to +105 °C (unless otherwise specified)		T _A = -40 °C to +105 °C (unless otherwise specified)			
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions			
V _{DD}	Supply Voltage	2.7	-	3.6	V				
V _{IL1}	Low Level Input Voltage	-0.3	_	0.3*V _{DD}	V				
V _{IH1}	High Level Input Voltage	0.7*V _{DD}	_	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.			
V _{IH2}	High Level Input Voltage	0.7*V _{DD}	_	V _{DD} +0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.			
V _{OL1}	Low Level Output Voltage	-	-	0.4	V	I _{OL} = 2 mA; V _{DD} = 3.0 V High Output Drive disabled.			
V _{OH1}	High Level Output Voltage	2.4	-	-	V	I _{OH} = -2 mA; V _{DD} = 3.0 V High Output Drive disabled.			
V _{OL2}	Low Level Output Voltage	-	-	0.6	V	I _{OL} = 20 mA; V _{DD} = 3.3 V High Output Drive enabled.			

Table 125. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V _{DD} T _A = (unless	= 3.0 V to 0 °C to + otherwis	3.6 V 70 °C e stated)			
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions	
Zin	Input Impedance	-	150		kΩ	In unbuffered mode at 20 MHz ⁵	
Vin	Input Voltage Range	0		V _{DD}	V	Unbuffered Mode	

Notes

1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.

Devices are factory calibrated at V_{DD} = 3.3 V and T_A = +30 °C, so the ADC is maximally accurate under these conditions.

3. LSBs are defined assuming 10-bit resolution.

4. This is the maximum recommended resistance seen by the ADC input pin.

5. The input impedance is inversely proportional to the system clock frequency.

Table 126.	Comparator	Electrical	Characteristics
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		V _{DD} = 2.7 V to 3.6 V T _A = -40 °C to +105 °C				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
V _{OS}	Input DC Offset		5		mV	
V _{CREF} Progi Refei	Programmable Internal Reference Voltage		<u>+</u> 5		%	20-/28-pin devices
			<u>+</u> 3		%	8-pin devices
T _{PROP}	Propagation Delay		200		ns	
V _{HYS}	Input Hysteresis		4		mV	
V _{IN}	Input Voltage Range	V _{SS}		V _{DD} -1	V	

General Purpose I/O Port Input Data Sample Timing

Figure 29 displays timing of the GPIO Port input sampling. The input value on a GPIO Port pin is sampled on the rising edge of the system clock. The Port value is available to the eZ8 CPU on the second rising clock edge following the change of the Port value.

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Packaging

Figure 34 displays the 8-pin Plastic Dual Inline Package (PDIP) available for the Z8 Encore! $XP^{\textcircled{R}}$ F0823 Series devices.



Figure 34. 8-Pin Plastic Dual Inline Package (PDIP)

Figure 40 displays the 28-pin Plastic Dual Inline Package (PDIP) available for Z8 Encore! XP F0823 Series devices.



Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 40. 28-Pin Plastic Dual Inline Package (PDIP)

Number	٤	_	ines	rupts	it Timers VM	it A/D Channels	t with IrDA	cription
Part	Flas	RAN	101	Inter	16-B w/P\	10-B	UAR	Des
Z8 Encore! XP with 1 KB Flash								
Standard Temperature: 0 °C to 70 °C								
Z8F0113PB005SC	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005SC	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005SC	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005SC	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005SC	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005SC	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005SC	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005SC	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005SC	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C								
Z8F0113PB005EC	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005EC	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005EC	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005EC	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005EC	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005EC	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005EC	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005EC	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005EC	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

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