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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0123sb005sc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 3.	Signal	Descriptions	(Continued)	
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Signal Mnemonic	I/O	Description				
Analog						
ANA[7:0]	Ι	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.				
VREF	I/O	Analog-to-Digital Converter reference voltage input.				
Clock Input						
CLKIN	I	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.				
LED Drivers						
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.				
On-Chip Debugger						
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD.				
		Caution: The DBG pin is open-drain and requires an external pull- up resistor to ensure proper operation.				
Reset						
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.				
Power Supply						
V _{DD}	Ι	Digital Power Supply.				
AV _{DD}	I	Analog Power Supply.				
V _{SS}	I	Digital Ground.				
AV _{SS}	Ι	Analog Ground.				
Note: The AV _{DD} and A PB7 on 28-pin pa	.V _{SS} sigr ackages	nals are available only in 28-pin packages with ADC. They are replaced by PB6 and without ADC.				

Pin Characteristics

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

Z8 Encore! XP[®] F0823 Series Product Specification

Priority	Program Memory Vector Address	Interrupt or Trap Source
Lowest	0036H	Port C Pin 0, both input edges
	0038H	Reserved

Table 33. Trap and Interrupt Vectors in Order of Priority (Continued)

Architecture

Figure 8 displays the interrupt controller block diagram.



Figure 8. Interrupt Controller Block Diagram

Operation

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control register globally enables and disables interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an Enable Interrupt (EI) instruction
- Execution of an Return from Interrupt (IRET) instruction

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR		FC6H						

Table 36. Interrupt Request 2 Register (IRQ2)

Reserved—Must be 0

PCxI—Port C Pin x Interrupt Request

0 = No interrupt request is pending for GPIO Port C pin x

1 = An interrupt request from GPIO Port C pin x is awaiting service

where x indicates the specific GPIO Port C pin number (0-3)

IRQ0 Enable High and Low Bit Registers

Table 37 describes the priority control for IRQ0. The IRQ0 Enable High and Low Bit registers (Table 38 and Table 39) form a priority encoded enabling for interrupts in the Interrupt Request 0 register. Priority is generated by setting bits in each register.

Table 37.	IRQ0	Enable	and	Priority	/ Encoding
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IRQ0ENL[x]	Priority	Description
0	Disabled	Disabled
1	Level 1	Low
0	Level 2	Nominal
1	Level 3	High
	IRQ0ENL[x] 0 1 0 1	IRQ0ENL[x] Priority 0 Disabled 1 Level 1 0 Level 2 1 Level 3

where x indicates the register bits from 0–7.

Table 38. IRQ0 Enable High Bit Register (IRQ0ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1ENH	T0ENH	U0RENH	U0TENH	Reserved	Reserved	ADCENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR		FC1H						

COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin Timer Input alternate function. The TPOL bit in the Timer Control register selects whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER mode, the prescaler is disabled.

Caution: The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Follow the steps below for configuring a timer for COUNTER mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COUNTER mode.
 - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER mode. After the first timer Reload in COUNTER mode, counting always begins at the reset value of 0001H. In COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value – Start Value

COMPARATOR COUNTER Mode

In COMPARATOR COUNTER mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPARATOR COUNTER mode, the prescaler is disabled.

Caution: *The frequency of the comparator output signal must not exceed one-fourth the system clock frequency.*

After reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Follow the steps below for configuring a timer for COMPARATOR COUNTER mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARATOR COUNTER mode.
 - Select either the rising edge or falling edge of the comparator output signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This action only affects the first pass in COMPARATOR COUNTER mode. After the first timer Reload in COMPARATOR COUNTER mode, counting always begins at the reset value of 0001H. Generally, in COMPARATOR COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer.

In COMPARATOR COUNTER mode, the number of comparator output transitions since the timer start is given by the following equation:

Comparator Output Transitions = Current Count Value – Start Value

- Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the PWM Control register to set the PWM dead band delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM high and low byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
- 5. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
- 6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 7. Configure the associated GPIO port pin for the Timer Output and Timer Output Complement alternate functions. The Timer Output Complement function is shared with the Timer Input function for both timers. Setting the timer mode to Dual PWM automatically switches the function from Timer In to Timer Out Complement.
- 8. Write to the Timer Control register to enable the timer and initiate counting.

The PWM period is represented by the following equation: $PWM \text{ Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT mode equation determines the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{PWM Value}{Reload Value} \times 100$

CAPTURE Mode

In CAPTURE mode, the current timer count value is recorded when the appropriate external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge

Flash Operation Timing Using the Flash Frequency Registers

Before performing either a program or erase operation on Flash memory, you must first configure the Flash Frequency High and Low Byte registers. The Flash Frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 32 kHz (32768 Hz) through 20 MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

FFREQ[15:0] = System Clock Frequency (Hz) 1000

Caution: Flash programming and erasure are not supported for system clock frequencies below 32 kHz (32768 Hz) or above 20 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of Z8 Encore! XP[®] F0823 Series devices.

Flash Code Protection Against External Access

The user code contained within the Flash memory can be protected against external access with the On-Chip Debugger. Programming the FRP Flash Option Bit prevents reading of the user code with the On-Chip Debugger. For more information, see Flash Option Bits on page 141 and On-Chip Debugger on page 151.

Flash Code Protection Against Accidental Program and Erasure

Z8 Encore! XP F0823 Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash Option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

Flash Code Protection Using the Flash Option Bits

The FRP and FWP Flash Option Bits combine to provide three levels of Flash Program Memory protection as listed in Table 78. For more information, see Flash Option Bits on page 141.

a bit of the Sector Protect Register has been set, it cannot be cleared except by powering down the device.

Byte Programming

The Flash Memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either Mass Erase or Page Erase. When the Flash Controller is unlocked and Mass Erase is successfully completed, all Program Memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and Page Erase is successfully enabled, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the Page Erase or Mass Erase commands.

Byte Programming is accomplished using the On-Chip Debugger's Write Memory command or eZ8 CPU execution of the LDC or LDCI instructions. For a description of the LDC and LDCI instructions, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at <u>www.zilog.com</u>. While the Flash Controller programs the Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control register, except the Mass Erase or Page Erase commands.

Caution: The byte at each address of the Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs. Doing so may result in corrupted data at the target byte.

Page Erase

The Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value FFH. The Flash Page Select register identifies the page to be erased. Only a page residing in an unprotected sector can be erased. With the Flash Controller unlocked and the active page set, writing the value 95h to the Flash Control register initiates the Page Erase operation. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. If the Page Erase operation is performed using the On-Chip Debugger, poll the Flash Status register to determine when the Page Erase operation is complete. When the Page Erase is complete, the Flash Controller returns to its locked state.

Mass Erase

The Flash memory can also be Mass Erased using the Flash Controller, but only by using the On-Chip Debugger. Mass Erasing the Flash memory sets all bytes to the value FFH. With the Flash Controller unlocked and the Mass Erase successfully enabled, writing the

configurations. The information contained here is lost when page 0 of the Program Memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in Flash Information Area on page 15

Serialization Bits

As an optional feature, Zilog[®] is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (for more details, see Reading the Flash Information Page on page 143 and Serialization Data on page 148) and are unaffected by mass erasure of the device's Flash memory.

Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

Note:

Flash Option Bits

Watchdog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Reserved—R/W bits must be 1 during writes; 1 when read.

VBO AO-Voltage Brownout Protection Always ON

0 = Voltage Brownout Protection can be disabled in STOP mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see Power Control Register 0 on page 32).

1 = Voltage Brownout Protection is always enabled including during STOP mode. This setting is the default for unprogrammed (erased) Flash.

FRP—Flash Read Protect

0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger.

1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.

Reserved-Must be 1

FWP—Flash Write Protect

This Option Bit provides Flash Program Memory protection:

0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase, and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger.

1 = Programming, Page Erase, and Mass Erase are enabled for all of Flash program memory.

Flash Program Memory Address 0001H

Table 88. Flash Options Bits at Program Memory Address 0001H

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0001H							
Noto: II -	Note: Up Lipphongod by Popot D/M = Popd/Mrite							

Note: U = Unchanged by Reset. R/W = Read/Write.

Reserved—R/W must be 1 during writes; 1 when read

XTLDIS—State of Crystal Oscillator at Reset

Table 95. Serialization Data Locations

Info Page Address	Memory Address	Usage
1C	FE1C	Serial Number Byte 3 (most significant)
1D	FE1D	Serial Number Byte 2
1E	FE1E	Serial Number Byte 1
1F	FE1F	Serial Number Byte 0 (least significant)

Randomized Lot Identifier

Table 96. Lot Identification Number (RAND_LOT)

BITS	7	6	5	4	3	2	1	0
FIELD	RAND_LOT							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	ADDR Interspersed throughout Information Page Memory							
Note: U = Unchanged by Reset. R/W = Read/Write.								

RAND LOT-Randomized Lot ID

The randomized lot ID is a 32 byte binary value that changes for each production lot.

Table 97. Randomized Lot ID Locations

Info Page Address	Memory Address	Usage
3C	FE3C	Randomized Lot ID Byte 31 (most significant)
3D	FE3D	Randomized Lot ID Byte 30
3E	FE3E	Randomized Lot ID Byte 29
3F	FE3F	Randomized Lot ID Byte 28
58	FE58	Randomized Lot ID Byte 27
59	FE59	Randomized Lot ID Byte 26
5A	FE5A	Randomized Lot ID Byte 25
5B	FE5B	Randomized Lot ID Byte 24

OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

- 1. Hold PA2/RESET Low.
- 2. Wait 5 ms for the internal reset sequence to complete.
- 3. Send the following bytes serially to the debug pin:

```
DBG \leftarrow 80H (autobaud)
DBG \leftarrow EBH
DBG \leftarrow 5AH
DBG \leftarrow 70H
DBG \leftarrow CDH (32-bit unlock key)
```

4. Release PA2/RESET. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20- or 28-pin device. To enter DEBUG mode, re-autobaud and write 80H to the OCD control register (see On-Chip Debugger Commands on page 157).

Breakpoints

Execution breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the OCD. If breakpoints are enabled, the OCD enters DEBUG mode and idles the eZ8 CPU. If breakpoints are not enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The OCD contains a 16-bit Runtime Counter. It counts system clock cycles between breakpoints. The counter starts counting when the OCD leaves DEBUG mode and stops counting when it enters DEBUG mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the OCD by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of Z8 Encore! XP[®] F0823 Series products. When this option is enabled, several of the OCD commands are disabled. Table 99 on page 162 is a summary of the OCD commands. Each OCD command is described in further detail in the bulleted list following this table. Table 99 on page 162 also indicates those commands that operate when the device is not in DEBUG mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	-
Reserved	01H	_	_
Read OCD Status Register	02H	Yes	-
Read Runtime Counter	03H	_	-
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	-
Write Program Counter	06H	-	Disabled.
Read Program Counter	07H	-	Disabled.
Write Register	08H	_	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	-	Disabled.
Write Program Memory	0AH	_	Disabled.
Read Program Memory	0BH	_	Disabled.
Write Data Memory	0CH	_	Yes.
Read Data Memory	0DH	-	_
Read Program Memory CRC	OEH	-	-
Reserved	0FH	-	-
Step Instruction	10H	_	Disabled.

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Table 112. Logical Instructions (Continued)

Mnemonic	Operands	Instruction
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 113. Program Control Instructions

Mnemonic	Operands	Instruction							
BRK	_	On-Chip Debugger Break							
BTJ	p, bit, src, DA	Bit Test and Jump							
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero							
BTJZ	bit, src, DA	Bit Test and Jump if Zero							
CALL	dst	Call Procedure							
DJNZ	dst, src, RA	Decrement and Jump Non-Zero							
IRET	_	Interrupt Return							
JP	dst	Jump							
JP cc	dst	Jump Conditional							
JR	DA	Jump Relative							
JR cc	DA	Jump Relative Conditional							
RET	_	Return							
TRAP	vector	Software Trap							

Table 114. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry

Table 114. Rotate and Shift Instructions	(Continued)
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Mnemonic	Operands	Instruction
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

eZ8 CPU Instruction Summary

Table 115 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch, and the number of CPU clock cycles required for the instruction.

Assombly		Addre	ss Mode	Oncode(s)	Fla	igs			Fotch	Instr		
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	z	S	v	D	Н	Cycles	Cycles
ADC dst, src	$dst \gets dst + src + C$	r	r	12	*	*	*	*	0	*	2	3
		r	lr	13	-						2	4
		R	R	14	-						3	3
		R	IR	15	-						3	4
		R	IM	16	_						3	3
		IR	IM	17	-						3	4
ADCX dst, src	$dst \gets dst + src + C$	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19	-						4	3
ADD dst, src	$dst \gets dst + src$	r	r	02	*	*	*	*	0	*	2	3
		r	lr	03	-						2	4
		R	R	04	-						3	3
		R	IR	05	-						3	4
		R	IM	06	-						3	3
		IR	IM	07	-						3	4
ADDX dst, src	$dst \gets dst + src$	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09	-						4	3
Flags Notation:	* = Value is a function o – = Unaffected X = Undefined	f the resu	It of the o	peration.	0 = 1 =	= Re = Se	eset et to	to 1	0			

Table 115. eZ8 CPU Instruction Summary

• · · · · · · · · · ·		Address Mode			Flags						E. ()	Instr
Assembly Mnemonic	Symbolic Operation	dst	src	- Opcode(s) (Hex)	С	z	S	v	D	Н	- Fetch Cycles	Instr. Cycles
RR dst		R		E0	*	*	*	*	-	_	2	2
	► D7 D6 D5 D4 D3 D2 D1 D0 ► C	IR		E1							2	3
RRC dst		R		C0	*	*	*	*	_	_	2	2
	► D7 D6 D5 D4 D3 D2 D1 D0 ► C dst	IR		C1	-						2	3
SBC dst, src	dst ← dst – src - C	r	r	32	*	*	*	*	1	*	2	3
		r	lr	33	-						2	4
		R	R	34	-						3	3
		R	IR	35	-						3	4
		R	IM	36	-						3	3
		IR	IM	37	-						3	4
SBCX dst, src	$dst \gets dst - src - C$	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39	-						4	3
SCF	C ← 1			DF	1	_	_	_	_	-	1	2
SRA dst		R		D0	*	*	*	0	_	_	2	2
		IR		D1	-						2	3
SRL dst	0 - D7 D6 D5 D4 D3 D2 D1 D0 D C	R		1F C0	*	*	0	*	_	_	3	2
	dst	IR		1F C1	_						3	3
SRP src	$RP \leftarrow src$		IM	01	_	_	_	_	-	-	2	2
STOP	STOP Mode			6F	_	_	-	_	-	_	1	2
SUB dst, src	$dst \gets dst - src$	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23	-						2	4
		R	R	24	-						3	3
		R	IR	25	-						3	4
		R	IM	26	-						3	3
		IR	IM	27	-						3	4
Flags Notation:	* = Value is a function of t – = Unaffected X = Undefined	he resu	It of the o	peration.	0 = 1 =	= Re = Se	eset et to	to 1	0			

Table 115. eZ8 CPU Instruction Summary (Continued)

Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 26. Figure 27 and Figure 28 provide information about each of the eZ8 CPU instructions. Table 116 lists Opcode Map abbreviations.



Figure 26. Opcode Map Cell Description

On-Chip Debugger Timing

Figure 31 and Table 129 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 ns maximum rise and fall time.



		Dela	y (ns)
Parameter	Abbreviation	Minimum	Maximum
DBG			
T ₁	XIN Rise to DBG Valid Delay	_	15
T ₂	XIN Rise to DBG Output Hold Time	2	_
T ₃	DBG to XIN Rise Input Setup Time	5	-
T ₄	DBG to XIN Rise Input Hold Time	5	-

Table 129. On-Chip Debugger Timing

er					ers	Channels	IrDA	E
Part Numb	Flash	RAM	I/O Lines	Interrupts	16-Bit Tim w/PWM	10-Bit A/D	UART with	Descriptio
Z8 Encore! XP with 2	KB Flash							
Standard Temperature	e: 0 °C to	70 °C						
Z8F0213PB005SC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005SC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005SC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005SC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005SC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005SC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005SC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005SC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005SC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
Extended Temperatur	e: -40 °C	to 105 °C	2					
Z8F0213PB005EC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005EC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005EC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005EC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005EC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005EC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005EC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005EC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005EC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead	d-Free Pac	kaging						