



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0213hj005ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	07
Receiving Data using the Interrupt Driven Method	. 97
Clear To Sond (CTS) Operation	. 98
	. 99
	101
	101
	103
	100
	104
	104
UART Status 0 Register	105
UART Status 1 Register	106
UART Control 0 and Control 1 Registers	107
UART Address Compare Register	109
UART Baud Rate High and Low Byte Registers	110
Infrared Encoder/Decoder	113
Architecture	113
Operation	113
Transmitting IrDA Data	114
Receiving IrDA Data	115
Infrared Encoder/Decoder Control Register Definitions	116
Analog-to-Digital Converter	447
	117
Architecture	117 117
Architecture	117 117 118
Architecture	117 117 118 118
Architecture Operation Operation Data Format Automatic Powerdown Operation	117117118118119
Architecture Operation Operation Data Format Automatic Powerdown Single-Shot Conversion	 117 117 118 118 119 119 119
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion	 117 117 118 118 119 119 120
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts	117 117 118 118 119 119 120 121
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation	 117 117 118 118 119 119 120 121 121
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions	 117 117 118 118 119 119 120 121 121 122
Architecture Operation Operation Data Format Data Format Automatic Powerdown Single-Shot Conversion Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 Operation	 117 117 118 118 119 119 120 121 121 122 122 122
Architecture Operation Operation Data Format Automatic Powerdown Single-Shot Conversion Single-Shot Conversion Continuous Conversion Interrupts Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1	 117 117 118 118 119 119 120 121 121 122 122 124
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1 ADC Data High Byte Register	 117 117 118 118 119 120 121 121 122 122 122 124 124
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1 ADC Data High Byte Register ADC Data Low Bits Register	 117 117 118 118 119 119 120 121 121 122 122 122 124 125
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1 ADC Data High Byte Register ADC Data Low Bits Register	117 117 118 118 119 120 121 121 122 122 122 124 124 125 127
Architecture Operation Data Format Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1 ADC Data High Byte Register ADC Data Low Bits Register Operation	117 117 118 118 119 120 121 121 122 122 122 122 124 124 125 127
Architecture Operation Data Format Automatic Powerdown Single-Shot Conversion Continuous Conversion Interrupts Calibration and Compensation ADC Control Register Definitions ADC Control Register 0 ADC Control/Status Register 1 ADC Data High Byte Register ADC Data Low Bits Register Comparator Operation Comparator Control Register Definitions	117 117 118 118 119 120 121 121 122 122 122 124 125 127 127

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.



Figure 2. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 8-Pin SOIC, QFN/MLF-S, or PDIP Package*



Figure 3. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 20-Pin SOIC, SSOP or PDIP Package*



Figure 4. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 28-Pin SOIC, SSOP or PDIP Package*

	Program Memory	
Priority	Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer on page 87)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Timer Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3 or Port D Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2 or Port D Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges

Table 33. Trap and Interrupt Vectors in Order of Priority

BITS	7	6	5	4	3	2	1	0			
FIELD	IRQE	Reserved									
RESET	0	0	0 0 0 0 0 0 0								
R/W	R/W	R	R	R	R	R	R	R			
ADDR			FCFH								

Table 48. Interrupt Control Register (IRQCTL)

IRQE—Interrupt Request Enable

This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, reset or by a direct register write of a 0 to this bit.

0 = Interrupts are disabled

1 =Interrupts are enabled

Reserved—0 when read

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT mode equation to determine the first PWM time-out period. If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by the following equation:

PWM Output High Time Ratio (%) = $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by the following equation:

PWM Output High Time Ratio (%) = $\frac{PWM \text{ Value}}{\text{Reload Value}} \times 100$

PWM Dual Output Mode

In PWM DUAL OUTPUT mode, the timer outputs a PWM output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

Follow the steps below for configuring a timer for PWM Dual Output mode and initiating the PWM operation:

- 1. Write to the Timer Control register to:
 - Disable the timer
 - Configure the timer for PWM Dual Output mode. Setting the mode also involves writing to TMODEHI bit in TxCTL1 register
 - Set the prescale value

of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in TxCTL1 register is set to indicate the timer interrupt is because of an input capture event.

The timer continues counting up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt and continues counting. The INPCAP bit in TxCTL1 register clears indicating the timer interrupt is not because of an input capture event.

Follow the steps below for configuring a timer for CAPTURE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer
 - Configure the timer for CAPTURE mode
 - Set the prescale value
 - Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a Capture or a Reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
- 5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

CAPTURE RESTART Mode

In CAPTURE RESTART mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is

86

010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128

TMODE—Timer mode

This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value.

0000 = ONE-SHOT mode

0001 = CONTINUOUS mode

0010 = COUNTER mode

- 0011 = PWM SINGLE OUTPUT mode
- 0100 = CAPTURE mode
- 0101 = COMPARE mode
- 0110 = GATED mode
- 0111 = CAPTURE/COMPARE mode
- 1000 = PWM DUAL OUTPUT mode
- 1001 = CAPTURE RESTART mode
- 1010 = COMPARATOR COUNTER Mode

received and the UART Receive Data register has not been read. If the RDA bit is reset to 0, reading the UART Receive Data register clears this bit.

0 = No overrun error occurred

1 = An overrun error occurred

FE—Framing Error

This bit indicates that a framing error (no Stop bit following data reception) was detected. Reading the UART Receive Data register clears this bit.

0 = No framing error occurred

1 = A framing error occurred

BRKD-Break Detect

This bit indicates that a break occurred. If the data bits, parity/multiprocessor bit, and Stop bit(s) are all 0s this bit is set to 1. Reading the UART Receive Data register clears this bit.

0 = No break occurred

1 = A break occurred

TDRE—Transmitter Data Register Empty

This bit indicates that the UART Transmit Data register is empty and ready for additional data. Writing to the UART Transmit Data register resets this bit.

0 = Do not write to the UART Transmit Data register

1 = The UART Transmit Data register is ready to receive an additional byte to be transmitted

TXE—Transmitter Empty

This bit indicates that the transmit shift register is empty and character transmission is finished.

0 = Data is currently transmitting

1 = Transmission is complete

$CTS \longrightarrow \overline{CTS}$ signal

When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low.

UART Status 1 Register

This register contains multiprocessor control and status bits.

Table 65. UART Status 1 Register (U0STAT1)

BITS	7	6	5	4	3	2	1	0		
FIELD	Reserved NEWFRM MPR									
RESET	0	0	0	0	0	0	0	0		
R/W	R	R	R	R	R/W	R/W	R	R		
ADDR	F44H									

Comparator

Z8 Encore! XP[®] F0823 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The features of Comparator include:

- Two inputs which can be connected up using the GPIO multiplex (MUX)
- One input can be connected to a programmable internal reference
- One input can be connected to the on-chip temperature sensor
- Output can be either an interrupt source or an output to an external pin

Operation

One of the comparator inputs can be connected to an internal reference which is a user selectable reference that is user programmable with 200 mV resolution.

The comparator can be powered down to save on supply current. For details, see Power Control Register 0 on page 32.

Caution: Because of the propagation delay of the comparator, it is not recommended to enable the comparator without first disabling interrupts and waiting for the comparator output to settle. Doing so can result in spurious interrupts after comparator enabling. The following example shows how to safely enable the comparator:

```
di
ld cmp0
nop
   ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei
```

Comparator Control Register Definitions

Comparator Control Register

The Comparator Control register (CMPCTL) configures the comparator inputs and sets the value of the internal voltage reference.

Z8 Encore! XP[®] F0823 Series Product Specification

132



Figure 21. Flash Controller Operation Flowchart

Table 78 Flash Code	Protection Usin	a the Flash O	ntion Bits
		y life i lasti O	

FWP	Flash Code Protection Description
0	Programming and erasing disabled for all of Flash Program Memory. In user code programming, Page Erase, and Mass Erase are all disabled. Mass Erase is available through the On-Chip Debugger.
1	Programming, Page Erase, and Mass Erase are enabled for all of Flash Program Memory.

Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the same page previously stored there. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. For more details, see Figure 21.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

Sector Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! XP devices are divided into maximum number of 8 sectors. A sector is 1/8 of the total size of the Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal.

The Sector Protect Register controls the protection state of each Flash sector. This register is shared with the Page Select Register. It is accessed by writing 73H followed by 5EH to the Flash controller. The next write to the Flash Control Register targets the Sector Protect Register.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector can no longer be written or erased by the CPU. External Flash programming through the OCD or via the Flash Controller Bypass mode are unaffected. After

142

configurations. The information contained here is lost when page 0 of the Program Memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in Flash Information Area on page 15

Serialization Bits

As an optional feature, Zilog[®] is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (for more details, see Reading the Flash Information Page on page 143 and Serialization Data on page 148) and are unaffected by mass erasure of the device's Flash memory.

Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

Note:

Trim Bit Data Register

The Trim Bid Data (TRMDR) register contains the read or write data for access to the trim option bits.

Table 86. Trim Bit Data Register (TRMDR)

BITS	7	6	5	4	3	2	1	0				
FIELD	TRMDR - Trim Bit Data											
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W R/W R/W						
ADDR				FF	7H							

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

Flash Program Memory Address 0000H

 Table 87. Flash Option Bits at Program Memory Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	WDT_RES	WDT_AO	Rese	erved	VBO_AO	FRP	Reserved	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				Program Me	mory 0000H			
Note: U =	Unchanged b	y Reset. R/W	= Read/Write).				

WDT RES—Watchdog Timer Reset

0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.

1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watchdog Timer Always ON

0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled.

1 = Watchdog Timer is enabled upon execution of the WDT instruction. Once enabled, the

is not in DEBUG mode or if the Flash Read Protect Option bit is enabled, the data is discarded.

DBG \leftarrow 0AH DBG \leftarrow Program Memory Address[15:8] DBG \leftarrow Program Memory Address[7:0] DBG \leftarrow Size[15:8] DBG \leftarrow Size[7:0] DBG \leftarrow 1-65536 data bytes

• **Read Program Memory (0BH)**—The Read Program Memory command reads data from Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG mode or if the Flash Read Protect Option Bit is enabled, this command returns FFH for the data.

```
DBG \leftarrow 0BH

DBG \leftarrow Program Memory Address[15:8]

DBG \leftarrow Program Memory Address[7:0]

DBG \leftarrow Size[15:8]

DBG \leftarrow Size[7:0]

DBG \rightarrow 1-65536 data bytes
```

• Write Data Memory (0CH)—The Write Data Memory command writes data to Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). If the device is not in DEBUG mode or if the Flash Read Protect Option Bit is enabled, the data is discarded.

```
DBG \leftarrow 0CH
DBG \leftarrow Data Memory Address[15:8]
DBG \leftarrow Data Memory Address[7:0]
DBG \leftarrow Size[15:8]
DBG \leftarrow Size[7:0]
DBG \leftarrow 1-65536 data bytes
```

• **Read Data Memory (0DH)**—The Read Data Memory command reads from Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be read 1 to 65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG mode, this command returns FFH for the data.

```
DBG \leftarrow 0DH
DBG \leftarrow Data Memory Address[15:8]
DBG \leftarrow Data Memory Address[7:0]
DBG \leftarrow Size[15:8]
DBG \leftarrow Size[7:0]
DBG \rightarrow 1-65536 data bytes
```

Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a non-standard frequency or use the automatic factory-trimmed version to achieve a 5.53 MHz frequency. The features of IPO include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53 MHz or 32.8 kHz (contains both a fast and a slow mode)
- Trimming possible through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53 MHz (fast mode) or 32.8 kHz (slow mode) is required. This trimming is done at +30 °C and a supply voltage of 3.3 V, so accuracy of this operating point is optimal.

Power down this block for minimum system power. By default, the oscillator is configured through the Flash Option bits. However, the user code can override these trim values as described in Trim Bit Address Space on page 146.

Select one of the two frequencies for the oscillator: 5.53 MHz and 32.8 kHz, using the OSCSEL bits in the Oscillator Control on page 165.

Assembly Language Syntax

For proper instruction execution, eZ8 CPU assembly language syntax requires that the operands be written as 'destination, source'. After assembly, the object code usually has the operands in the order 'source, destination', but ordering is opcode-dependent. The following instruction examples illustrate the format of some basic assembly instructions and the resulting object code produced by the assembler. You must follow this binary format if you prefer manual program coding or intend to implement your own assembler.

Example 1

If the contents of Registers 43H and 08H are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 103. Assembly Language Syntax Example 1

Assembly Language Code	ADD	43н,	08H	(ADD	dst,	src)
Object Code	04	08	43	(OPC	src,	dst)

Example 2

In general, when an instruction format requires an 8-bit register address, that address can specify any register location in the range 0–255 or, using Escaped Mode Addressing, a Working Register R0–R15. If the contents of Register 43H and Working Register R8 are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 104. Assembly Language Syntax Example 2

Assembly Language Code	ADD	43H,	R8	(ADD dst, sr	C)
Object Code	04	E8	43	(OPC src, ds	t)

See the device-specific Product Specification to determine the exact register file range available. The register file size varies, depending on the device type.

eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags, and address modes are represented by a notational shorthand that is described in Table 105.

Z8 Encore! XP[®] F0823 Series Product Specification

										,						
	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0	1.1 BRK	2.2 SRP	2.3 ADD	2.4 ADD	3.3 ADD	3.4 ADD	3.3 ADD	3.4 ADD	4.3 ADDX	4.3 ADDX	2.3 DJNZ	2.2 JR	2.2 LD	3.2 JP	1.2 INC	1.2 NOP
		IM	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1	r1,X	cc,X	r1,IM	cc,DA	r1	
1	2.2 RLC R1	2.3 RLC IR1	2.3 ADC r1 r2	2.4 ADC r1 lr2	3.3 ADC B2 B1	3.4 ADC	3.3 ADC R1 IM	3.4 ADC	4.3 ADCX FR2 FR1	4.3 ADCX						See 2nd Opcode Map
2	2.2 INC	2.3 INC	2.3 SUB	2.4 SUB	3.3 SUB	3.4 SUB	3.3 SUB	3.4 SUB	4.3 SUBX	4.3 SUBX						1, 2 ATM
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
3	2.2 DEC	2.3 DEC	2.3 SBC r1 r2	2.4 SBC	3.3 SBC R2 R1	3.4 SBC	3.3 SBC R1 IM	3.4 SBC	4.3 SBCX	4.3 SBCX						
4	2.2 DA	2.3 DA	2.3 OR	2.4 OR	3.3 OR	3.4 OR	3.3 OR	3.4 OR	4.3 ORX	4.3 ORX						
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
5	2.2 POP	2.3 POP	2.3 AND	2.4 AND	3.3 AND	3.4 AND	3.3 AND	3.4 AND	4.3 ANDX	4.3 ANDX						1.2 WDT
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
6	2.2 COM	2.3 COM	2.3 TCM	2.4 TCM	3.3 TCM	3.4 TCM	3.3 TCM	3.4 TCM	4.3 TCMX	4.3 TCMX						1.2 STOP
0	R1	IR1	r1.r2	r1.lr2	R2.R1	IR2.R1	R1.IM	IR1.IM	ER2.ER1	IM.ER1						0101
7	2.2 PUSH	2.3 PUSH	2.3 TM	2.4 TM	3.3 TM	3.4 TM	3.3 TM	3.4 TM	4.3 TMX	4.3 TMX						1.2 HALT
	R2	IR2	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
8	2.5 DECW	2.6 DECW	2.5 LDE	2.9 LDEI	3.2 LDX	3.3 LDX	3.4 LDX	3.5 LDX	3.4 LDX	3.4 LDX						1.2 DI
	22		2.5	2.0	11,ERZ	111,ER2	2.4	2.5	2.2	2.5						1.2
9	R1	2.3 RL IR1	LDE r2,lrr1	LDEI Ir2,Irr1	LDX r2,ER1	LDX Ir2,ER1	LDX R2,IRR1	LDX IR2,IRR1	LEA r1,r2,X	LEA rr1,rr2,X						EI
А	2.5 INCW	2.6 INCW	2.3 CP	2.4 CP	3.3 CP	3.4 CP	3.3 CP	3.4 CP	4.3 CPX	4.3 CPX						1.4 RET
	RR1	IRR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
В	2.2 CLR	2.3 CLR	2.3 XOR	2.4 XOR	3.3 XOR	3.4 XOR	3.3 XOR	3.4 XOR	4.3 XORX	4.3 XORX						1.5 IRET
	22	23	2.5	29	23	29	151,110	3.4	3.2	wi,∟i×1						12
С	RRC R1	RRC IR1	LDC	LDCI	JP IRR1	LDC		LD r1.r2.X	PUSHX ER2							RCF
	2.2	2.3	2.5	2.9	2.6	2.2	3.3	3.4	3.2							1.2
D	SRA	SRA	LDC	LDCI		BSWAP			POPX							SCF
	22	23	22	23	3.2	33	32	33	42	42						12
Е	RR	RR	BIT	LD	LD	LD	LD	LD	LDX	LDX						CCF
-	R1	IR1	p,b,r1	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
F	2.2 SWAP	2.3 SWAP	2.6 TRAP	2.3 LD	2.8 MULT	3.3 LD	3.3 BTJ	3.4 BTJ				♦				

Figure 27. First Opcode Map

190

Upper Nibble (Hex)

Electrical Characteristics

The data in this chapter is pre-qualification and pre-characterization and is subject to change. Additional electrical characteristics may be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed in Table 117 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		220	mW	
Maximum current into V_{DD} or out of V_{SS}		60	mA	
20-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		430	mW	
Maximum current into V _{DD} or out of V _{SS}		120	mA	
28-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		450	mW	

Table 117. Absolute Maximum Ratings

UART Timing

Figure 32 and Table 130 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the transmit data register has been loaded with data prior to CTS assertion.



Figure 32. UART Timing With CTS

		Delay (ns)	
Parameter	Abbreviation	Minimum	Maximum
UART			
T ₁	CTS Fall to DE output delay	2 * XIN period	2 * XIN period + 1 bit time
T ₂	DE assertion to TXD falling edge (start bit) dela	ay ± 5	
T ₃	End of Stop Bit(s) to DE deassertion delay	± 5	

Table 130. UART Timing With CTS

Z8 Encore! XP[®] F0823 Series Product Specification

Index

Symbols

174 % 174 @ 174

Numerics

10-bit ADC 4 40-lead plastic dual-inline package 214, 215

Α

absolute maximum ratings 193 AC characteristics 197 ADC 175 architecture 117 automatic power-down 118 block diagram 118 continuous conversion 120 control register 122, 124 control register definitions 122 data high byte register 124 data low bits register 125 electrical characteristics and timing 201 operation 118 single-shot conversion 119 ADCCTL register 122, 124 ADCDH register 124 ADCDL register 125 ADCX 175 ADD 175 add - extended addressing 175 add with carry 175 add with carry - extended addressing 175 additional symbols 174 address space 13 ADDX 175 analog signals 10 analog-to-digital converter (ADC) 117 AND 177

ANDX 177 arithmetic instructions 175 assembly language programming 171 assembly language syntax 172

В

B 174 b 173 baud rate generator, UART 103 **BCLR 176** binary number suffix 174 **BIT 176** bit 173 clear 176 manipulation instructions 176 set 176 set or clear 176 swap 176 test and jump 178 test and jump if non-zero 178 test and jump if zero 178 bit jump and test if non-zero 178 bit swap 178 block diagram 3 block transfer instructions 176 **BRK 178 BSET 176** BSWAP 176, 178 **BTJ 178 BTJNZ 178 BTJZ 178**

С

CALL procedure 178 CAPTURE mode 84, 85 CAPTURE/COMPARE mode 85 cc 173 CCF 176 characteristics, electrical 193 clear 177 CLR 177 COM 177 227