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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0213pj005ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- 2.7 V to 3.6 V operating voltage
- Up to thirteen 5 V-tolerant input pins
- 8-, 20-, and 28-pin packages
- 0 °C to +70 °C and -40 °C to +105 °C for operating temperature ranges

# **Part Selection Guide**

Table 1 lists the basic features and package styles available for each device within the Z8 Encore! XP<sup>®</sup> F0823 Series product line.

Table 1.	Z8 Encore!	XP F0823	Series	Family	Part	Selection	Guide
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Part Number	Flash (KB)	RAM (B)	I/O	ADC Inputs	Packages
Z8F0823	8	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0813	8	1024	6–24	0	8-, 20-, and 28-pins
Z8F0423	4	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0413	4	1024	6–24	0	8-, 20-, and 28-pins
Z8F0223	2	512	6–22	4–8	8-, 20-, and 28-pins
Z8F0213	2	512	6–24	0	8-, 20-, and 28-pins
Z8F0123	1	256	6–22	4–8	8-, 20-, and 28-pins
Z8F0113	1	256	6–24	0	8-, 20-, and 28-pins

# **Reset Controller**

Z8 Encore!  $XP^{\mathbb{R}}$  F0823 Series products can be reset using the  $\overline{RESET}$  pin, POR, WDT time-out, STOP mode exit, or Voltage Brownout warning signal. The  $\overline{RESET}$  pin is bidirectional, that is, it functions as reset source as well as a reset indicator.

# **On-Chip Debugger**

Z8 Encore! XP F0823 Series products feature an integrated On-Chip Debugger. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

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# **Register Map**

Table 8 lists the address map for the Register File of the Z8 Encore! XP<sup>®</sup> F0823 Series devices. Not all devices and package styles in the Z8 Encore! XP F0823 Series support the ADC, or all GPIO ports. Consider registers for unimplemented peripherals as reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
General-Purpos	se RAM			
Z8F0823/Z8F08	13 Devices			
000–3FF	General-Purpose Register File RAM	_	XX	
400–EFF	Reserved		XX	
Z8F0423/Z8F04	13 Devices			
000–3FF	General-Purpose Register File RAM		XX	
400–EFF	Reserved	_	XX	
Z8F0223/Z8F02	13 Devices			
000–1FF	General-Purpose Register File RAM		XX	
200–EFF	Reserved		XX	
Z8F0123/Z8F01	13 Devices			
000–0FF	General-Purpose Register File RAM		XX	
100–EFF	Reserved		XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	80
F01	Timer 0 Low Byte	TOL	01	80
F02	Timer 0 Reload High Byte	T0RH	FF	81
F03	Timer 0 Reload Low Byte	T0RL	FF	81
F04	Timer 0 PWM High Byte	T0PWMH	00	81
F05	Timer 0 PWM Low Byte	T0PWML	00	82
F06	Timer 0 Control 0	T0CTL0	00	82
F07	Timer 0 Control 1	T0CTL1	00	83
Timer 1				
F08	Timer 1 High Byte	T1H	00	80
F09	Timer 1 Low Byte	T1L	01	80
F0A	Timer 1 Reload High Byte	T1RH	FF	81
F0B	Timer 1 Reload Low Byte	T1RL	FF	81

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# Stop Mode Recovery Using the External RESET Pin

When the Z8 Encore! XP F0823 Series device is in STOP mode and the external  $\overline{\text{RESET}}$  pin is driven Low, a system reset occurs. Because of a glitch filter operating on the  $\overline{\text{RESET}}$  pin, the Low pulse must be greater than the minimum width specified, or it is ignored. For more details, see Electrical Characteristics on page 193.

# **Reset Register Definitions**

## **Reset Status Register**

The Reset Status (RSTSTAT) register is a read-only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer control register, which is writeonly (Table 12).

#### Table 12. Reset Status Register (RSTSTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	POR	STOP	WDT	EXT		Rese	erved	
RESET	See descriptions below			0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF0H							

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using WDT time-out	0	0	1	0
Reset using the OCD (OCTCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using WDT time-out	0	1	1	0

#### POR—Power-On Reset Indicator

If this bit is set to 1, a Power-On Reset event is occurred. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port A	PA0	T0IN/T0OUT*	Timer 0 Input/Timer 0 Output Complement	N/A
		Reserved		-
	PA1	TOOUT	Timer 0 Output	-
		Reserved		-
	PA2	DE0	UART 0 Driver Enable	-
		Reserved		-
	PA3	CTS0	UART 0 Clear to Send	-
		Reserved		-
	PA4	RXD0/IRRX0	UART 0 / IrDA 0 Receive Data	-
		Reserved		-
	PA5	TXD0/IRTX0	UART 0 / IrDA 0 Transmit Data	-
		Reserved		-
	PA6	T1IN/T1OUT*	Timer 1 Input/Timer 1 Output Complement	-
		Reserved		
	PA7	T1OUT	Timer 1 Output	-
		Reserved		-

#### Table 15. Port Alternate Function Mapping (Non 8-Pin Parts)

**Note:** Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections as described in Port A–C Alternate Function Sub-Registers automatically enables the associated alternate function.

\* Whether PA0/PA6 take on the timer input or timer output complement function depends on the timer configuration as described in Timer Pin Signal Operation on page 79.

	Program Memory	
Priority	Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer on page 87)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Timer Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3 or Port D Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2 or Port D Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges

## Table 33. Trap and Interrupt Vectors in Order of Priority

# Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which can place Z8 Encore! XP<sup>®</sup> F0823 Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

# Operation

The WDT is a retriggerable one-shot timer that resets or interrupts Z8 Encore! XP F0823 Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT\_AO Flash Option Bit. The WDT\_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable down counter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

WDT Time-out Period (ms) =  $\frac{\text{WDT Reload Value}}{10}$ 

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10 kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 57 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

#### Table 57. Watchdog Timer Approximate Time-Out Delays

WDT Reload Value	WDT Reload Value	Approximate (with 10 kHz typical W	e Time-Out Delay VDT oscillator frequency)
(Hex)	(Decimal)	Typical	Description
000004	4	400 μs	Minimum time-out delay
FFFFF	16,777,215	28 minutes	Maximum time-out delay

## Z8 Encore! XP<sup>®</sup> F0823 Series Product Specification

## **Receiving IrDA Data**

Data received from the infrared transceiver using the IR\_RXD signal through the RXD pin is decoded by the Infrared Endec and passed to the UART. The UART's baud rate clock is used by the Infrared Endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 18 displays data reception. When the Infrared Endec is enabled, the UART's RXD signal is internal to the Z8 Encore! XP<sup>®</sup> F0823 Series products while the IR\_RXD signal is received through the RXD pin.



Figure 18. IrDA Data Reception

#### **Infrared Data Reception**

**Caution:** The system clock frequency must be at least 1.0 MHz to ensure proper reception of the 1.4 μs minimum width pulses allowed by the IrDA standard.

#### **Endec Receiver Synchronization**

The IrDA receiver uses a local baud rate clock counter (0 to 15 clock periods) to generate an input stream for the UART and to create a sampling window for detection of incoming pulses. The generated UART input (UART RXD) is delayed by 8 baud rate clock periods with respect to the incoming IrDA data stream. When a falling edge in the input data stream is detected, the Endec counter is reset. When the count reaches a value of 8, the UART RXD value is updated to reflect the value of the decoded data. When the count reaches 12 baud clock periods, the sampling window for the next incoming pulse opens. The window remains open until the count again reaches 8 (that is, 24 baud clock periods since the previous pulse was detected), giving the Endec a sampling window of minus four baud rate clocks to plus eight baud rate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window this process is repeated. If the incoming data is a logical 1 (no pulse), the Endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the Endec clock counter is reset, resynchronizing the Endec to the incoming signal, allowing the Endec to tolerate jitter and baud rate errors in the incoming datastream. Resynchronizing the Endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

# Infrared Encoder/Decoder Control Register Definitions

All Infrared Endec configuration and status information is set by the UART control registers as defined in Universal Asynchronous Receiver/Transmitter on page 93.

**Caution:** To prevent spurious signals during IrDA data transmission, set the IREN bit in the UART Control 1 register to 1 to enable the Infrared Encoder/Decoder before enabling the GPIO port alternate function for the corresponding pin.

REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL};

Note:

*This reference is independent of the Comparator reference.* 

00= Internal Reference Disabled, reference comes from external pin.

01 = Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

REFEXT—External Reference Select

0 = External reference buffer is disabled; V<sub>ref</sub> pin is available for GPIO functions

1 = The internal ADC reference is buffered and connected to the  $V_{ref}$  pin

#### CONT

0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles.

1 = Continuous conversion. ADC data updated every 256 system clock cycles.

ANAIN[3:0]—Analog Input Select

These bits select the analog input for conversion. Not all port pins in this list are available in all packages for Z8 Encore!  $XP^{\mathbb{R}}$  F0823 Series. For information on the port pins available with each package style, see Pin Description on page 7. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

Single-Ended:

0000 = ANA00001 = ANA10010 = ANA20011 = ANA30100 = ANA40101 = ANA50110 = ANA60111 = ANA71000 = Reserved1001 = Reserved1010 = Reserved1011 = Reserved1100 = Reserved1101 = Reserved1110 = Reserved1111 = Reserved A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG mode, a run function can be implemented by writing 40H to this register.

Table 99. OCD Control Register (OCDCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	DBGMODE	BRKEN	DBGACK		Rese	erved		RST
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R	R/W

#### DBGMODE—DEBUG Mode

The device enters DEBUG mode when this bit is 1. When in DEBUG mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to restart. This bit is automatically set when a BRK instruction is decoded and breakpoints are enabled. If the Flash Read Protect Option Bit is enabled, this bit can only be cleared by resetting the device. It cannot be written to 0.

0 = Z8 Encore! XP F0823 Series device is operating in NORMAL mode

1 = Z8 Encore! XP F0823 Series device is in DEBUG mode

#### BRKEN—Breakpoint Enable

This bit controls the behavior of the BRK instruction (opcode 00H). By default, breakpoints are disabled and the BRK instruction behaves similar to an NOP instruction. If this bit is 1, when a BRK instruction is decoded, the DBGMODE bit of the OCDCTL register is automatically set to 1.

- 0 = Breakpoints are disabled
- 1 = Breakpoints are enabled

#### DBGACK—Debug Acknowledge

This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.

0 = Debug Acknowledge is disabled

1 = Debug Acknowledge is enabled

#### Reserved—0 when read

#### RST—Reset

Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the OCD is not reset. This bit is automatically cleared to 0 at the end of reset.

0 = No effect

1 = Reset the Flash Read Protect Option Bit device

## Z8 Encore! XP<sup>®</sup> F0823 Series Product Specification

## Z8 Encore! XP<sup>®</sup> F0823 Series Product Specification

## Table 105. Notational Shorthand

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
СС	Condition Code	—	See Condition Codes overview in the eZ8 CPU User Manual.
DA	Direct Address	Addrs	Addrs represents a number in the range of 0000H to FFFFH.
ER	Extended Addressing Register	Reg	Reg represents a number in the range of 000H to FFFH.
IM	Immediate Data	#Data	Data is a number between 00H to FFH.
lr	Indirect Working Register	@Rn	n = 0–15.
IR	Indirect Register	@Reg	Reg. represents a number in the range of 00H to FFH.
Irr	Indirect Working Register Pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
IRR	Indirect Register Pair	@Reg	Reg represents an even number in the range 00H to FEH
р	Polarity	р	Polarity is a single bit binary value of either 0B or 1B.
r	Working Register	Rn	n = 0–15.
R	Register	Reg	Reg. represents a number in the range of 00H to FFH.
RA	Relative Address	Х	X represents an index in the range of +127 to – 128 which is an offset relative to the address of the next instruction
rr	Working Register Pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14.
RR	Register Pair	Reg	Reg. represents an even number in the range of 00H to FEH.
Vector	Vector Address	Vector	Vector represents a number in the range of 00H to FFH.
X	Indexed	#Index	The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to -128 range.

Table 108.	Bit Mani	pulation	Instructions

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	_	Complement Carry Flag
RCF	_	Reset Carry Flag
SCF	_	Set Carry Flag
ТСМ	dst, src	Test Complement Under Mask
TCMX	dst, src	Test Complement Under Mask using Extended Addressing
ТМ	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

Table 109. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses

## Table 110. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	HALT Mode
NOP	—	No Operation
RCF		Reset Carry Flag

# Figure 40 displays the 28-pin Plastic Dual Inline Package (PDIP) available for Z8 Encore! XP F0823 Series devices.



Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

#### Figure 40. 28-Pin Plastic Dual Inline Package (PDIP)

Number	٩	5	ines	rrupts	lit Timers WM	sit A/D Channels	tT with IrDA	cription
Part	Flas	RAN	101	Intel	16-E w/P\	10-E	UAF	Des
Z8 Encore! XP with 8	KB Flash							
Standard Temperatur	e: 0 °C to	70 °C						
Z8F0813PB005SC	8 KB	1 KB	6	12	2	0	1	PDIP 8-pin package
Z8F0813QB005SC	8 KB	1 KB	6	12	2	0	1	QFN 8-pin package
Z8F0813SB005SC	8 KB	1 KB	6	12	2	0	1	SOIC 8-pin package
Z8F0813SH005SC	8 KB	1 KB	16	18	2	0	1	SOIC 20-pin package
Z8F0813HH005SC	8 KB	1 KB	16	18	2	0	1	SSOP 20-pin package
Z8F0813PH005SC	8 KB	1 KB	16	18	2	0	1	PDIP 20-pin package
Z8F0813SJ005SC	8 KB	1 KB	24	18	2	0	1	SOIC 28-pin package
Z8F0813HJ005SC	8 KB	1 KB	24	18	2	0	1	SSOP 28-pin package
Z8F0813PJ005SC	8 KB	1 KB	24	18	2	0	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C								
Z8F0813PB005EC	8 KB	1 KB	6	12	2	0	1	PDIP 8-pin package
Z8F0813QB005EC	8 KB	1 KB	6	12	2	0	1	QFN 8-pin package
Z8F0813SB005EC	8 KB	1 KB	6	12	2	0	1	SOIC 8-pin package
Z8F0813SH005EC	8 KB	1 KB	16	18	2	0	1	SOIC 20-pin package
Z8F0813HH005EC	8 KB	1 KB	16	18	2	0	1	SSOP 20-pin package
Z8F0813PH005EC	8 KB	1 KB	16	18	2	0	1	PDIP 20-pin package
Z8F0813SJ005EC	8 KB	1 KB	24	18	2	0	1	SOIC 28-pin package
Z8F0813HJ005EC	8 KB	1 KB	24	18	2	0	1	SSOP 28-pin package
Z8F0813PJ005EC	8 KB	1 KB	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

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## Part Number Suffix Designations



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