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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0213sb005ec

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Address Space

The eZ8 CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more detailed information regarding the eZ8 CPU and its address space, refer to eZ8 CPU Core User Manual (UM0128) available for download at www.zilog.com.

Register File

The Register File address space in the Z8 Encore! XP[®] MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. Z8 Encore! XP F0823 Series devices contain 256 B-1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

Program Memory

The eZ8 CPU supports 64 KB of Program Memory address space. Z8 Encore! XP F0823 Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space. Reading from Program Memory addresses outside the available Flash

Table 19. Port A–C Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0	
FIELD	PCTL								
RESET				00	ЭH				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	FD1H, FD5H, FD9H								

PCTL[7:0]—Port Control

The Port Control register provides access to all sub-registers that configure the GPIO Port operation.

Port A-C Data Direction Sub-Registers

The Port A–C Data Direction sub-register is accessed through the Port A–C Control register by writing 01H to the Port A–C Address register (Table 20).

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 01H i	n Port A–C	Address Reg	gister, acces	sible throug	n the Port A-	-C Control F	Register

Table 20. Port A–C Data Direction Sub-Registers (PxDD)

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–C Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–C Input Data Register. The output driver is tristated.

Port A–C Alternate Function Sub-Registers

The Port A–C Alternate Function sub-register (Table 21) is accessed through the Port A–C Control register by writing 02H to the Port A–C Address register. The Port A–C Alternate Function sub-registers enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the Port A–C Alternate Function Set 1 Sub-Registers on page 48 and Port A–C Alternate Function Set 2 Sub-Registers on

PSMRE[7:0]—Port Stop Mode Recovery Source Enabled.

0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP mode do not initiate Stop Mode Recovery.

1 = The Port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP mode initiates Stop Mode Recovery.

Port A–C Pull-up Enable Sub-Registers

The Port A–C Pull-up Enable sub-register (Table 25) is accessed through the Port A–C Control register by writing 06H to the Port A–C Address register. Setting the bits in the Port A–C Pull-up Enable sub-registers enables a weak internal resistive pull-up on the specified Port pins.

Table 25. Port A–C Pull-Up Enable Sub-Registers (PxPUE)

BITS	7	6	5	4	3	2	1	0	
FIELD	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0	
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	lf 06H i	If 06H in Port A–C Address Register, accessible through the Port A–C Control Register							

PPUE[7:0]—Port Pull-up Enabled

0 = The weak pull-up on the Port pin is disabled.

1 = The weak pull-up on the Port pin is enabled.

Port A–C Alternate Function Set 1 Sub-Registers

The Port A–C Alternate Function Set1 sub-register (Table 26) is accessed through the Port A–C Control register by writing 07H to the Port A–C Address register. The Alternate Function Set 1 sub-registers selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register are defined in GPIO Alternate Functions on page 36.

Note:

Alternate function selection on port pins must also be enabled as described in Port A–C Alternate Function Sub-Registers *on page 45*.

	Program Memory	
Priority	Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer on page 87)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Timer Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3 or Port D Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2 or Port D Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges

Table 33. Trap and Interrupt Vectors in Order of Priority

Writing a 1 to the IRQE bit in the Interrupt Control register

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control register
- Reset
- Execution of a Trap instruction
- Illegal Instruction Trap
- Primary Oscillator Fail Trap
- Watchdog Timer Oscillator Fail Trap

Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all interrupts are enabled with identical interrupt priority (for example, all as Level 2 interrupts), the interrupt priority is assigned from highest to lowest as specified in Table 33 on page 54. Level 3 interrupts are always assigned higher priority than Level 2 interrupts which, in turn, always are assigned higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 33. Reset, Watchdog Timer interrupt (if enabled), Primary Oscillator Fail Trap, Watchdog Timer Oscillator Fail Trap, and Illegal Instruction Trap always have highest (Level 3) priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.

Caution: The following coding style that clears bits in the Interrupt Request registers is not recommended. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost.

Poor coding style that can result in lost interrupt requests: LDX r0, IRQ0 AND r0, MASK LDX IRQ0, r0

010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128

TMODE—Timer mode

This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value.

0000 = ONE-SHOT mode

0001 = CONTINUOUS mode

0010 = COUNTER mode

- 0011 = PWM SINGLE OUTPUT mode
- 0100 = CAPTURE mode
- 0101 = COMPARE mode
- 0110 = GATED mode
- 0111 = CAPTURE/COMPARE mode
- 1000 = PWM DUAL OUTPUT mode
- 1001 = CAPTURE RESTART mode
- 1010 = COMPARATOR COUNTER Mode

Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which can place Z8 Encore! XP[®] F0823 Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

Operation

The WDT is a retriggerable one-shot timer that resets or interrupts Z8 Encore! XP F0823 Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash Option Bit. The WDT_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable down counter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

WDT Time-out Period (ms) = $\frac{\text{WDT Reload Value}}{10}$

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10 kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 57 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

Table 57. Watchdog Timer Approximate Time-Out Delays

WDT Reload Value	WDT Reload Value	Approximate Time-Out Delay (with 10 kHz typical WDT oscillator frequency)				
(Hex)	(Decimal)	Typical	Description			
000004	4	400 μs	Minimum time-out delay			
FFFFF	16,777,215	28 minutes	Maximum time-out delay			

- 3. Clears the UART Receiver interrupt in the applicable Interrupt Request register.
- 4. Executes the IRET instruction to return from the interrupt-service routine and await more data.

Clear To Send (CTS) Operation

The CTS pin, if enabled by the CTSE bit of the UART Control 0 register, performs flow control on the outgoing transmit datastream. The Clear To Send ($\overline{\text{CTS}}$) input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert $\overline{\text{CTS}}$ at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this action is typically performed during Stop Bit transmission. If $\overline{\text{CTS}}$ deasserts in the middle of a character transmission, the current character is sent completely.

MULTIPROCESSOR (9-Bit) Mode

The UART has a MULTIPROCESSOR (9-bit) mode that uses an extra (9th) bit for selective communication when a number of processors share a common UART bus. In MULTIPROCESSOR mode (also referred to as 9-bit mode), the multiprocessor bit (MP) is transmitted immediately following the 8-bits of data and immediately preceding the Stop bit(s) as displayed in Figure 13. The character format is given below:



Figure 13. UART Asynchronous MULTIPROCESSOR Mode Data Format

In MULTIPROCESSOR (9-bit) mode, the Parity bit location (9th bit) becomes the Multiprocessor control bit. The UART Control 1 and Status 1 registers provide MULTIPROCESSOR (9-bit) mode control and status information. If an automatic address matching scheme is enabled, the UART Address Compare register holds the network address of the device.

MULTIPROCESSOR (9-bit) Mode Receive Interrupts

When MULTIPROCESSOR mode is enabled, the UART only processes frames addressed to it. The determination of whether a frame of data is addressed to the UART can be made

Reserved—0 when read

FSTAT—Flash Controller Status 000000 = Flash Controller locked 000001 = First unlock command received (73H written) 000010 = Second unlock command received (8CH written) 000011 = Flash Controller unlocked 000100 = Sector protect register selected 001xxx = Program operation in progress 010xxx = Page erase operation in progress 100xxx = Mass erase operation in progress

Flash Page Select Register

The Flash Page Select (FPS) register shares address space with the Flash Sector Protect Register. Unless the Flash controller is unlocked and written with 5EH, writes to this address target the Flash Page Select Register.

The register is used to select one of the eight available Flash memory pages to be programmed or erased. Each Flash Page contains 512 bytes of Flash memory. During a Page Erase operation, all Flash memory having addresses with the most significant 7-bits given by FPS[6:0] are chosen for program/erase operation.

BITS	7	6	5	4	3	2	1	0	
FIELD	INFO_EN	PAGE							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR		FF9H							

Table 81. Flash Page Select Register (FPS)

INFO_EN—Information Area Enable

0 = Information Area us not selected

1 = Information Area is selected. The Information Area is mapped into the Program Memory address space at addresses FE00H through FFFFH.

PAGE—Page Select

This 7-bit field identifies the Flash memory page for Page Erase and page unlocking. Program Memory Address[15:9] = PAGE[6:0]. For the Z8F04x3 devices, the upper 4 bits must always be 0. For the Z8F02x3 devices, the upper 5 bits must always be 0. For the Z8F01x3 devices, the upper 6 bits must always be 0.



Note:

- *This bit only enables the crystal oscillator. Its selection as system clock must be done manually.*
 - 0 = Crystal oscillator is enabled during reset, resulting in longer reset timing
 - *I* = *Crystal oscillator is disabled during reset, resulting in shorter reset timing*
- *¥* Warning: Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin. This is due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.

Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 89 through Table 91.

Trim Bit Address 0000H—Reserved

Table 89. Tri	im Options	Bits at A	Address	0000H

BITS	7	6	5	4	3	2	1	0			
FIELD	Reserved										
RESET	U	U	U	U	U	U	U	U			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR	Information Page Memory 0020H										
Note: U = Unchanged by Reset. R/W = Read/Write.											

Reserved—Altering this register may result in incorrect device operation.

Trim Bit Address 0001H—Reserved

Table 90. Trim Option Bits at 0001H

BITS	7	6	5	4	3	2	1	0		
FIELD	Reserved									
RESET	U	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR	Information Page Memory 0021H									
Note: U = Unchanged by Reset. R/W = Read/Write.										

```
DBG \leftarrow 05H
DBG \rightarrow OCDCTL[7:0]
```

• Write Program Counter (06H)—The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG mode or if the Flash Read Protect Option bit is enabled, the Program Counter (PC) values are discarded.

```
DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]
```

• **Read Program Counter (07H)**—The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG mode or if the Flash Read Protect Option bit is enabled, this command returns FFFFH.

```
DBG \leftarrow 07H
DBG \rightarrow ProgramCounter[15:8]
DBG \rightarrow ProgramCounter[7:0]
```

• Write Register (08H)—The Write Register command writes data to the Register File. Data can be written 1–256 bytes at a time (256 bytes can be written by setting size to 0). If the device is not in DEBUG mode, the address and data values are discarded. If the Flash Read Protect Option bit is enabled, only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

```
DBG \leftarrow 08H
DBG \leftarrow {4'h0,Register Address[11:8]}
DBG \leftarrow Register Address[7:0]
DBG \leftarrow Size[7:0]
DBG \leftarrow 1-256 data bytes
```

• **Read Register (09H)**—The Read Register command reads data from the Register File. Data can be read 1–256 bytes at a time (256 bytes can be read by setting size to 0). If the device is not in DEBUG mode or if the Flash Read Protect Option bit is enabled, this command returns FFH for all the data values.

```
DBG \leftarrow 09H
DBG \leftarrow {4'h0,Register Address[11:8]
DBG \leftarrow Register Address[7:0]
DBG \leftarrow Size[7:0]
DBG \rightarrow 1-256 data bytes
```

• Write Program Memory (0AH)—The Write Program Memory command writes data to Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. If the device

• **Read Program Memory CRC (0EH)**—The Read Program Memory Cyclic Redundancy Check (CRC) command computes and returns the CRC of Program Memory using the 16-bit CRC-CCITT polynomial. If the device is not in DEBUG mode, this command returns FFFFH for the CRC value. Unlike most other OCD Read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads the Program Memory, calculates the CRC value, and returns the result. The delay is a function of the Program Memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Program Memory.

```
DBG \leftarrow 0EH
DBG \rightarrow CRC[15:8]
DBG \rightarrow CRC[7:0]
```

• Step Instruction (10H)—The Step Instruction command steps one assembly instruction at the current Program Counter (PC) location. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

DBG \leftarrow 10H

• Stuff Instruction (11H)—The Stuff Instruction command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0-4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG \leftarrow 11H
DBG \leftarrow opcode[7:0]
```

• Execute Instruction (12H)—The Execute Instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.

```
DBG \leftarrow 12H
DBG \leftarrow 1-5 byte opcode
```

On-Chip Debugger Control Register Definitions

OCD Control Register

The OCD Control register controls the state of the OCD. This register is used to enter or exit DEBUG mode and to enable the BRK instruction. It also resets Z8 Encore! $XP^{\mbox{\ensuremath{\mathbb{R}}}}$ F0823 Series device.

Z8 Encore! XP[®] F0823 Series Product Specification

Table 114. Rotate and Shift Instructions	(Continued)
--	-------------

Mnemonic	Operands	Instruction
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

eZ8 CPU Instruction Summary

Table 115 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch, and the number of CPU clock cycles required for the instruction.

Assombly		Addre	ss Mode	Oncode(s)	Flags						Fotch	Inetr
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	z	S	v	D	Н	Cycles	Cycles
ADC dst, src	$dst \gets dst + src + C$	r	r	12	*	*	*	*	0	*	2	3
		r	lr	13	-						2	4
		R	R	14	-						3	3
		R	IR	15	-						3	4
		R	IM	16	_						3	3
		IR	IM	17	-						3	4
ADCX dst, src	$dst \gets dst + src + C$	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19	-						4	3
ADD dst, src	$dst \gets dst + src$	r	r	02	*	*	*	*	0	*	2	3
		r	lr	03	-						2	4
		R	R	04	-						3	3
		R	IR	05	-						3	4
		R	IM	06	-						3	3
		IR	IM	07	-						3	4
ADDX dst, src	$dst \gets dst + src$	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09	-						4	3
Flags Notation:	 * = Value is a function of the result of the operation. - = Unaffected X = Undefined 					0 = Reset to 0 1 = Set to 1						

Table 115. eZ8 CPU Instruction Summary

Figure 33 and Table 131 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.



Figure 33. UART Timing Without CTS

Table 131. UART	Timing Without CTS	

		Delay (ns)				
Parameter	Abbreviation	Minimum	Maximum			
UART						
T ₁	DE assertion to TXD falling edge (start bit) delay	1 * XIN period	1 bit time			
T ₂	End of Stop Bit(s) to DE deassertion delay (Tx data register is empty)	± 5				

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description		
Z8 Encore! XP with 4 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0423PB005SC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package		
Z8F0423QB005SC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package		
Z8F0423SB005SC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package		
Z8F0423SH005SC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package		
Z8F0423HH005SC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package		
Z8F0423PH005SC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package		
Z8F0423SJ005SC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package		
Z8F0423HJ005SC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package		
Z8F0423PJ005SC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package		
Extended Temperatu	re: -40 °C	to 105 °C	C							
Z8F0423PB005EC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package		
Z8F0423QB005EC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package		
Z8F0423SB005EC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package		
Z8F0423SH005EC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package		
Z8F0423HH005EC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package		
Z8F0423PH005EC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package		
Z8F0423SJ005EC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package		
Z8F0423HJ005EC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package		
Z8F0423PJ005EC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package		
Replace C with G for Lea	d-Free Pac	kaging								

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description		
Z8 Encore! XP with 2 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0223PB005SC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package		
Z8F0223QB005SC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package		
Z8F0223SB005SC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package		
Z8F0223SH005SC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package		
Z8F0223HH005SC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package		
Z8F0223PH005SC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package		
Z8F0223SJ005SC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package		
Z8F0223HJ005SC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package		
Z8F0223PJ005SC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package		
Extended Temperatur	re: -40 °C	to 105 °C	2							
Z8F0223PB005EC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package		
Z8F0223QB005EC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package		
Z8F0223SB005EC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package		
Z8F0223SH005EC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package		
Z8F0223HH005EC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package		
Z8F0223PH005EC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package		
Z8F0223SJ005EC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package		
Z8F0223HJ005EC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package		
Z8F0223PJ005EC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package		
Replace C with G for Lea	d-Free Pac	kaging								

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP [®] F0823 Se	eries D)evelopm	ent Ki	t				
Z8F08A28100KITG	2	Z8 Encor	e! XP	F082/	A Serie	s De	velop	oment Kit (20- and 28-Pin)
Z8F04A28100KITG	:	Z8 Encor	e! XP	F042	A Serie	s De	velop	oment Kit (20- and 28-Pin)
Z8F04A08100KITG	i	Z8 Encor	e! XP	F042	A Serie	s De	velop	oment Kit (8-Pin)
ZUSBSC00100ZACG		USB Smart Cable Accessory Kit						
ZUSBOPTSC01ZACG		Opto-Isolated USB Smart Cable Accessory Kit						
ZENETSC0100ZACG		Ethernet	Smart	Cab	le Acce	essor	y Kit	