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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0223pb005sc">https://www.e-xfl.com/product-detail/zilog/z8f0223pb005sc</a>

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP<sup>®</sup> F0823 Series 8-pin devices.

► **Note:** *All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 4 below describes 5 V-tolerance for the 20- and 28-pin packages only.*

**Table 4. Pin Characteristics (20- and 28-pin Devices)**

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output	5 V Tolerance
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PB[7:6] only
PC[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PC[7:3] only
RESET	I/O	I/O (defaults to RESET)	Low (in Reset mode)	Yes (PD0 only)	Always on for RESET	Yes	Always on for RESET	Yes
VDD	N/A	N/A	N/A	N/A			N/A	N/A
VSS	N/A	N/A	N/A	N/A			N/A	N/A

► **Note:** *PB6 and PB7 are available only in the devices without ADC.*

# Low-Power Modes

Z8 Encore! XP<sup>®</sup> F0823 Series products contain power-saving features. The highest level of power reduction is provided by the STOP mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in ACTIVE mode (defined as being in neither STOP nor HALT mode).

## STOP Mode

Executing the eZ8 CPU's Stop instruction places the device into STOP mode, powering down all peripherals except the Voltage Brownout detector, and the Watchdog Timer. These two blocks may also be disabled for additional power savings. In STOP mode, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; XIN and XOUT (if previously enabled) are disabled, and PA0/PA1 revert to the states programmed by the GPIO registers.
- System clock is stopped.
- eZ8 CPU is stopped.
- Program counter (PC) stops incrementing.
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control Register.
- If enabled, the Watchdog Timer logic continues to operate.
- If enabled for operation in STOP mode by the associated Flash Option Bit, the Voltage Brownout protection circuit continues to operate.
- All other on-chip peripherals are idle.

To minimize current in STOP mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails ( $V_{CC}$  or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP mode using Stop Mode Recovery. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

**Table 30. LED Drive Enable (LEDEN)**

BITS	7	6	5	4	3	2	1	0
FIELD	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F82H							

LEDEN[7:0]—LED Drive Enable

These bits determine which Port C pins are connected to an internal current sink.

0 = Tristate the Port C pin.

1= Connect controlled current sink to the Port C pin.

## LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 31).

These two bits select between four programmable drive levels. Each pin is individually programmable.

**Table 31. LED Drive Level High Register (LEDLVLH)**

BITS	7	6	5	4	3	2	1	0
FIELD	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F83H							

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA

01= 7 mA

10= 13 mA

11= 20 mA

## LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 32).

These two bits select between four programmable drive levels. Each pin is individually programmable.

Reserved—Must be 0

T1ENH—Timer 1 Interrupt Request Enable High Bit

T0ENH—Timer 0 Interrupt Request Enable High Bit

U0RENH—UART 0 Receive Interrupt Request Enable High Bit

U0TENH—UART 0 Transmit Interrupt Request Enable High Bit

ADCENH—ADC Interrupt Request Enable High Bit

**Table 39. IRQ0 Enable Low Bit Register (IRQ0ENL)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1ENL	T0ENL	U0RENL	U0TENL	Reserved	Reserved	ADCENL
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W
ADDR	FC2H							

Reserved—0 when read

T1ENL—Timer 1 Interrupt Request Enable Low Bit

T0ENL—Timer 0 Interrupt Request Enable Low Bit

U0RENL—UART 0 Receive Interrupt Request Enable Low Bit

U0TENL—UART 0 Transmit Interrupt Request Enable Low Bit

ADCENL—ADC Interrupt Request Enable Low Bit

## IRQ1 Enable High and Low Bit Registers

Table 40 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers (Table 41 and Table 42) form a priority encoded enabling for interrupts in the Interrupt Request 1 register. Priority is generated by setting bits in each register.

**Table 40. IRQ1 Enable and Priority Encoding**

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

where x indicates the register bits from 0–7.

**Table 48. Interrupt Control Register (IRQCTL)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	IRQE	Reserved						
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R/W	R	R	R	R	R	R	R
<b>ADDR</b>	FCFH							

IRQE—Interrupt Request Enable

This bit is set to 1 by executing an `EI` (Enable Interrupts) or `IRET` (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a `DI` instruction, eZ8 CPU acknowledgement of an interrupt request, reset or by a direct register write of a 0 to this bit.

0 = Interrupts are disabled

1 = Interrupts are enabled

Reserved—0 when read

# Timers

Z8 Encore! XP<sup>®</sup> F0823 Series products contain up to two 16-bit reloadable timers that are used for timing, event counting, or generation of PWM signals. The timers' features include:

- 16-bit reload counter.
- Programmable prescaler with prescale values from 1 to 128.
- PWM output generation.
- Capture and compare capability.
- External input pin for timer input, clock gating, or capture signal. External input pin signal frequency is limited to a maximum of one-fourth the system clock frequency.
- Timer output pin.
- Timer interrupt.

In addition to the timers described in this chapter, the baud rate generator of the UART (if unused) also provides basic timing functionality. For information on using the baud rate generator as an additional timer, see Universal Asynchronous Receiver/Transmitter on page 93.

## Architecture

Figure 9 displays the architecture of the timers.

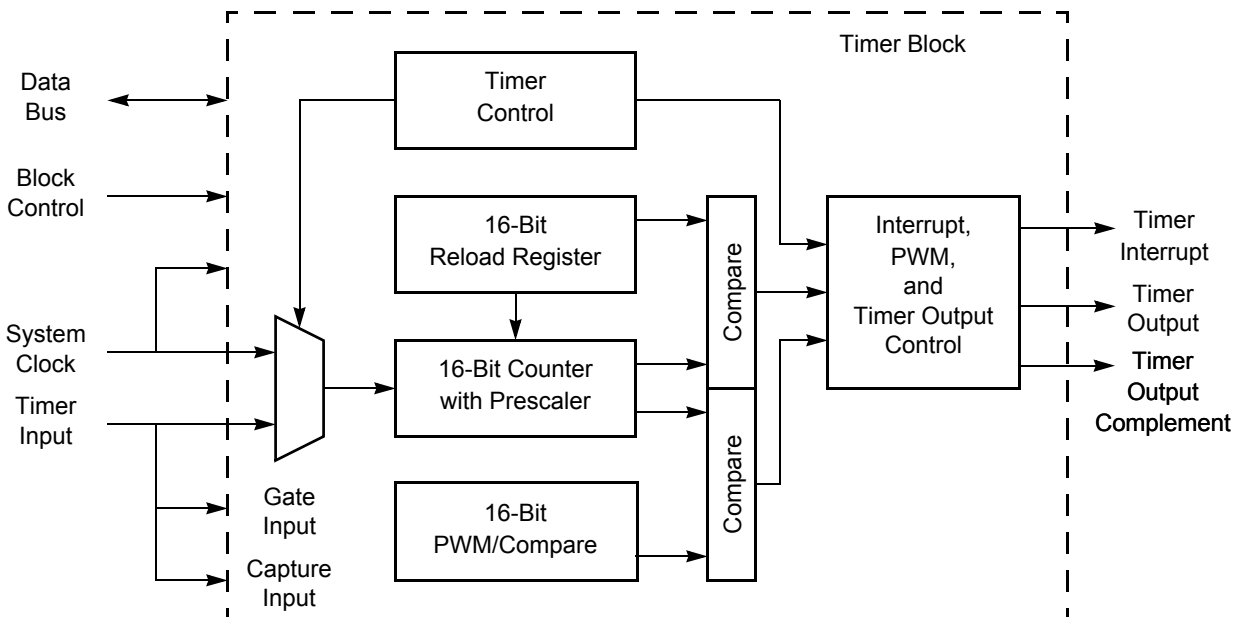


Figure 9. Timer Block Diagram

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT mode equation to determine the first PWM time-out period. If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

### **PWM Dual Output Mode**

In PWM DUAL OUTPUT mode, the timer outputs a PWM output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

Follow the steps below for configuring a timer for PWM Dual Output mode and initiating the PWM operation:

1. Write to the Timer Control register to:
  - Disable the timer
  - Configure the timer for PWM Dual Output mode. Setting the mode also involves writing to TMODEHI bit in TxCTL1 register
  - Set the prescale value



0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events  
 10 = Timer Interrupt only on defined Input Capture/Deassertion Events  
 11 = Timer Interrupt only on defined Reload/Compare Events

Reserved—Must be 0

PWMD—PWM Delay value

This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state.

000 = No delay  
 001 = 2 cycles delay  
 010 = 4 cycles delay  
 011 = 8 cycles delay  
 100 = 16 cycles delay  
 101 = 32 cycles delay  
 110 = 64 cycles delay  
 111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event  
 1 = Previous timer interrupt is a result of Timer Input Capture Event

### **Timer 0–1 Control Register 1**

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

**Table 56. Timer 0–1 Control Register 1 (TxCTL1)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	TEN	TPOL	PRES			TMODE		
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>ADDR</b>	F07H, F0FH							

TEN—Timer Enable

0 = Timer is disabled

1 = Timer enabled to count

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer

## Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Follow the steps below to configure the UART receiver for interrupt-driven operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a `DI` instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
5. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
  - Set the Multiprocessor Mode Select (`MPEN`) to Enable `MULTIPROCESSOR` mode
  - Set the Multiprocessor Mode Bits, `MPMD[1:0]`, to select the acceptable address matching scheme
  - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! XP devices without a DMA block)
7. Write the device address to the Address Compare Register (automatic `MULTIPROCESSOR` modes only).
8. Write to the UART Control 0 register to:
  - Set the receive enable bit (`REN`) to enable the UART for data reception
  - Enable parity, if appropriate and if multiprocessor mode is not enabled, and select either even or odd parity
9. Execute an `EI` instruction to enable interrupts.

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

1. Checks the UART Status 0 register to determine the source of the interrupt - error, break, or received data.
2. Reads the data from the UART Receive Data register if the interrupt was because of data available. If operating in `MULTIPROCESSOR` (9-bit) mode, further actions may be required depending on the `MULTIPROCESSOR` mode bits `MPMD[1:0]`.

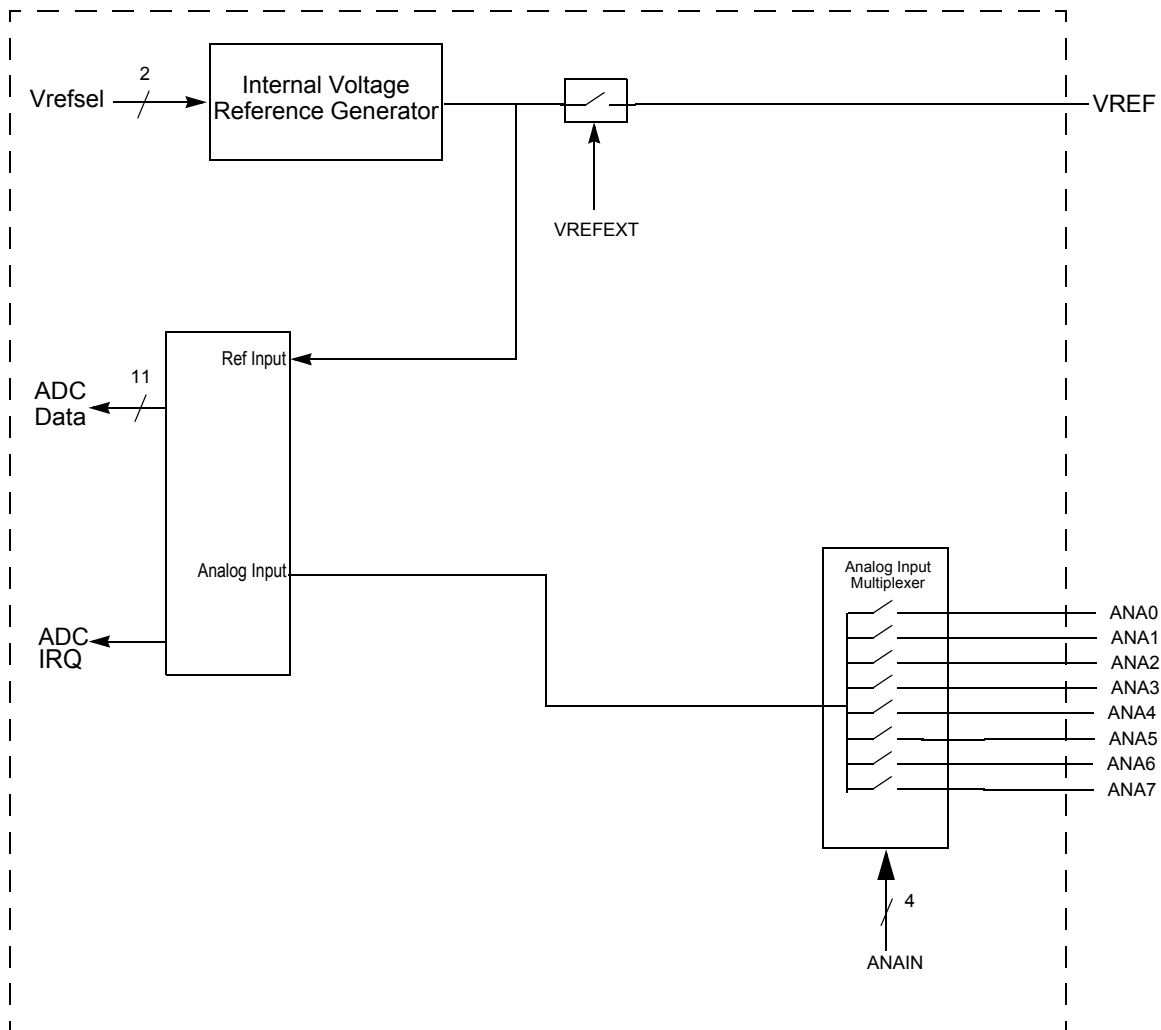


Figure 19. Analog-to-Digital Converter Block Diagram

## Operation

### Data Format

The output of the ADC is an 11-bit, signed, two's complement digital value. The output generally ranges from 0 to +1023, but offset errors can cause small negative values.

The ADC registers return 13 bits of data, but the two LSBs are intended for compensation use only. When the compensation routine is performed on the 13 bit raw ADC value, two

**Figure 20. Flash Memory Arrangement**

## **Flash Information Area**

The Flash information area is separate from program memory and is mapped to the address range `FE00H` to `FFFFH`. Not all these addresses are accessible. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

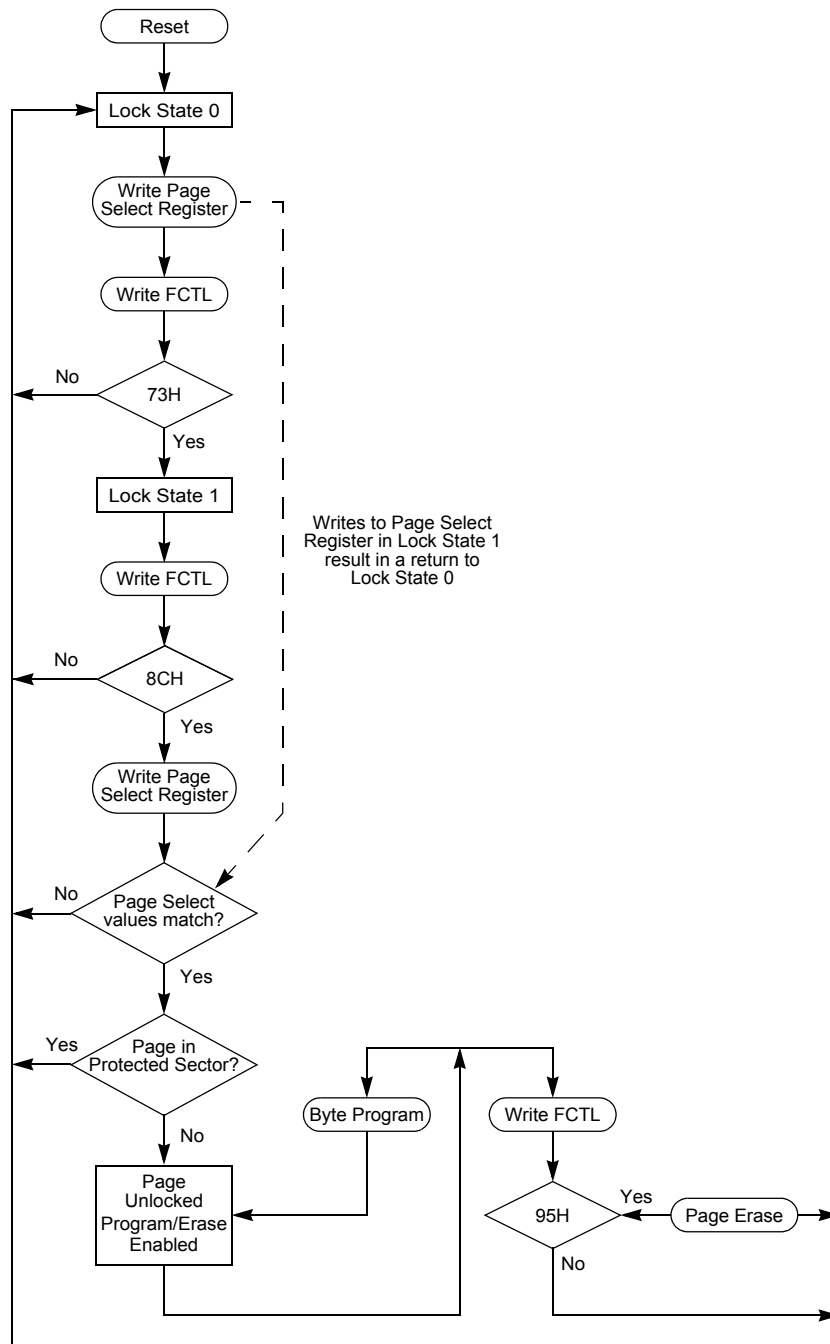


Figure 21. Flash Controller Operation Flowchart

## Flash Control Register Definitions

### Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FCTL) register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL. Page Erase applies only to the active page selected in Flash Page Select register. Mass Erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

**Table 79. Flash Control Register (FCTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
ADDR	FF8H							

FCMD—Flash Command

73H = First unlock command

8CH = Second unlock command

95H = Page Erase command (must be third command in sequence to initiate Page Erase)

63H = Mass Erase command (must be third command in sequence to initiate Mass Erase)

5EH = Enable Flash Sector Protect Register Access

### Flash Status Register

The Flash Status register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the write-only Flash Control Register.

**Table 80. Flash Status Register (FSTAT)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved		FSTAT					
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF8H							

Watchdog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Reserved—R/W bits must be 1 during writes; 1 when read.

VBO\_AO—Voltage Brownout Protection Always ON

0 = Voltage Brownout Protection can be disabled in STOP mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see Power Control Register 0 on page 32).

1 = Voltage Brownout Protection is always enabled including during STOP mode. This setting is the default for unprogrammed (erased) Flash.

FRP—Flash Read Protect

0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger.

1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.

Reserved—Must be 1

FWP—Flash Write Protect

This Option Bit provides Flash Program Memory protection:

0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase, and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger.

1 = Programming, Page Erase, and Mass Erase are enabled for all of Flash program memory.

## Flash Program Memory Address 0001H

**Table 88. Flash Options Bits at Program Memory Address 0001H**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0001H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Reserved—R/W must be 1 during writes; 1 when read

XTLDIS—State of Crystal Oscillator at Reset

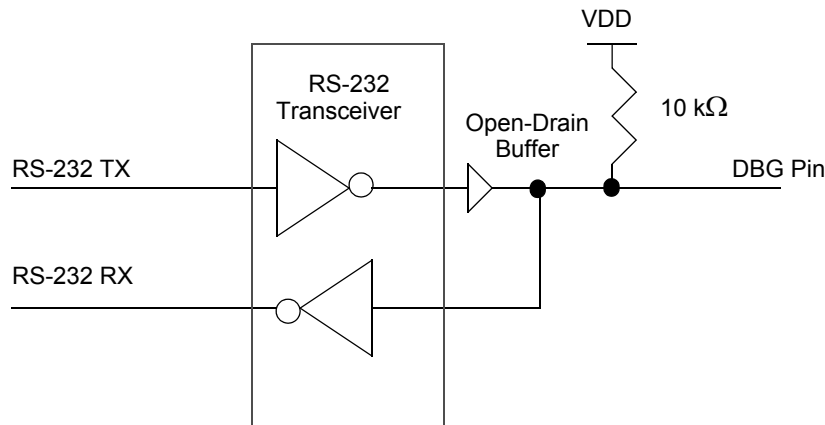


Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)

## DEBUG Mode

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP mode
- All enabled on-chip peripherals operate unless in STOP mode
- Automatically exits HALT mode
- Constantly refreshes the Watchdog Timer, if enabled.

### Entering DEBUG Mode

The device enters DEBUG mode following the operations below:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (breakpoint) instruction
- If the DBG pin is held Low during the most recent clock cycle of System Reset, the part enters DEBUG mode upon exiting System Reset

► **Note:** Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see OCD Auto-Baud Detector/Generator on page 154).

- If the PA2/ $\overline{\text{RESET}}$  pin is held Low while a 32-bit key sequence is issued to the PA0/DBG pin, the DBG feature is unlocked. After releasing PA2/ $\overline{\text{RESET}}$ , it is pulled high. At this



- **Read Program Memory CRC (0EH)**—The Read Program Memory Cyclic Redundancy Check (CRC) command computes and returns the CRC of Program Memory using the 16-bit CRC-CCITT polynomial. If the device is not in DEBUG mode, this command returns FFFFH for the CRC value. Unlike most other OCD Read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads the Program Memory, calculates the CRC value, and returns the result. The delay is a function of the Program Memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Program Memory.

```
DBG ← 0EH
DBG → CRC[15:8]
DBG → CRC[7:0]
```

- **Step Instruction (10H)**—The Step Instruction command steps one assembly instruction at the current Program Counter (PC) location. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 10H
```

- **Stuff Instruction (11H)**—The Stuff Instruction command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0-4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

- **Execute Instruction (12H)**—The Execute Instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.


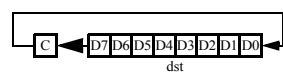
```
DBG ← 12H
DBG ← 1-5 byte opcode
```

## On-Chip Debugger Control Register Definitions

### OCD Control Register

The OCD Control register controls the state of the OCD. This register is used to enter or exit DEBUG mode and to enable the BRK instruction. It also resets Z8 Encore! XP<sup>®</sup> F0823 Series device.

Table 115. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	lr	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	–	–	–	–	–	–	3	2
RCF	C ← 0			CF	0	–	–	–	–	–	1	2
RET	PC ← @SP SP ← SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91								2
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11								2
Flags Notation:	* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1							

**Table 117. Absolute Maximum Ratings (Continued)**

Parameter	Minimum	Maximum	Units	Notes
Maximum current into $V_{DD}$ or out of $V_{SS}$		125	mA	
Operating temperature is specified in DC Characteristics.				
1. This voltage applies to all pins except the following: $V_{DD}$ , $AV_{DD}$ , pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but $V_{DD}$ .				
2. This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).				

## DC Characteristics

Table 118 lists the DC characteristics of the Z8 Encore! XP<sup>®</sup> F0823 Series products. All voltages are referenced to  $V_{SS}$ , the primary system ground.

**Table 118. DC Characteristics**

Symbol	Parameter	$T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ (unless otherwise specified)			Units	Conditions
		Minimum	Typical	Maximum		
$V_{DD}$	Supply Voltage	2.7	—	3.6	V	
$V_{IL1}$	Low Level Input Voltage	-0.3	—	$0.3 \cdot V_{DD}$	V	
$V_{IH1}$	High Level Input Voltage	$0.7 \cdot V_{DD}$	—	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.
$V_{IH2}$	High Level Input Voltage	$0.7 \cdot V_{DD}$	—	$V_{DD} + 0.3$	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.
$V_{OL1}$	Low Level Output Voltage	—	—	0.4	V	$I_{OL} = 2\text{ mA}$ ; $V_{DD} = 3.0\text{ V}$ High Output Drive disabled.
$V_{OH1}$	High Level Output Voltage	2.4	—	—	V	$I_{OH} = -2\text{ mA}$ ; $V_{DD} = 3.0\text{ V}$ High Output Drive disabled.
$V_{OL2}$	Low Level Output Voltage	—	—	0.6	V	$I_{OL} = 20\text{ mA}$ ; $V_{DD} = 3.3\text{ V}$ High Output Drive enabled.

Figure 35 displays the 8-pin Small Outline Integrated Circuit package (SOIC) available for the Z8 Encore! XP F0823 Series devices.

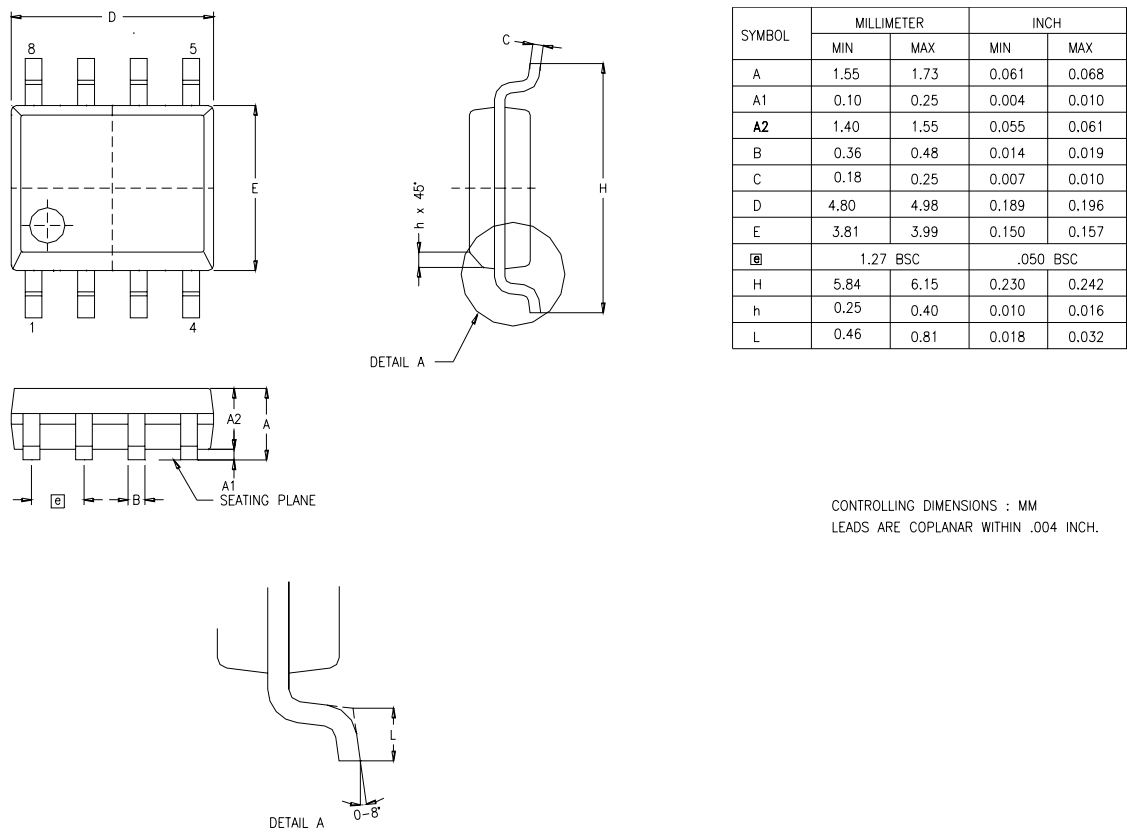


Figure 35. 8-Pin Small Outline Integrated Circuit Package (SOIC)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
<b>Z8 Encore! XP with 2 KB Flash, 10-Bit Analog-to-Digital Converter</b>								
<b>Standard Temperature: 0 °C to 70 °C</b>								
Z8F0223PB005SC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005SC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005SC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005SC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005SC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005SC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005SC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005SC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005SC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>								
Z8F0223PB005EC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005EC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005EC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005EC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005EC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005EC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005EC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005EC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005EC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								