



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-QFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0223qb005ec

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! $XP^{\text{(R)}}$ F0823 Series 8-pin devices.

Note: All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 4 below describes 5 V-tolerance for the 20- and 28-pin packages only.

Symbol		Reset	Active Low or Active	Tristate	Internal Pull-un	Schmitt-	Open Drain	5 V
Mnemonic	Direction	Direction	High	Output	or Pull-down	Input	Output	Tolerance
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PB[7:6] only
PC[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PC[7:3] only
RESET	I/O	I/O (d <u>efaults</u> to RESET)	Low (in Reset mode)	Yes (PD0 only)	Always on for RESET	Yes	Always on for RESET	Yes
VDD	N/A	N/A	N/A	N/A			N/A	N/A
VSS	N/A	N/A	N/A	N/A			N/A	N/A

Table 4. Pin Characteristics (20- and 28-pin Devices)

Note: *PB6 and PB7 are available only in the devices without ADC.*

Reset and Stop Mode Recovery

The Reset Controller within the Z8 Encore! XP[®] F0823 Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brownout (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash Option Bit to initiate a reset)
- External RESET pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-chip Debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP mode, a Stop Mode Recovery is initiated by either of the following:

- Watchdog Timer time-out
- GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device performs the following function:

• Generates the VBO reset when the supply voltage drops below a minimum safe level

Reset Types

Z8 Encore! XP F0823 Series provides several different types of Reset operation. Stop Mode Recovery is considered a form of Reset. Table 9 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

	Reset Characteristics and Latency							
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)					
System Reset	Reset (as applicable)	Reset	66 Internal Precision Oscillator Cycles					
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	66 Internal Precision Oscillator Cycles + IPO startup time					

Table 9. Reset and Stop Mode Recovery Characteristics and Latency

During a System Reset or Stop Mode Recovery, the IPO requires 4 µs to start up. Then the Z8 Encore! XP F0823 Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer, and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

When the control registers are re-initialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

Reset Sources

Table 10 lists the possible sources of a System Reset.

vector address. Following Stop Mode Recovery, the STOP bit in the Watchdog Timer Control Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The section following the table provides more detailed information on each of the Stop Mode Recovery sources.

Table 11. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external RESET Pin	System Reset
	Debug Pin driven Low	System Reset

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP mode, the device undergoes a Stop Mode Recovery sequence. In the Watchdog Timer Control register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and Z8 Encore! XP[®] F0823 Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins can be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

- **Note:** The SMR pulses shorter than specified does not trigger a recovery. When this happens, the STOP bit in the Reset Status (RSTSTAT) register is set to 1.
- **Caution:** In STOP mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin can initiate Stop Mode Recovery without being written to the Port Input Data register or without initiating an interrupt (if enabled for that pin).

tions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see On-Chip Debugger on page 151.

Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see Oscillator Control Register Definitions on page 167), the GPIO settings are overridden and PA0 and PA1 are disabled.

5 V Tolerance

All six I/O pins on the 8-pin devices are 5 V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than V_{DD} are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

Note: In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0], and PC[2:0]. All other signal pins are 5 V-tolerant, and can safely handle inputs higher than V_{DD} even with the pull-ups enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see Oscillator Control Register Definitions on page 167) such that the external oscillator is selected as the system clock. For 8-pin devices use PA1 instead of PB3.

46

page 49. See GPIO Alternate Functions on page 36 to determine the alternate function associated with each port pin.

Caution: Do not enable alternate functions for GPIO port pins for which there is no associated alternate function. Failure to follow this guideline can result in unpredictable operation.

Table 21. Port A–C Alternate Function Sub-Registers (PxAF)

BITS	7	6	5	4	3	2	1	0			
FIELD	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0			
RESET	00H (Ports A–C); 04H (Port A of 8-pin device)										
R/W		R/W									
ADDR	lf 02H i	If 02H in Port A–C Address Register, accessible through the Port A–C Control Register									

AF[7:0]—Port Alternate Function enabled

0 = The port pin is in normal mode and the DDx bit in the Port A–C Data Direction subregister determines the direction of the pin.

1 = The alternate function selected through Alternate Function Set sub-registers is enabled. Port pin operation is controlled by the alternate function.

Port A–C Output Control Sub-Registers

The Port A–C Output Control sub-register (Table 22) is accessed through the Port A–C Control register by writing 03H to the Port A–C Address register. Setting the bits in the Port A–C Output Control sub-registers to 1 configures the specified port pins for opendrain operation. These sub-registers affect the pins directly and, as a result, alternate functions are also affected.

Table 22. Port A–C Output Control Sub-Registers (PxOC)

BITS	7	6	5	4	3	2	1	0		
FIELD	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR	lf 03H i	If 03H in Port A–C Address Register, accessible through the Port A–C Control Register								

POC[7:0]—Port Output Control

These bits function independently of the alternate function bit and always disable the drains if set to 1.

Table 30. LED Drive Enable (LEDEN)

BITS	7	6	5	4	3	2	1	0				
FIELD		LEDEN[7:0]										
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
ADDR		F82H										

LEDEN[7:0]—LED Drive Enable

These bits determine which Port C pins are connected to an internal current sink.

0 = Tristate the Port C pin.

1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 31). These two bits select between four programmable drive levels. Each pin is individually programmable.

Table 31. LED Drive Level High Register (LEDLVLH)

BITS	7	6	5	4	3	2	1	0			
FIELD	LEDLVLH[7:0]										
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F83H									

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA01 = 7 mA10 = 13 mA

10 10 mA11 = 20 mA

LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 32). These two bits select between four programmable drive levels. Each pin is individually programmable.

- Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the PWM Control register to set the PWM dead band delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM high and low byte registers). It must also be less than the duration of the negative phase of the PWM signal (as defined by the difference between the PWM registers and the Timer Reload registers).
- 5. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
- 6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 7. Configure the associated GPIO port pin for the Timer Output and Timer Output Complement alternate functions. The Timer Output Complement function is shared with the Timer Input function for both timers. Setting the timer mode to Dual PWM automatically switches the function from Timer In to Timer Out Complement.
- 8. Write to the Timer Control register to enable the timer and initiate counting.

The PWM period is represented by the following equation: $PWM \text{ Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT mode equation determines the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{PWM Value}{Reload Value} \times 100$

CAPTURE Mode

In CAPTURE mode, the current timer count value is recorded when the appropriate external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge

BITS	7	6	5	4	3	2	1	0			
FIELD	PWML										
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F05H, F0DH									

Table 54. Timer 0–1 PWM Low Byte Register (TxPWML)

PWMH and PWML—Pulse-Width Modulator High and Low Bytes These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control Register (TxCTL1) register.

The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

Timer 0–1 Control Registers

Time 0–1 Control Register 0

The Timer Control Register 0 (TxCTL0) and Timer Control Register 1 (TxCTL1) determine the timer operating mode. It also includes a programmable PWM deadband delay, two bits to configure timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input Capture event.

Table 55. Timer 0–1 Control Register 0 (TxCTL0)

BITS	7	6	5	4	3	2	1	0			
FIELD	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP			
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F06H, F0EH									

TMODEHI—Timer Mode High Bit

This bit along with the TMODE field in TxCTL1 register determines the operating mode of the timer. This is the most-significant bit of the Timer mode selection value. See the TxCTL1 register description for more details.

TICONFIG—Timer Interrupt Configuration

This field configures timer interrupt definition.

- 0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events
- 10 = Timer Interrupt only on defined Input Capture/Deassertion Events
- 11 = Timer Interrupt only on defined Reload/Compare Events

Reserved-Must be 0

PWMD—PWM Delay value

This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state.

000 = No delay 001 = 2 cycles delay 010 = 4 cycles delay 011 = 8 cycles delay 100 = 16 cycles delay 101 = 32 cycles delay 110 = 64 cycles delay111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event

1 = Previous timer interrupt is a result of Timer Input Capture Event

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

BITS	7	6	5	4	3	2	1	0	
FIELD	TEN	TPOL		PRES		TMODE			
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	F07H, F0FH								

Table 56. Timer 0–1 Control Register 1 (TxCTL1)

TEN—Timer Enable

0 = Timer is disabled

1 = Timer enabled to count

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer

Z8 Encore! XP[®] F0823 Series Product Specification

External Driver Enable

The UART provides a Driver Enable (DE) signal for off-chip bus transceivers. This feature reduces the software overhead associated with using a GPIO pin to control the transceiver when communicating on a multi-transceiver bus, such as RS-485.

Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.





The Driver Enable to Start bit setup time is calculated as follows: (2)

$$\left(\frac{1}{\text{Baud Rate (Hz)}}\right) \le \text{DE to Start Bit Setup Time (s)} \le \left(\frac{2}{\text{Baud Rate (Hz)}}\right)$$

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to its digital representation. The features of this sigma-delta ADC include:

- 10-bit resolution
- Eight single-ended analog input sources are multiplexed with general-purpose I/O ports
- Interrupt upon conversion complete
- Bandgap generated internal voltage reference generator with two selectable levels
- Factory offset and gain calibration

Architecture

Figure 19 displays the major functional blocks of the ADC. An analog multiplexer network selects the ADC input from the available analog pins, ANA0 through ANA7.

Table 83. Flash Frequency High Byte Register (FFREQH)

BITS	7	6	5	4	3	2	1	0	
FIELD	FFREQH								
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	FFAH								

FFREQH—Flash Frequency High Byte High byte of the 16-bit Flash Frequency value

Table 84. Flash Frequency Low Byte Register (FFREQL)

BITS	7	6	5	4	3	2	1	0		
FIELD	FFREQL									
RESET	0									
R/W	R/W									
ADDR	FFBH									

FFREQL—Flash Frequency Low Byte Low byte of the 16-bit Flash Frequency value

Operation

The following sections describes the operation of OCD.

OCD Interface

The OCD uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, in that transmit and receive cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface from the Z8 Encore! XP F0823 Series products to the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figure 23 and Figure 24. The recommended method is the buffered implementation depicted in Figure 24. The DBG pin has a internal pull-up resistor which is sufficient for some applications (for more details on the pull-up current, see Electrical Characteristics on page 193). For OCD operation at higher data rates or in noisy systems, an external pull-up resistor is recommended.

Caution: For operation of the OCD, all power pins (V_{DD} and AV_{DD}) must be supplied with power, and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin is opendrain and may require an external pull-up resistor to ensure proper operation.





183

Assombly		Addres	Address Mode		Flags					Fotob Instr		
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	z	S	v	D	Н	Cycles	Cycles
LDC dst, src	$dst \gets src$	r	Irr	C2	_	_	_	_	-	-	2	5
		lr	Irr	C5	-						2	9
		Irr	r	D2	-						2	5
LDCI dst, src	dst ← src	lr	Irr	C3	_	_	_	_	-	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	Ir	D3							2	9
LDE dst, src	$dst \gets src$	r	Irr	82	-	-	-	-	-	_	2	5
		Irr	r	92	-						2	5
LDEI dst, src	dst ← src	lr	Irr	83	-	-	-	-	-	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	93							2	9
LDWX dst, src	$dst \gets src$	ER	ER	1FE8	_	_	_	_	_	_	5	4
LDX dst, src	$dst \gets src$	r	ER	84	-	-	-	-	-	_	3	2
		lr	ER	85	-						3	3
		R	IRR	86	-						3	4
		IR	IRR	87	-						3	5
		r	X(rr)	88	-						3	4
		X(rr)	r	89	-						3	4
		ER	r	94	-						3	2
		ER	lr	95	-						3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8	_						4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$dst \gets src + X$	r	X(r)	98		-	-	-	-	-	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	-	-	-	-	-	-	2	8
NOP	No operation			0F	_	_	_	_	_	_	1	2
Flags Notation:	* = Value is a function of f – = Unaffected X = Undefined	peration.	0 = 1 =	= Re = Se	eset et to	to 1	0					

Table 115. eZ8 CPU Instruction Summary (Continued)

Z8 Encore! XP[®] F0823 Series Product Specification

192

Electrical Characteristics

The data in this chapter is pre-qualification and pre-characterization and is subject to change. Additional electrical characteristics may be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed in Table 117 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		220	mW	
Maximum current into V_{DD} or out of V_{SS}		60	mA	
20-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		430	mW	
Maximum current into V _{DD} or out of V _{SS}		120	mA	
28-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		450	mW	

Table 117. Absolute Maximum Ratings

Table 117. Absolute Maximum Ratings (Continued)

Parameter	Minimum Maximum	Units	Notes
Maximum current into V_{DD} or out of V_{SS}	125	mA	

Operating temperature is specified in DC Characteristics.

- This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.
- This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

DC Characteristics

Table 118 lists the DC characteristics of the Z8 Encore! $XP^{\ensuremath{\mathbb{R}}}$ F0823 Series products. All voltages are referenced to V_{SS}, the primary system ground.

Table 118. DC Characteristics

		T _A = -40 °C to +105 °C (unless otherwise specified)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
V _{DD}	Supply Voltage	2.7	-	3.6	V	
V _{IL1}	Low Level Input Voltage	-0.3	_	0.3*V _{DD}	V	
V _{IH1}	High Level Input Voltage	0.7*V _{DD}	_	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.
V _{IH2}	High Level Input Voltage	0.7*V _{DD}	_	V _{DD} +0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.
V _{OL1}	Low Level Output Voltage	-	-	0.4	V	I _{OL} = 2 mA; V _{DD} = 3.0 V High Output Drive disabled.
V _{OH1}	High Level Output Voltage	2.4	-	-	V	I _{OH} = -2 mA; V _{DD} = 3.0 V High Output Drive disabled.
V _{OL2}	Low Level Output Voltage	-	-	0.6	V	I _{OL} = 20 mA; V _{DD} = 3.3 V High Output Drive enabled.

er					ers	Channels	IrDA	E	
Part Numb	Flash	RAM	I/O Lines	Interrupts	16-Bit Tim w/PWM	10-Bit A/D	UART with	Descriptio	
Z8 Encore! XP with 2	KB Flash								
Standard Temperature: 0 °C to 70 °C									
Z8F0213PB005SC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package	
Z8F0213QB005SC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package	
Z8F0213SB005SC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package	
Z8F0213SH005SC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package	
Z8F0213HH005SC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package	
Z8F0213PH005SC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package	
Z8F0213SJ005SC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package	
Z8F0213HJ005SC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package	
Z8F0213PJ005SC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package	
Extended Temperatur	e: -40 °C	to 105 °C	2						
Z8F0213PB005EC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package	
Z8F0213QB005EC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package	
Z8F0213SB005EC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package	
Z8F0213SH005EC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package	
Z8F0213HH005EC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package	
Z8F0213PH005EC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package	
Z8F0213SJ005EC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package	
Z8F0213HJ005EC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package	
Z8F0213PJ005EC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package	
Replace C with G for Lead-Free Packaging									

222