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#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0413hh005sc

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# **Pin Description**

Z8 Encore! XP<sup>®</sup> F0823 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and pin configurations available for each of the package styles. For information on physical package specifications, see Packaging on page 209.

## **Available Packages**

Table 2 lists the package styles that are available for each device in the Z8 Encore! XP F0823 Series product line.

Part Number	ADC	8-pin PDIP	8-pin SOIC	20-pin PDIP	20-pin SOIC	20-pin SSOP	28-pin PDIP	28-pin SOIC	28-pin SSOP	8-pin QFN/ MLF-S
Z8F0823	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0813	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0423	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0413	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0223	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0213	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0123	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0113	No	Х	Х	Х	Х	Х	Х	Х	Х	Х

Table 2. Z8 Encore! XP F0823 Series Package Options

## **Pin Configurations**

Figure 2 through Figure 4 displays the pin configurations for all packages available in the Z8 Encore! XP F0823 Series. For description of signals, see Table 3. The analog input alternate functions (ANA*x*) are not available on the Z8F0x13 devices. The analog supply pins (AV<sub>DD</sub> and AV<sub>SS</sub>) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all pins of Ports A, B, and C default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general-purpose input ports until programmed otherwise.

Table 3.	Signal	Descriptions	(Continued)	
	orginar	Descriptions	(Continucu)	ł.,

Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	I	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD.
		<b>Caution:</b> The DBG pin is open-drain and requires an external pull- up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V <sub>DD</sub>	Ι	Digital Power Supply.
AV <sub>DD</sub>	I	Analog Power Supply.
V <sub>SS</sub>	I	Digital Ground.
AV <sub>SS</sub>	Ι	Analog Ground.
Note: The AV <sub>DD</sub> and A PB7 on 28-pin pa	.V <sub>SS</sub> sigr ackages	nals are available only in 28-pin packages with ADC. They are replaced by PB6 and without ADC.

# **Pin Characteristics**

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

# **Register Map**

Table 8 lists the address map for the Register File of the Z8 Encore! XP<sup>®</sup> F0823 Series devices. Not all devices and package styles in the Z8 Encore! XP F0823 Series support the ADC, or all GPIO ports. Consider registers for unimplemented peripherals as reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
General-Purpos	se RAM			
Z8F0823/Z8F08	13 Devices			
000–3FF	General-Purpose Register File RAM	_	XX	
400–EFF	Reserved		XX	
Z8F0423/Z8F04	13 Devices			
000–3FF	General-Purpose Register File RAM		XX	
400–EFF	Reserved	_	XX	
Z8F0223/Z8F02	13 Devices			
000–1FF	General-Purpose Register File RAM		XX	
200–EFF	Reserved		XX	
Z8F0123/Z8F01	13 Devices			
000–0FF	General-Purpose Register File RAM		XX	
100–EFF	Reserved		XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	80
F01	Timer 0 Low Byte	TOL	01	80
F02	Timer 0 Reload High Byte	T0RH	FF	81
F03	Timer 0 Reload Low Byte	T0RL	FF	81
F04	Timer 0 PWM High Byte	T0PWMH	00	81
F05	Timer 0 PWM Low Byte	T0PWML	00	82
F06	Timer 0 Control 0	T0CTL0	00	82
F07	Timer 0 Control 1	T0CTL1	00	83
Timer 1				
F08	Timer 1 High Byte	T1H	00	80
F09	Timer 1 Low Byte	T1L	01	80
F0A	Timer 1 Reload High Byte	T1RH	FF	81
F0B	Timer 1 Reload Low Byte	T1RL	FF	81



Figure 6. Voltage Brownout Reset Operation

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a POR after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is in NORMAL or STOP mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT\_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT\_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT status bit in the WDT Control register is set to signify that the reset was initiated by the Watchdog Timer.

## **External Reset Input**

The  $\overline{\text{RESET}}$  pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the  $\overline{\text{RESET}}$  pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system

# Stop Mode Recovery Using the External RESET Pin

When the Z8 Encore! XP F0823 Series device is in STOP mode and the external  $\overline{\text{RESET}}$  pin is driven Low, a system reset occurs. Because of a glitch filter operating on the  $\overline{\text{RESET}}$  pin, the Low pulse must be greater than the minimum width specified, or it is ignored. For more details, see Electrical Characteristics on page 193.

# **Reset Register Definitions**

#### **Reset Status Register**

The Reset Status (RSTSTAT) register is a read-only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer control register, which is writeonly (Table 12).

#### Table 12. Reset Status Register (RSTSTAT)

BITS	7	6	5	4	3	2	1	0		
FIELD	POR	STOP	WDT	EXT	Reserved					
RESET	See d	lescriptions	below	0	0	0	0	0		
R/W	R	R	R	R	R	R	R	R		
ADDR		FF0H								

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using WDT time-out	0	0	1	0
Reset using the OCD (OCTCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using WDT time-out	0	1	1	0

#### POR—Power-On Reset Indicator

If this bit is set to 1, a Power-On Reset event is occurred. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.

## Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.



Figure 7. GPIO Port Pin Block Diagram

# **GPIO Alternate Functions**

Many of the GPIO port pins are used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The port A–D Alternate Function sub-registers configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. Table 15 on page 39 lists the alternate functions possible with each port pin. The alternate function associated at a pin is defined through Alternate Function Sets sub-registers AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

## Table 32. LED Drive Level Low Register (LEDLVLL)

BITS	7	6	5	4	3	2	1	0		
FIELD		LEDLVLL[7:0]								
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR				F8	4H					

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA01 = 7 mA10 = 13 mA

10 = 13 mA11 = 20 mA

# **Interrupt Request 1 Register**

The Interrupt Request 1 (IRQ1) register (Table 35) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ1 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 1 register to determine if any interrupt requests are pending.

Table 35. Interrupt Request 1 Register (IRQ1)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7VI	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	3H			

PA7VI—Port A7 Interrupt Request

0 = No interrupt request is pending for GPIO Port A

1 = An interrupt request from GPIO Port A

PA6CI—Port A6 or Comparator Interrupt Request

0 = No interrupt request is pending for GPIO Port A or Comparator

1 = An interrupt request from GPIO Port A or Comparator

PAxI—Port A Pin x Interrupt Request

0 = No interrupt request is pending for GPIO Port A pin x

1 = An interrupt request from GPIO Port A pin x is awaiting service

where x indicates the specific GPIO Port pin number (0-5)

# **Interrupt Request 2 Register**

The Interrupt Request 2 (IRQ2) register (Table 36) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 register to determine if any interrupt requests are pending.

## Z8 Encore! XP<sup>®</sup> F0823 Series Product Specification

# **Timer Control Register Definitions**

## Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 49 and Table 50) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from the TxL reads the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0	
FIELD		TH							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR		F00H, F08H							

Table 49. Timer 0–1 High Byte Register (TxH)

#### Table 50. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0		
FIELD	TL									
RESET	0	0	0	0	0	0	0	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR	F01H, F09H									

TH and TL—Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value

## **Timer Reload High and Low Byte Registers**

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 51 and Table 52) store a 16-bit Reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte register occurs, the temporary holding register value is written to the Timer High Byte register. This operation allows simultaneous updates of the 16-bit Timer Reload value.

## Watchdog Timer Refresh

When first enabled, the WDT is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the down counter to be reloaded with the WDT Reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When Z8 Encore! XP<sup>®</sup> F0823 Series devices are operating in DEBUG Mode (using the OCD), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

## Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT\_RES Flash Option Bit determines the time-out response of the Watchdog Timer. For information on programming of the WDT\_RES Flash Option Bit, see Flash Option Bits on page 141.

#### WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watchdog Timer Control register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

The Reset Status Register (see Reset Status Register on page 28) must be read before clearing the WDT interrupt. This read clears the WDT time-out Flag and prevents further WDT interrupts for immediately occurring.

#### WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and Z8 Encore! XP F0823 Series are in STOP mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watchdog Timer Control register are set to 1 following a WDT time-out in STOP mode. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

- 6. Check the TDRE bit in the UART Status 0 register to determine if the Transmit Data register is empty (indicated by a 1). If empty, continue to step 7. If the Transmit Data register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data register becomes available to receive new data.
- 7. Write the UART Control 1 register to select the outgoing address bit.
- 8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
- 9. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
- 10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR mode is enabled,.
- 11. To transmit additional bytes, return to step 5.

#### Transmitting Data using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data register to accept new data for transmission. Follow the steps below to configure the UART for interrupt-driven data transmission:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
- 5. Write to the UART Control 1 register to enable MULTIPROCESSOR (9-bit) mode functions, if MULTIPROCESSOR mode is appropriate.
- 6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR mode.
- 7. Write to the UART Control 0 register to:
  - Set the transmit enable bit (TEN) to enable the UART for data transmission.
  - Enable parity, if appropriate and if MULTIPROCESSOR mode is not enabled, and select either even or odd parity.
  - Set or clear CTSE to enable or disable control from the remote receiver using the  $\overline{\text{CTS}}$  pin.
- 8. Execute an EI instruction to enable interrupts.

received and the UART Receive Data register has not been read. If the RDA bit is reset to 0, reading the UART Receive Data register clears this bit.

0 = No overrun error occurred

1 = An overrun error occurred

FE—Framing Error

This bit indicates that a framing error (no Stop bit following data reception) was detected. Reading the UART Receive Data register clears this bit.

0 = No framing error occurred

1 = A framing error occurred

#### BRKD-Break Detect

This bit indicates that a break occurred. If the data bits, parity/multiprocessor bit, and Stop bit(s) are all 0s this bit is set to 1. Reading the UART Receive Data register clears this bit.

0 = No break occurred

1 = A break occurred

TDRE—Transmitter Data Register Empty

This bit indicates that the UART Transmit Data register is empty and ready for additional data. Writing to the UART Transmit Data register resets this bit.

0 = Do not write to the UART Transmit Data register

1 = The UART Transmit Data register is ready to receive an additional byte to be transmitted

TXE—Transmitter Empty

This bit indicates that the transmit shift register is empty and character transmission is finished.

0 = Data is currently transmitting

1 = Transmission is complete

#### $CTS \longrightarrow \overline{CTS}$ signal

When this bit is read it returns the level of the  $\overline{\text{CTS}}$  signal. This signal is active Low.

#### **UART Status 1 Register**

This register contains multiprocessor control and status bits.

#### Table 65. UART Status 1 Register (U0STAT1)

BITS	7	6	5	4	3	2	1	0		
FIELD	Reserved							MPRX		
RESET	0	0	0	0	0	0	0	0		
R/W	R	R	R	R	R/W	R/W	R	R		
ADDR	F44H									

bits of resolution are lost because of a rounding error. As a result, the final value is an 11- bit number.

#### Automatic Powerdown

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered down. From this powerdown state, the ADC requires 40 system clock cycles to powerup. The ADC powers up when a conversion is requested by the ADC Control register.

## Single-Shot Conversion

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. Follow the steps below for setting up the ADC and initiating a single-shot conversion:

- 1. Enable the acceptable analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
- 2. Write the ADC Control/Status Register 1 to configure the ADC
  - Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
- 3. Write to the ADC Control Register 0 to configure the ADC and begin the conversion. The bit fields in the ADC Control register can be written simultaneously:
  - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
  - Clear CONT to 0 to select a single-shot conversion.
  - If the internal voltage reference must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
  - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in the ADC Control Register 0.
  - Set CEN to 1 to start the conversion.
- 4. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power-up before beginning the 5129 cycle conversion.

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## Flash Operation Timing Using the Flash Frequency Registers

Before performing either a program or erase operation on Flash memory, you must first configure the Flash Frequency High and Low Byte registers. The Flash Frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 32 kHz (32768 Hz) through 20 MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

FFREQ[15:0] = System Clock Frequency (Hz) 1000

**Caution:** Flash programming and erasure are not supported for system clock frequencies below 32 kHz (32768 Hz) or above 20 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of Z8 Encore! XP<sup>®</sup> F0823 Series devices.

## Flash Code Protection Against External Access

The user code contained within the Flash memory can be protected against external access with the On-Chip Debugger. Programming the FRP Flash Option Bit prevents reading of the user code with the On-Chip Debugger. For more information, see Flash Option Bits on page 141 and On-Chip Debugger on page 151.

## Flash Code Protection Against Accidental Program and Erasure

Z8 Encore! XP F0823 Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash Option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

#### Flash Code Protection Using the Flash Option Bits

The FRP and FWP Flash Option Bits combine to provide three levels of Flash Program Memory protection as listed in Table 78. For more information, see Flash Option Bits on page 141.

# **On-Chip Debugger**

Z8 Encore! XP<sup>®</sup> F0823 Series devices contain an integrated On-Chip Debugger (OCD) that provides advanced debugging features that include:

- Single pin interface
- Reading and writing of the register file
- Reading and writing of program and data memory
- Setting of breakpoints and watchpoints
- Executing eZ8 CPU instructions
- Debug pin sharing with general-purpose input-output function to maximize the pins available

# Architecture

The on-chip debugger consists of four primary functional blocks: transmitter, receiver, auto-baud detector/generator, and debug controller. Figure 22 displays the architecture of the OCD.



Figure 22. On-Chip Debugger Block Diagram

#### Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar non-maskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while searching for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

**Caution:** It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! XP F0823 Series device ceases functioning and can only be recovered by Power-On Reset.

# **Oscillator Control Register Definitions**

The following section provides the bit definitions for the Oscillator Control register.

#### **Oscillator Control Register**

The Oscillator Control register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.

BITS	7	6	5	4	3	2	1	0					
FIELD	INTEN	Reserved	WDTEN	POFEN	WDFEN	SCKSEL							
RESET	1	0	1	0	0	0	0	0					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
ADDR	F86H												

Table 102. Oscillator Control Register (OSCCTL)

Assembly	Symbolic Operation	Addre	ss Mode	Opcode(s) (Hex)	Flags						Fetch	Instr
Mnemonic		dst	src		С	z	S	v	D	н	Cycles	Cycles
XOR dst, src	$dst \gets dst \ XOR \ src$	r	r	B2	-	*	*	0	_	_	2	3
		r	lr	B3	_						2	4
		R	R	B4	_						3	3
		R	IR	B5	_						3	4
		R	IM	B6	_						3	3
		IR	IM	B7	_						3	4
XORX dst, src	$dst \gets dst \: XOR \: src$	ER	ER	B8	_	*	*	0	_	_	4	3
		ER	IM	B9	_						4	3
Flags Notation:	* = Value is a function o – = Unaffected X = Undefined	f the resu	It of the o	peration.	0 = 1 =	= Re = Se	ese et to	t to 0 1	0			

#### Table 115. eZ8 CPU Instruction Summary (Continued)

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reset in STOP mode 89 time-out response 88 Watchdog Timer Control Register (WDTCTL) 90 WDTCTL register 90, 128, 167 WDTH register 91 WDTL register 91 WDTU register 91 working register 173 working register pair 173

# Χ

X 173 XOR 178 XORX 178

# Ζ

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