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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	22
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0423hj005ec">https://www.e-xfl.com/product-detail/zilog/z8f0423hj005ec</a>

 **Warning:** DO NOT USE IN LIFE SUPPORT

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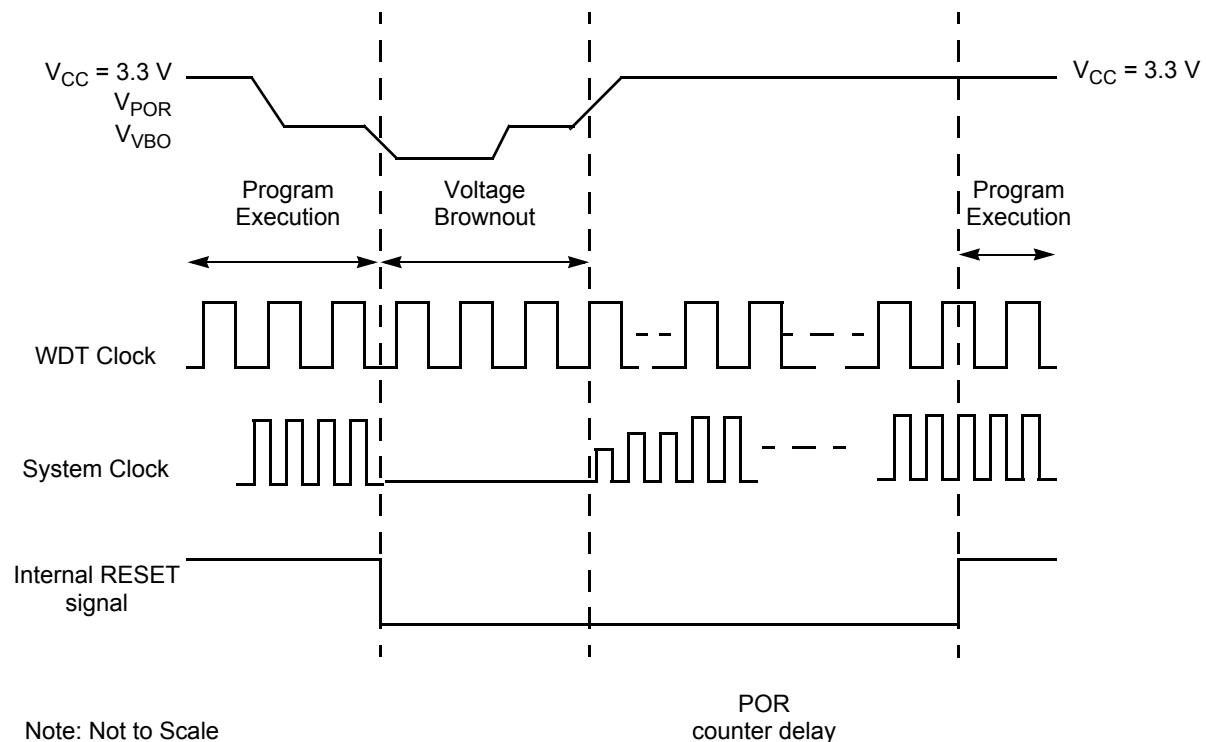
► **Note:** \*Analog input alternate functions (ANA) are not available on the Z8F0x13 devices.

## Signal Descriptions

Table 3 lists the Z8 Encore! XP<sup>®</sup> F0823 Series signals. To determine the signals available for the specific package styles, see Pin Configurations on page 7.

**Table 3. Signal Descriptions**

Signal Mnemonic	I/O	Description
<b>General-Purpose I/O Ports A–D</b>		
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
<b>Note:</b> PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV <sub>DD</sub> and AV <sub>SS</sub> .		
<b>UART Controllers</b>		
TXD0	O	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	I	Clear To Send. This signal is the flow control input for the UART.
DE	O	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
<b>Timers</b>		
T0OUT/T1OUT	O	Timer Output 0–1. These signals are output from the timers.
$\overline{T0OUT/T1OUT}$	O	Timer Complement Output 0–1. These signals are output from the timers in PWM Dual Output mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed $\overline{T0OUT}$ signals.
<b>Comparator</b>		
CINP/CINN	I	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
COUT	O	Comparator Output. This is the output of the comparator.



**Figure 6. Voltage Brownout Reset Operation**

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a POR after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is in NORMAL or STOP mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT\_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT\_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT status bit in the WDT Control register is set to signify that the reset was initiated by the Watchdog Timer.

## External Reset Input

The  $\overline{\text{RESET}}$  pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the  $\overline{\text{RESET}}$  pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system



# Interrupt Controller

The interrupt controller on the Z8 Encore! XP<sup>®</sup> F0823 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 unique interrupt vectors
  - 12 GPIO port pin interrupt sources (two are shared)
  - 8 on-chip peripheral interrupt sources (two are shared)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information on interrupt servicing by the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Interrupt Vector Listing

Table 33 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

► **Note:** *Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.*



**Table 43. IRQ2 Enable and Priority Encoding (Continued)**

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
1	1	Level 3	High

where x indicates the register bits from 0–7.

**Table 44. IRQ2 Enable High Bit Register (IRQ2ENH)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC7H							

Reserved—Must be 0

C3ENH—Port C3 Interrupt Request Enable High Bit

C2ENH—Port C2 Interrupt Request Enable High Bit

C1ENH—Port C1 Interrupt Request Enable High Bit

C0ENH—Port C0 Interrupt Request Enable High Bit

**Table 45. IRQ2 Enable Low Bit Register (IRQ2ENL)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC8H							

Reserved—Must be 0

C3ENL—Port C3 Interrupt Request Enable Low Bit

C2ENL—Port C2 Interrupt Request Enable Low Bit

C1ENL—Port C1 Interrupt Request Enable Low Bit

C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 46) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin.

**Table 48. Interrupt Control Register (IRQCTL)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	IRQE	Reserved						
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R/W	R	R	R	R	R	R	R
<b>ADDR</b>	FCFH							

IRQE—Interrupt Request Enable

This bit is set to 1 by executing an `EI` (Enable Interrupts) or `IRET` (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a `DI` instruction, eZ8 CPU acknowledgement of an interrupt request, reset or by a direct register write of a 0 to this bit.

0 = Interrupts are disabled

1 = Interrupts are enabled

Reserved—0 when read

generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 register is set to indicate the timer interrupt is because of an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 register is cleared to indicate the timer interrupt is not caused by an input capture event.

Follow the steps below for configuring a timer for CAPTURE RESTART mode and initiating the count:

1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for CAPTURE RESTART mode. Setting the mode also involves writing to TMODEHI bit in TxCTL1 register.
  - Set the prescale value.
  - Set the Capture edge (rising or falling) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a Capture or a Reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input Capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

### **COMPARE Mode**

In COMPARE mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the

### CAPTURE/COMPARE Mode

0 = Counting is started on the first rising edge of the Timer Input signal. The current count is captured on subsequent rising edges of the Timer Input signal.

1 = Counting is started on the first falling edge of the Timer Input signal. The current count is captured on subsequent falling edges of the Timer Input signal.

### PWM DUAL OUTPUT Mode

0 = Timer Output is forced Low (0) and Timer Output Complement is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload. When enabled, the Timer Output Complement is forced Low (0) upon PWM count match and forced High (1) upon Reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to High (1).

1 = Timer Output is forced High (1) and Timer Output Complement is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload. When enabled, the Timer Output Complement is forced High (1) upon PWM count match and forced Low (0) upon Reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to Low (0).

### CAPTURE RESTART Mode

0 = Count is captured on the rising edge of the Timer Input signal

1 = Count is captured on the falling edge of the Timer Input signal

### COMPARATOR COUNTER Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit.

When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

**! Caution:** *When the Timer Output alternate function TxOUT on a GPIO port pin is enabled, TxOUT changes to whatever state the TPOL bit is in. The timer does not need to be enabled for that to happen. Also, the port data direction sub register is not needed to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.*

PRES—Prescale value.

The timer input clock is divided by  $2^{\text{PRES}}$ , where PRES can be set from 0 to 7. The prescaler is reset each time the Timer is disabled. This reset ensures proper clock division each time the Timer is restarted.

000 = Divide by 1

001 = Divide by 2

**Table 59. Watchdog Timer Reload Upper Byte Register (WDTU)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTU							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF1H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTU—WDT Reload Upper Byte  
Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

**Table 60. Watchdog Timer Reload High Byte Register (WDTH)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	04H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF2H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTH—WDT Reload High Byte  
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 61. Watchdog Timer Reload Low Byte Register (WDTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF3H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTL—WDT Reload Low  
Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

bits of resolution are lost because of a rounding error. As a result, the final value is an 11-bit number.

## **Automatic Powerdown**

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered down. From this powerdown state, the ADC requires 40 system clock cycles to powerup. The ADC powers up when a conversion is requested by the ADC Control register.

## **Single-Shot Conversion**

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. Follow the steps below for setting up the ADC and initiating a single-shot conversion:

1. Enable the acceptable analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
2. Write the ADC Control/Status Register 1 to configure the ADC
  - Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
3. Write to the ADC Control Register 0 to configure the ADC and begin the conversion. The bit fields in the ADC Control register can be written simultaneously:
  - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
  - Clear CONT to 0 to select a single-shot conversion.
  - If the internal voltage reference must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
  - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in the ADC Control Register 0.
  - Set CEN to 1 to start the conversion.
4. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power-up before beginning the 5129 cycle conversion.

## ADC Data Low Bits Register

The ADC Data Low Byte register contains the lower bits of the ADC output as well as an overflow status bit. The output is a 11-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte register is read-only. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

**Table 75. ADC Data Low Bits Register (ADCD\_L)**

BITS	7	6	5	4	3	2	1	0
FIELD	ADCDL			Reserved				OVF
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F73H							

ADCDL—ADC Data Low Bits

These bits are the least significant three bits of the 11-bits of the ADC output. These bits are undefined after a Reset.

Reserved—Undefined when read

OVF—Overflow Status

0= An overflow did not occur in the digital filter for the current sample

1= An overflow did occur in the digital filter for the current sample

**Table 116. Opcode Map Abbreviations**

<b>Abbreviation</b>	<b>Description</b>	<b>Abbreviation</b>	<b>Description</b>
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair



		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	1.1 <b>BRK</b> IM	2.2 <b>SRP</b> IM	2.3 <b>ADD</b> r1,r2	2.4 <b>ADD</b> r1,l,r2	3.3 <b>ADD</b> R2,R1	3.4 <b>ADD</b> IR2,R1	3.3 <b>ADD</b> R1,IM	3.4 <b>ADD</b> IR1,IM	4.3 <b>ADDX</b> ER2,ER1	4.3 <b>ADDX</b> IM,ER1	2.3 <b>DJNZ</b> r1,X	2.2 <b>JR</b> cc,X	2.2 <b>LD</b> r1,IM	3.2 <b>JP</b> cc,DA	1.2 <b>INC</b> r1	1.2 <b>NOP</b>
	1	2.2 <b>RLC</b> R1	2.3 <b>RLC</b> IR1	2.3 <b>ADC</b> r1,r2	2.4 <b>ADC</b> r1,l,r2	3.3 <b>ADC</b> R2,R1	3.4 <b>ADC</b> IR2,R1	3.3 <b>ADC</b> R1,IM	3.4 <b>ADC</b> IR1,IM	4.3 <b>ADCX</b> ER2,ER1	4.3 <b>ADCX</b> IM,ER1	↓	↓	↓	↓	↓	See 2nd Opcode Map
	2	2.2 <b>INC</b> R1	2.3 <b>INC</b> IR1	2.3 <b>SUB</b> r1,r2	2.4 <b>SUB</b> r1,l,r2	3.3 <b>SUB</b> R2,R1	3.4 <b>SUB</b> IR2,R1	3.3 <b>SUB</b> R1,IM	3.4 <b>SUB</b> IR1,IM	4.3 <b>SUBX</b> ER2,ER1	4.3 <b>SUBX</b> IM,ER1						1, 2 ATM
	3	2.2 <b>DEC</b> R1	2.3 <b>DEC</b> IR1	2.3 <b>SBC</b> r1,r2	2.4 <b>SBC</b> r1,l,r2	3.3 <b>SBC</b> R2,R1	3.4 <b>SBC</b> IR2,R1	3.3 <b>SBC</b> R1,IM	3.4 <b>SBC</b> IR1,IM	4.3 <b>SBCX</b> ER2,ER1	4.3 <b>SBCX</b> IM,ER1						
	4	2.2 <b>DA</b> R1	2.3 <b>DA</b> IR1	2.3 <b>OR</b> r1,r2	2.4 <b>OR</b> r1,l,r2	3.3 <b>OR</b> R2,R1	3.4 <b>OR</b> IR2,R1	3.3 <b>OR</b> R1,IM	3.4 <b>OR</b> IR1,IM	4.3 <b>ORX</b> ER2,ER1	4.3 <b>ORX</b> IM,ER1						
	5	2.2 <b>POP</b> R1	2.3 <b>POP</b> IR1	2.3 <b>AND</b> r1,r2	2.4 <b>AND</b> r1,l,r2	3.3 <b>AND</b> R2,R1	3.4 <b>AND</b> IR2,R1	3.3 <b>AND</b> R1,IM	3.4 <b>AND</b> IR1,IM	4.3 <b>ANDX</b> ER2,ER1	4.3 <b>ANDX</b> IM,ER1						1.2 WDT
	6	2.2 <b>COM</b> R1	2.3 <b>COM</b> IR1	2.3 <b>TCM</b> r1,r2	2.4 <b>TCM</b> r1,l,r2	3.3 <b>TCM</b> R2,R1	3.4 <b>TCM</b> IR2,R1	3.3 <b>TCM</b> R1,IM	3.4 <b>TCM</b> IR1,IM	4.3 <b>TCMX</b> ER2,ER1	4.3 <b>TCMX</b> IM,ER1						1.2 STOP
	7	2.2 <b>PUSH</b> R2	2.3 <b>PUSH</b> IR2	2.3 <b>TM</b> r1,r2	2.4 <b>TM</b> r1,l,r2	3.3 <b>TM</b> R2,R1	3.4 <b>TM</b> IR2,R1	3.3 <b>TM</b> R1,IM	3.4 <b>TM</b> IR1,IM	4.3 <b>TMX</b> ER2,ER1	4.3 <b>TMX</b> IM,ER1						1.2 HALT
	8	2.5 <b>DECW</b> RR1	2.6 <b>DECW</b> IRR1	2.5 <b>LDE</b> r1,l,r2	2.9 <b>LDEI</b> l,r1,l,r2	3.2 <b>LDX</b> r1,ER2	3.3 <b>LDX</b> l,r1,ER2	3.4 <b>LDX</b> IRR2,R1	3.5 <b>LDX</b> IRR2,IR1	3.4 <b>LDX</b> r1,r2,X	3.4 <b>LDX</b> rr1,r2,X						1.2 DI
	9	2.2 <b>RL</b> R1	2.3 <b>RL</b> IR1	2.5 <b>LDE</b> r2,l,r1	2.9 <b>LDEI</b> l,r2,l,r1	3.2 <b>LDX</b> r2,ER1	3.3 <b>LDX</b> l,r2,ER1	3.4 <b>LDX</b> R2,IRR1	3.5 <b>LDX</b> IR2,IRR1	3.3 <b>LEA</b> r1,r2,X	3.5 <b>LEA</b> rr1,r2,X						1.2 EI
	A	2.5 <b>INCW</b> RR1	2.6 <b>INCW</b> IRR1	2.3 <b>CP</b> r1,r2	2.4 <b>CP</b> r1,l,r2	3.3 <b>CP</b> R2,R1	3.4 <b>CP</b> IR2,R1	3.3 <b>CP</b> R1,IM	3.4 <b>CP</b> IR1,IM	4.3 <b>CPX</b> ER2,ER1	4.3 <b>CPX</b> IM,ER1						1.4 RET
	B	2.2 <b>CLR</b> R1	2.3 <b>CLR</b> IR1	2.3 <b>XOR</b> r1,r2	2.4 <b>XOR</b> r1,l,r2	3.3 <b>XOR</b> R2,R1	3.4 <b>XOR</b> IR2,R1	3.3 <b>XOR</b> R1,IM	3.4 <b>XOR</b> IR1,IM	4.3 <b>XORX</b> ER2,ER1	4.3 <b>XORX</b> IM,ER1						1.5 IRET
	C	2.2 <b>RRC</b> R1	2.3 <b>RRC</b> IR1	2.5 <b>LDC</b> r1,l,r2	2.9 <b>LDCI</b> l,r1,l,r2	2.3 <b>JP</b> IRR1	2.9 <b>LDC</b> l,r1,l,r2		3.4 <b>LD</b> r1,r2,X	3.2 <b>PUSHX</b> ER2							1.2 RCF
	D	2.2 <b>SRA</b> R1	2.3 <b>SRA</b> IR1	2.5 <b>LDC</b> r2,l,r1	2.9 <b>LDCI</b> l,r2,l,r1	2.6 <b>CALL</b> IRR1	2.2 <b>BSWAP</b> R1	3.3 <b>CALL</b> DA	3.4 <b>LD</b> r2,r1,X	3.2 <b>POPX</b> ER1							1.2 SCF
	E	2.2 <b>RR</b> R1	2.3 <b>RR</b> IR1	2.2 <b>BIT</b> p,b,r1	2.3 <b>LD</b> r1,l,r2	3.2 <b>LD</b> R2,R1	3.3 <b>LD</b> IR2,R1	3.2 <b>LD</b> R1,IM	3.3 <b>LD</b> IR1,IM	4.2 <b>LDX</b> ER2,ER1	4.2 <b>LDX</b> IM,ER1						1.2 CCF
	F	2.2 <b>SWAP</b> R1	2.3 <b>SWAP</b> IR1	2.6 <b>TRAP</b> Vector	2.3 <b>LD</b> l,r1,r2	2.8 <b>MULT</b> RR1	3.3 <b>LD</b> R2,IR1	3.3 <b>BTJ</b> p,b,r1,X	3.4 <b>BTJ</b> p,b,l,r1,X								

Figure 27. First Opcode Map

**Table 125. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)**

Symbol	Parameter	V <sub>DD</sub> = 3.0 V to 3.6 V T <sub>A</sub> = 0 °C to +70 °C (unless otherwise stated)			Units	Conditions
		Minimum	Typical	Maximum		
Z <sub>in</sub>	Input Impedance	–	150		kΩ	In unbuffered mode at 20 MHz <sup>5</sup>
V <sub>in</sub>	Input Voltage Range	0		V <sub>DD</sub>	V	Unbuffered Mode
<b>Notes</b> <ol style="list-style-type: none"> <li>1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.</li> <li>2. Devices are factory calibrated at V<sub>DD</sub> = 3.3 V and T<sub>A</sub> = +30 °C, so the ADC is maximally accurate under these conditions.</li> <li>3. LSBs are defined assuming 10-bit resolution.</li> <li>4. This is the maximum recommended resistance seen by the ADC input pin.</li> <li>5. The input impedance is inversely proportional to the system clock frequency.</li> </ol>						

**Table 126. Comparator Electrical Characteristics**

Symbol	Parameter	V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = -40 °C to +105 °C			Units	Conditions
		Minimum	Typical	Maximum		
V <sub>OS</sub>	Input DC Offset		5		mV	
V <sub>CREF</sub>	Programmable Internal Reference Voltage		±5		%	20-/28-pin devices
			±3		%	8-pin devices
T <sub>PROP</sub>	Propagation Delay		200		ns	
V <sub>HYS</sub>	Input Hysteresis		4		mV	
V <sub>IN</sub>	Input Voltage Range	V <sub>SS</sub>		V <sub>DD</sub> -1	V	

## General Purpose I/O Port Input Data Sample Timing

Figure 29 displays timing of the GPIO Port input sampling. The input value on a GPIO Port pin is sampled on the rising edge of the system clock. The Port value is available to the eZ8 CPU on the second rising clock edge following the change of the Port value.

# Packaging

Figure 34 displays the 8-pin Plastic Dual Inline Package (PDIP) available for the Z8 Encore! XP® F0823 Series devices.

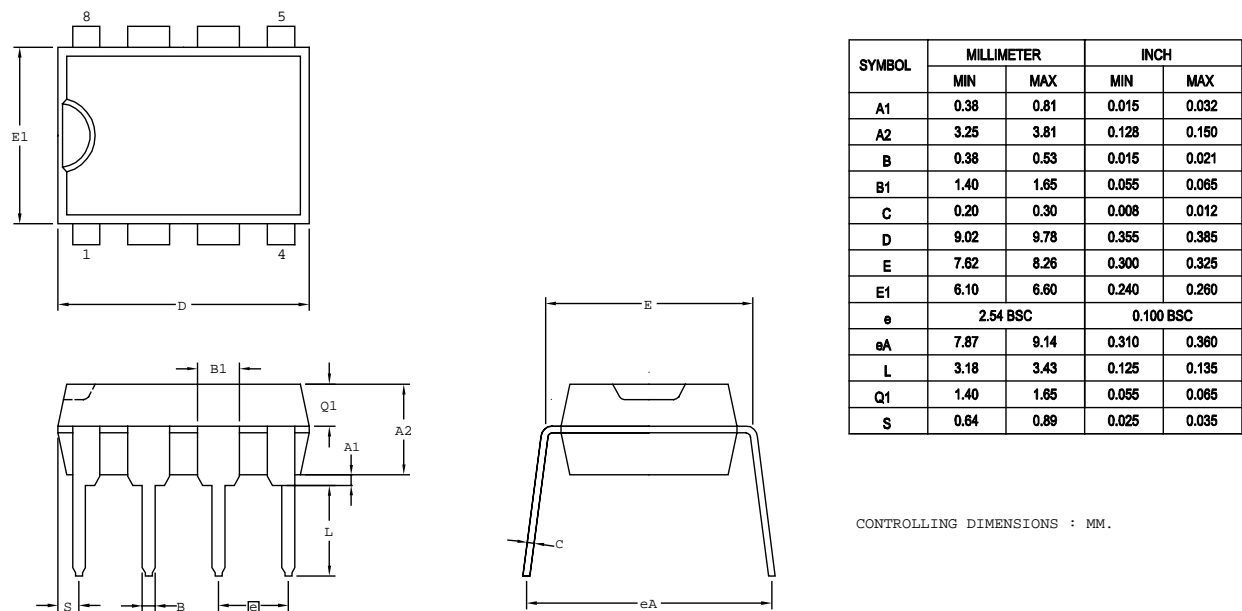


Figure 34. 8-Pin Plastic Dual Inline Package (PDIP)

Figure 35 displays the 8-pin Small Outline Integrated Circuit package (SOIC) available for the Z8 Encore! XP F0823 Series devices.

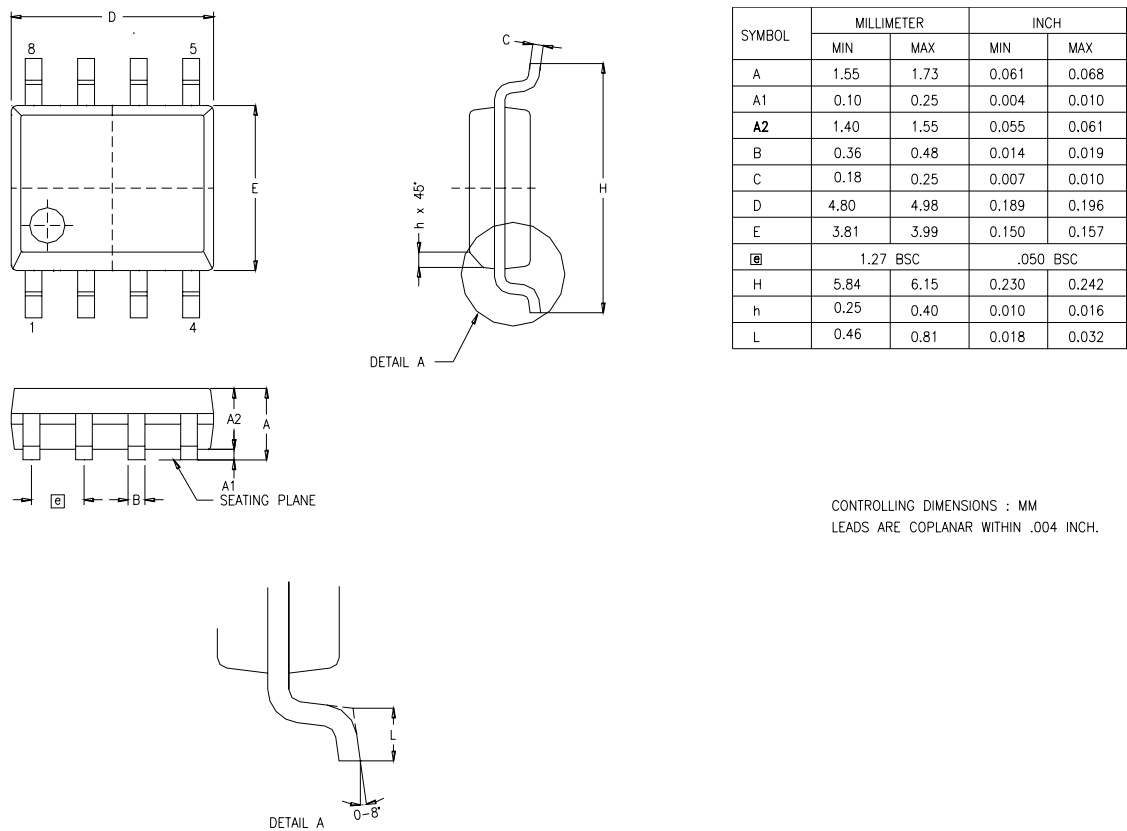


Figure 35. 8-Pin Small Outline Integrated Circuit Package (SOIC)

Figure 41 displays the 28-pin Small Outline Integrated Circuit package (SOIC) available in Z8 Encore! XP F0823 Series devices.

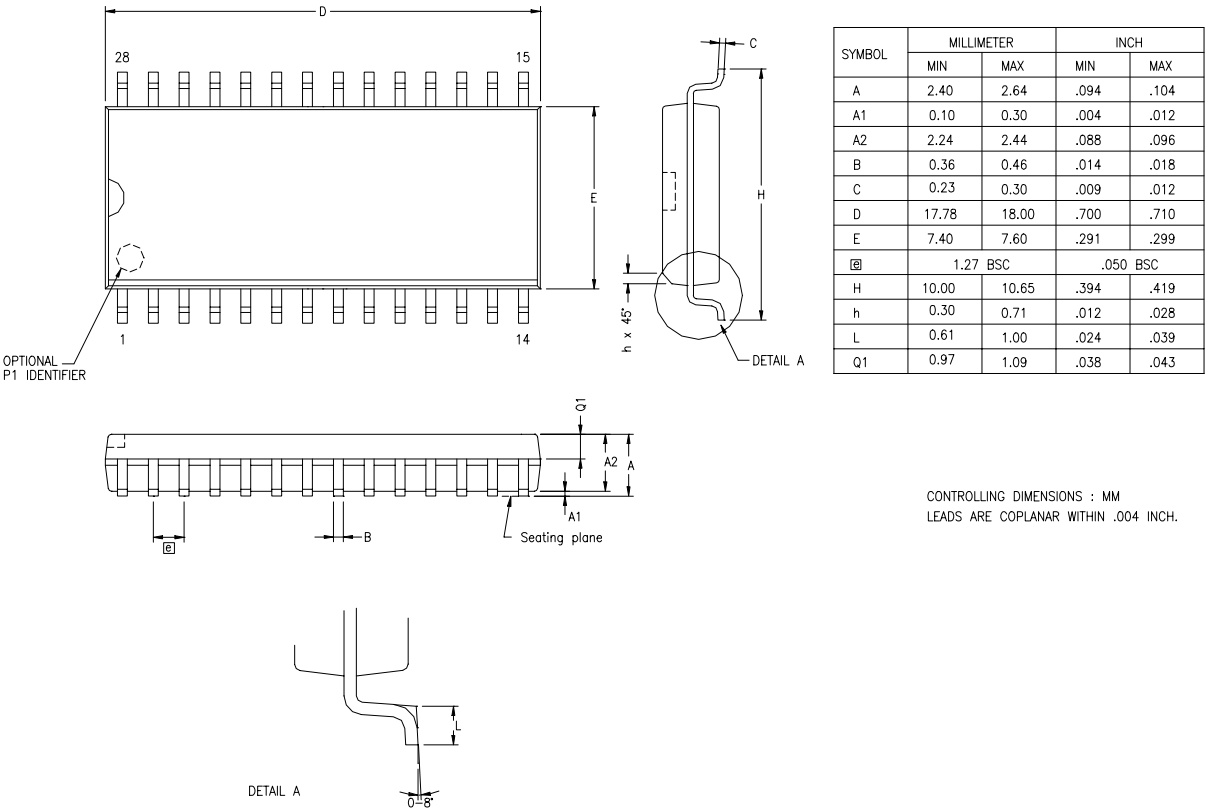


Figure 41. 28-Pin Small Outline Integrated Circuit Package (SOIC)