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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 5MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0423hj005sc |

**Warning:** DO NOT USE IN LIFE SUPPORT

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**Table 8. Register File Address Map (Continued)**

| Address (Hex) | Register Description | Mnemonic | Reset (Hex) | Page No |
|---|---|---|---|---|
| FF2 | Watchdog Timer Reload High Byte | WDTH | FF | 91 |
| FF3 | Watchdog Timer Reload Low Byte | WDTL | FF | 91 |
| FF4–FF5 | Reserved | — | XX | |
| **Trim Bit Control** | | | | |
| FF6 | Trim Bit Address | TRMADR | 00 | 143 |
| FF7 | Trim Data | TRMDR | XX | 144 |
| **Flash Memory Controller** | | | | |
| FF8 | Flash Control | FCTL | 00 | 137 |
| FF8 | Flash Status | FSTAT | 00 | 137 |
| FF9 | Flash Page Select | FPS | 00 | 138 |
| | Flash Sector Protect | FPROT | 00 | 139 |
| FFA | Flash Programming Frequency High Byte | FFREQH | 00 | 140 |
| FFB | Flash Programming Frequency Low Byte | FFREQL | 00 | 140 |
| **eZ8 CPU** | | | | |
| FFC | Flags | — | XX | Refer to *eZ8 CPU Core User Manual (UM0128)* |
| FFD | Register Pointer | RP | XX | |
| FFE | Stack Pointer High Byte | SPH | XX | |
| FFF | Stack Pointer Low Byte | SPL | XX | |

XX=Undefined

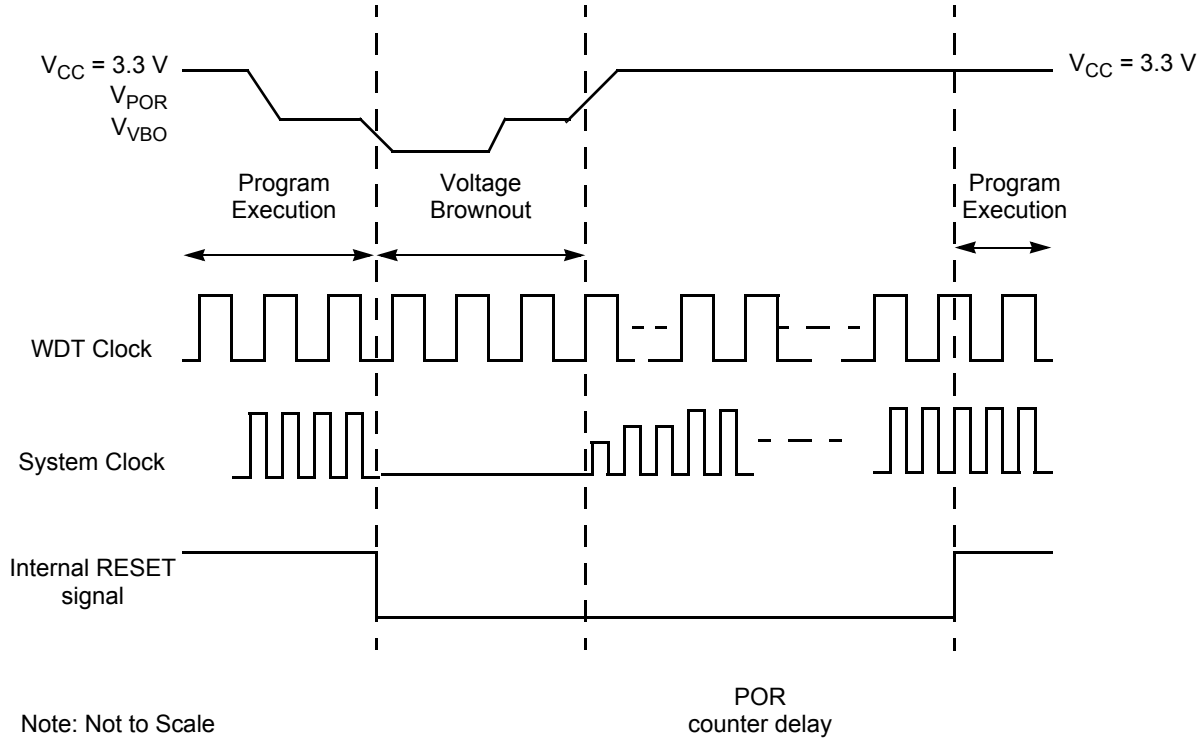



**Figure 6. Voltage Brownout Reset Operation**

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a POR after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is in NORMAL or STOP mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT status bit in the WDT Control register is set to signify that the reset was initiated by the Watchdog Timer.

## External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system

vector address. Following Stop Mode Recovery, the STOP bit in the Watchdog Timer Control Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The section following the table provides more detailed information on each of the Stop Mode Recovery sources.

**Table 11. Stop Mode Recovery Sources and Resulting Action**

| Operating Mode | Stop Mode Recovery Source | Action |
|---|---|---|
| STOP mode | Watchdog Timer time-out when configured for Reset | Stop Mode Recovery |
| | Watchdog Timer time-out when configured for interrupt | Stop Mode Recovery followed by interrupt (if interrupts are enabled) |
| | Data transition on any GPIO port pin enabled as a Stop Mode Recovery source | Stop Mode Recovery |
| | Assertion of external $\overline{\text{RESET}}$ Pin | System Reset |
| | Debug Pin driven Low | System Reset |

## Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP mode, the device undergoes a Stop Mode Recovery sequence. In the Watchdog Timer Control register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and Z8 Encore! XP® F0823 Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

## Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins can be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

**Note:** *The SMR pulses shorter than specified does not trigger a recovery. When this happens, the STOP bit in the Reset Status (RSTSTAT) register is set to 1.*

**Caution:** *In STOP mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin can initiate Stop Mode Recovery without being written to the Port Input Data register or without initiating an interrupt (if enabled for that pin).*

- Writing a 1 to the IRQE bit in the Interrupt Control register

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control register
- Reset
- Execution of a Trap instruction
- Illegal Instruction Trap
- Primary Oscillator Fail Trap
- Watchdog Timer Oscillator Fail Trap

## Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all interrupts are enabled with identical interrupt priority (for example, all as Level 2 interrupts), the interrupt priority is assigned from highest to lowest as specified in Table 33 on page 54. Level 3 interrupts are always assigned higher priority than Level 2 interrupts which, in turn, always are assigned higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 33. Reset, Watchdog Timer interrupt (if enabled), Primary Oscillator Fail Trap, Watchdog Timer Oscillator Fail Trap, and Illegal Instruction Trap always have highest (Level 3) priority.

## Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.

**Caution:** *The following coding style that clears bits in the Interrupt Request registers is not recommended. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost.*

**Poor coding style that can result in lost interrupt requests:**

```
LDX r0, IRQ0
AND r0, MASK
LDX IRQ0, r0
```

**Table 48. Interrupt Control Register (IRQCTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | IRQE | Reserved | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R | R | R | R | R | R | R |
| ADDR | FCFH | | | | | | | |

IRQE—Interrupt Request Enable
This bit is set to 1 by executing an `EI` (Enable Interrupts) or `IRET` (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, reset or by a direct register write of a 0 to this bit.
0 = Interrupts are disabled
1 = Interrupts are enabled

Reserved—0 when read

of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in TxCTL1 register is set to indicate the timer interrupt is because of an input capture event.

The timer continues counting up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt and continues counting. The INPCAP bit in TxCTL1 register clears indicating the timer interrupt is not because of an input capture event.

Follow the steps below for configuring a timer for CAPTURE mode and initiating the count:

1. Write to the Timer Control register to:
   - Disable the timer
   - Configure the timer for CAPTURE mode
   - Set the prescale value
   - Set the Capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a Capture or a Reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

### CAPTURE RESTART Mode

In CAPTURE RESTART mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is

## Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Follow the steps below to configure the UART receiver for interrupt-driven operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
5. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
   - Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR mode
   - Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme
   - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! XP devices without a DMA block)
7. Write the device address to the Address Compare Register (automatic MULTIPROCESSOR modes only).
8. Write to the UART Control 0 register to:
   - Set the receive enable bit (REN) to enable the UART for data reception
   - Enable parity, if appropriate and if multiprocessor mode is not enabled, and select either even or odd parity
9. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

1. Checks the UART Status 0 register to determine the source of the interrupt - error, break, or received data.
2. Reads the data from the UART Receive Data register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) mode, further actions may be required depending on the MULTIPROCESSOR mode bits MPMD[1:0].

### Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data register before the Transmit shift register completes shifting the current character. Writing to the UART Transmit Data register clears the TDRE bit to 0.

### Receiver Interrupts

The receiver generates an interrupt when any of the following occurs:

- A data byte is received and is available in the UART Receive Data register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

**Note:** *In MULTIPROCESSOR mode (MPEN = 1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.*

- A break is received
- An overrun is detected
- A data framing error is detected

### UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data register contains a data byte. However, because the overrun error occurred, this byte cannot contain valid data and must be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status byte indicating an overrun error, the Receive Data register must be read again to clear the error bits is the UART Status 0 register. Updates to the Receive Data register occur only when the next data word is received.

### UART Data and Error Handling Procedure

Figure 15 displays the recommended procedure for use in UART receiver interrupt service routines.

# Oscillator Control

Z8 Encore! XP® F0823 Series devices uses three possible clocking schemes, each user-selectable:

- On-chip precision trimmed RC oscillator
- External clock drive
- On-chip low power Watchdog Timer oscillator

In addition, Z8 Encore! XP F0823 Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the primary oscillator.

## Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures. A description of the specific operation of each oscillator is outlined elsewhere in this document.

### System Clock Selection

The oscillator control block selects from the available clocks. Table 101 details each clock source and its usage.

**Table 101. Oscillator Configuration and Selection**

| Clock Source | Characteristics | Required Setup |
|---|---|---|
| Internal Precision RC Oscillator | • 32.8 kHz or 5.53 MHz<br>• ± 4% accuracy when trimmed<br>• No external components required | • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator at either 5.53 MHz or 32.8 kHz |
| External Clock Drive | • 0 to 20 MHz<br>• Accuracy dependent on external clock source | • Write GPIO registers to configure PB3 pin for external clock function<br>• Unlock and write OSCCTL to select external system clock<br>• Apply external clock signal to GPIO |
| Internal Watchdog Timer Oscillator | • 10 kHz nominal<br>• ± 40% accuracy; no external components required<br>• Very Low power consumption | • Enable WDT if not enabled and wait until WDT Oscillator is operating.<br>• Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator |

**Table 115. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Opcode(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HALT | HALT Mode | | | 7F | – | – | – | – | – | – | 1 | 2 |
| INC dst | dst ← dst + 1 | R | | 20 | – | * | * | – | – | – | 2 | 2 |
| | | IR | | 21 | | | | | | | 2 | 3 |
| | | r | | 0E-FE | | | | | | | 1 | 2 |
| INCW dst | dst ← dst + 1 | RR | | A0 | – | * | * | * | – | – | 2 | 5 |
| | | IRR | | A1 | | | | | | | 2 | 6 |
| IRET | FLAGS ← @SP<br>SP ← SP + 1<br>PC ← @SP<br>SP ← SP + 2<br>IRQCTL[7] ← 1 | | | BF | * | * | * | * | * | * | 1 | 5 |
| JP dst | PC ← dst | DA | | 8D | – | – | – | – | – | – | 3 | 2 |
| | | IRR | | C4 | | | | | | | 2 | 3 |
| JP cc, dst | if cc is true<br>PC ← dst | DA | | 0D-FD | – | – | – | – | – | – | 3 | 2 |
| JR dst | PC ← PC + X | DA | | 8B | – | – | – | – | – | – | 2 | 2 |
| JR cc, dst | if cc is true<br>PC ← PC + X | DA | | 0B-FB | – | – | – | – | – | – | 2 | 2 |
| LD dst, rc | dst ← src | r | IM | 0C-FC | – | – | – | – | – | – | 2 | 2 |
| | | r | X(r) | C7 | | | | | | | 3 | 3 |
| | | X(r) | r | D7 | | | | | | | 3 | 4 |
| | | r | Ir | E3 | | | | | | | 2 | 3 |
| | | R | R | E4 | | | | | | | 3 | 2 |
| | | R | IR | E5 | | | | | | | 3 | 4 |
| | | R | IM | E6 | | | | | | | 3 | 2 |
| | | IR | IM | E7 | | | | | | | 3 | 3 |
| | | Ir | r | F3 | | | | | | | 2 | 3 |
| | | IR | R | F5 | | | | | | | 3 | 3 |
| Flags Notation: | * = Value is a function of the result of the operation.<br>– = Unaffected<br>X = Undefined | | | | 0 = Reset to 0<br>1 = Set to 1 | | | | | | | |

| Upper Nibble (Hex) \ Lower Nibble (Hex) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | |
| 7 | 3, 2 **PUSH** IM | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | |
| A | | | 3.3 **CPC** r1,r2 | 3.4 **CPC** r1,Ir2 | 4.3 **CPC** R2,R1 | 4.4 **CPC** IR2,R1 | 4.3 **CPC** R1,IM | 4.4 **CPC** IR1,IM | 5.3 **CPCX** ER2,ER1 | 5.3 **CPCX** IM,ER1 | | | | | | |
| B | | | | | | | | | | | | | | | | |
| C | 3.2 **SRL** R1 | 3.3 **SRL** IR1 | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | | | |
| E | | | | | | | | | 5, 4 **LDWX** ER2,ER1 | | | | | | | |
| F | | | | | | | | | | | | | | | | |

**Figure 28. Second Opcode Map after 1FH**

**Table 118. DC Characteristics (Continued)**

| Symbol | Parameter | $T_A$ = -40 °C to +105 °C (unless otherwise specified) | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | | |
| $V_{OH2}$ | High Level Output Voltage | 2.4 | – | – | V | $I_{OH}$ = -20 mA; $V_{DD}$ = 3.3 V High Output Drive enabled. |
| $I_{IH}$ | Input Leakage Current | – | ±0.002 | ±5 | µA | $V_{IN} = V_{DD}$ $V_{DD}$ = 3.3 V; |
| $I_{IL}$ | Input Leakage Current | – | ±0.007 | ±5 | µA | $V_{IN} = V_{SS}$ $V_{DD}$ = 3.3 V; |
| $I_{TL}$ | Tristate Leakage Current | – | – | ±5 | µA | |
| $I_{LED}$ | Controlled Current Drive | 1.8 | 3 | 4.5 | mA | {AFS2,AFS1} = {0,0} |
| | | 2.8 | 7 | 10.5 | mA | {AFS2,AFS1} = {0,1} |
| | | 7.8 | 13 | 19.5 | mA | {AFS2,AFS1} = {1,0} |
| | | 12 | 20 | 30 | mA | {AFS2,AFS1} = {1,1} |
| $C_{PAD}$ | GPIO Port Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XIN}$ | XIN Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XOUT}$ | XOUT Pad Capacitance | – | 9.5[2] | – | pF | |
| $I_{PU}$ | Weak Pull-up Current | 30 | 100 | 350 | µA | $V_{DD}$ = 3.0 V–3.6 V |
| $V_{RAM}$ | RAM Data Retention Voltage | TBD | | | V | Voltage at which RAM retains static values; no reading or writing is allowed. |

**Notes**
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.

# On-Chip Peripheral AC and DC Electrical Characteristics

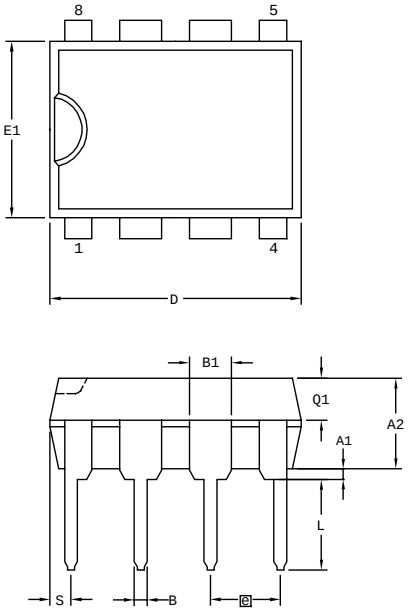
**Table 122. Power-On Reset and Voltage Brownout Electrical Characteristics and Timing**

| | | $T_A$ = -40 °C to +105 °C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical[1]** | **Maximum** | **Units** | **Conditions** |
| $V_{POR}$ | Power-On Reset Voltage Threshold | 2.20 | 2.45 | 2.70 | V | $V_{DD} = V_{POR}$ |
| $V_{VBO}$ | Voltage Brownout Reset Voltage Threshold | 2.15 | 2.40 | 2.65 | V | $V_{DD} = V_{VBO}$ |
| | $V_{POR}$ to $V_{VBO}$ hysteresis | | 50 | 75 | mV | |
| | Starting $V_{DD}$ voltage to ensure valid Power-On Reset. | – | $V_{SS}$ | – | V | |
| $T_{ANA}$ | Power-On Reset Analog Delay | – | 70 | – | µs | $V_{DD} > V_{POR}$; $T_{POR}$ Digital Reset delay follows $T_{ANA}$ |
| $T_{POR}$ | Power-On Reset Digital Delay | | 16 | | µs | 66 Internal Precision Oscillator cycles + IPO startup time ($T_{IPOST}$) |
| $T_{SMR}$ | Stop Mode Recovery | | 16 | | µs | 66 Internal Precision Oscillator cycles |
| $T_{VBO}$ | Voltage Brownout Pulse Rejection Period | – | 10 | – | µs | Period of time in which $V_{DD} < V_{VBO}$ without generating a Reset. |
| $T_{RAMP}$ | Time for $V_{DD}$ to transition from $V_{SS}$ to $V_{POR}$ to ensure valid Reset | 0.10 | – | 100 | ms | |
| $T_{SMP}$ | Stop Mode Recovery pin pulse rejection period | | 20 | | ns | For any SMR pin or for the Reset pin when it is asserted in STOP mode. |

[1]Data in the typical column is from characterization at 3.3 V and 30 °C. These values are provided for design guidance only and are not tested in production.

# Packaging

Figure 34 displays the 8-pin Plastic Dual Inline Package (PDIP) available for the Z8 Encore! XP® F0823 Series devices.




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.38 | 0.81 | 0.015 | 0.032 |
| A2 | 3.25 | 3.81 | 0.128 | 0.150 |
| B | 0.38 | 0.53 | 0.015 | 0.021 |
| B1 | 1.40 | 1.65 | 0.055 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 9.02 | 9.78 | 0.355 | 0.385 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E1 | 6.10 | 6.60 | 0.240 | 0.260 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.87 | 9.14 | 0.310 | 0.360 |
| L | 3.18 | 3.43 | 0.125 | 0.135 |
| Q1 | 1.40 | 1.65 | 0.055 | 0.065 |
| S | 0.64 | 0.89 | 0.025 | 0.035 |

CONTROLLING DIMENSIONS : MM.

**Figure 34. 8-Pin Plastic Dual Inline Package (PDIP)**

# Ordering Information

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP with 8 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | |
| **Standard Temperature: 0 °C to 70 °C** | | | | | | | | |
| Z8F0823PB005SC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0823QB005SC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0823SB005SC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0823SH005SC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0823HH005SC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0823PH005SC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0823SJ005SC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0823HJ005SC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0823PJ005SC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| **Extended Temperature: -40 °C to 105 °C** | | | | | | | | |
| Z8F0823PB005EC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0823QB005EC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0823SB005EC | 8 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0823SH005EC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0823HH005EC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0823PH005EC | 8 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0823SJ005EC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0823HJ005EC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0823PJ005EC | 8 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| Replace C with G for Lead-Free Packaging | | | | | | | | |

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP with 4 KB Flash** | | | | | | | | |
| **Standard Temperature: 0 °C to 70 °C** | | | | | | | | |
| Z8F0413PB005SC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0413QB005SC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0413SB005SC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0413SH005SC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0413HH005SC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0413PH005SC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0413SJ005SC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0413HJ005SC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0413PJ005SC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |
| **Extended Temperature: -40 °C to 105 °C** | | | | | | | | |
| Z8F0413PB005EC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0413QB005EC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0413SB005EC | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0413SH005EC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0413HH005EC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0413PH005EC | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0413SJ005EC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0413HJ005EC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0413PJ005EC | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |
| Replace C with G for Lead-Free Packaging | | | | | | | | |

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP® F0823 Series Development Kit** | | | | | | | | |
| **Z8F08A28100KITG** | | | | | | | | **Z8 Encore! XP F082A Series Development Kit (20- and 28-Pin)** |
| **Z8F04A28100KITG** | | | | | | | | **Z8 Encore! XP F042A Series Development Kit (20- and 28-Pin)** |
| **Z8F04A08100KITG** | | | | | | | | **Z8 Encore! XP F042A Series Development Kit (8-Pin)** |
| **ZUSBSC00100ZACG** | | | | | | | | **USB Smart Cable Accessory Kit** |
| **ZUSBOPTSC01ZACG** | | | | | | | | **Opto-Isolated USB Smart Cable Accessory Kit** |
| **ZENETSC0100ZACG** | | | | | | | | **Ethernet Smart Cable Accessory Kit** |

## P



## R