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Zilog - Z8F0423SH005EC Datasheet



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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0423sh005ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Pin Description

Z8 Encore! XP[®] F0823 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and pin configurations available for each of the package styles. For information on physical package specifications, see Packaging on page 209.

Available Packages

Table 2 lists the package styles that are available for each device in the Z8 Encore! XP F0823 Series product line.

Part Number	ADC	8-pin PDIP	8-pin SOIC	20-pin PDIP	20-pin SOIC	20-pin SSOP	28-pin PDIP	28-pin SOIC	28-pin SSOP	8-pin QFN/ MLF-S
Z8F0823	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0813	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0423	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0413	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0223	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0213	No	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0123	Yes	Х	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0113	No	Х	Х	Х	Х	Х	Х	Х	Х	Х

Table 2. Z8 Encore! XP F0823 Series Package Options

Pin Configurations

Figure 2 through Figure 4 displays the pin configurations for all packages available in the Z8 Encore! XP F0823 Series. For description of signals, see Table 3. The analog input alternate functions (ANA*x*) are not available on the Z8F0x13 devices. The analog supply pins (AV_{DD} and AV_{SS}) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all pins of Ports A, B, and C default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general-purpose input ports until programmed otherwise.

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Table 3.	Signal	Descriptions	(Continued)	
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Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	I	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD.
		Caution: The DBG pin is open-drain and requires an external pull- up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V _{DD}	Ι	Digital Power Supply.
AV _{DD}	I	Analog Power Supply.
V _{SS}	I	Digital Ground.
AV _{SS}	Ι	Analog Ground.
Note: The AV _{DD} and A PB7 on 28-pin pa	.V _{SS} sigr ackages	nals are available only in 28-pin packages with ADC. They are replaced by PB6 and without ADC.

Pin Characteristics

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

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Table 32. LED Drive Level Low Register (LEDLVLL)

BITS	7	6	5	4	3	2	1	0	
FIELD		LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR				F8	4H				

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA 01 = 7 mA10 = 13 mA

10 = 13 mA11 = 20 mA

BITS	7	6	5	4	3	2	1	0
FIELD	IRQE				Reserved			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R
ADDR				FC	FH			

Table 48. Interrupt Control Register (IRQCTL)

IRQE—Interrupt Request Enable

This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, reset or by a direct register write of a 0 to this bit.

0 = Interrupts are disabled

1 = Interrupts are enabled

Reserved—0 when read

In COMPARE mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

Table 51. Timer 0–1 Reload High Byte Register (TxRH)

BITS	7	6	5	4	3	2	1	0		
FIELD		TRH								
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR		F02H, F0AH								

Table 52. Timer 0–1 Reload Low Byte Register (TxRL)

BITS	7	6	5	4	3	2	1	0		
FIELD		TRL								
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR		F03H, F0BH								

TRH and TRL—Timer Reload Register High and Low

These two bytes form the 16-bit Reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to 0001H. In Compare mode, these two bytes form the 16-bit Compare value.

Timer 0-1 PWM High and Low Byte Registers

The Timer 0-1 PWM High and Low Byte (TxPWMH and TxPWML) registers (Table 53 and Table 54) control pulse-width modulator (PWM) operations. These registers also store the Capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 53. Timer 0–1 PWM High Byte Register (TxPWMH)

BITS	7	6	5	4	3	2	1	0		
FIELD		PWMH								
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR				F04H,	F0CH					

WDT Reset in NORMAL Operation

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Watchdog Timer Control register is set to 1. For more information on System Reset, see Reset and Stop Mode Recovery on page 21.

WDT Reset in STOP Mode

If configured to generate a Reset when a time-out occurs and the device is in STOP mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Watchdog Timer Control register are set to 1 following WDT time-out in STOP mode. For more information, see Reset and Stop Mode Recovery on page 21.

Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer Control Register (WDTCTL) address unlocks the three Watchdog Timer Reload Byte Registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers. The following sequence is required to unlock the Watchdog Timer Reload Byte Registers (WDTU, WDTH, and WDTL) for write access.

- 1. Write 55H to the Watchdog Timer Control register (WDTCTL).
- 2. Write AAH to the Watchdog Timer Control register (WDTCTL).
- 3. Write the Watchdog Timer Reload Upper Byte register (WDTU).
- 4. Write the Watchdog Timer Reload High Byte register (WDTH).
- 5. Write the Watchdog Timer Reload Low Byte register (WDTL).

All three Watchdog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

Watchdog Timer Control Register Definitions

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL register address unlocks the three

BITS	7	6	5	4	3	2	1	0			
FIELD				COMP	_ADDR						
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F45H									

Table 68. UART Address Compare Register (U0ADDR)

COMP ADDR—Compare Address

This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (Table 69 and Table 70) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 69. UART Baud Rate High Byte Register (U0BRH)

BITS	7	6	5	4	3	2	1	0		
FIELD		BRH								
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR		F46H								

Table 70. UART Baud Rate Low Byte Register (U0BRL)

BITS	7	6	5	4	3	2	1	0					
FIELD		BRL											
RESET	1	1	1	1	1	1	1	1					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
ADDR				F4	F47H								

The UART data rate is calculated using the following equation:

UART Baud Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

For a given UART data rate, calculate the integer baud rate divisor value using the following equation:

UART Baud Rate Divisor Value (BRG) = Round $\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$

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value 63H to the Flash Control register initiates the Mass Erase operation. While the Flash Controller executes the Mass Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Using the On-Chip Debugger, poll the Flash Status register to determine when the Mass Erase operation is complete. When the Mass Erase is complete, the Flash Controller returns to its locked state.

Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Row Programming algorithms by controlling the Flash programming signals directly.

Row programing is recommended for gang programming applications and large volume customers who do not require in-circuit initial programming of the Flash memory. Page Erase operations are also supported when the Flash Controller is bypassed.

For more information on bypassing the Flash Controller, refer to *Third-Party Flash Pro*gramming Support for Z8 Encore! (AN0117) available for download at <u>www.zilog.com</u>.

Flash Controller Behavior in DEBUG Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored
- The Flash Sector Protect register is ignored for programming and erase operations
- Programming operations are not limited to the page selected in the Page Select register
- Bits in the Flash Sector Protect register can be written to one or zero
- The second write of the Page Select register to unlock the Flash Controller is not necessary
- The Page Select register can be written when the Flash Controller is unlocked
- The Mass Erase command is enabled through the Flash Control register
- **Caution:** For security reasons, Flash controller allows only a single page to be opened for write/ erase. When writing multiple Flash pages, the Flash controller must go through the unlock sequence again to select another page.

Flash Control Register Definitions

Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FTCTL) register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL. Page Erase applies only to the active page selected in Flash Page Select register. Mass Erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

BITS	7	6	5	4	3	2	1	0	
FIELD	FCMD								
RESET	0 0 0 0 0 0 0 0								
R/W	w w w w w w w								
ADDR		FF8H							

Table 79. Flash Control Register (FCTL)

FCMD—Flash Command

73H = First unlock command

8CH = Second unlock command

95H = Page Erase command (must be third command in sequence to initiate Page Erase) 63H = Mass Erase command (must be third command in sequence to initiate Mass Erase)

5EH = Enable Flash Sector Protect Register Access

Flash Status Register

The Flash Status register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the write-only Flash Control Register.

Table ov. Flash Status Register (FSTAT)	Table	80.	Flash	Status	Register	(FSTAT)
---	-------	-----	-------	--------	----------	---------

BITS	7	6	5 4 3 2 1 0						
FIELD	Rese	erved	FSTAT						
RESET	0	0	0 0 0 0 0 0						
R/W	R	R	R R R R R R						
ADDR			FF8H						

The randomized lot identifier is a 32 byte binary value, stored in the flash information page (for more details, see Reading the Flash Information Page on page 143 and Randomized Lot Identifier on page 149) and is unaffected by mass erasure of the device's flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash Information Area.

; get value at info address 60 (FE60h)
ldx FPS, #%80 ; enable access to flash info page
ld R0, #%FE
ld R1, #%60
ldc R2, @RR0 ; R2 now contains the calibration value

Flash Option Bit Control Register Definitions

Trim Bit Address Register

The Trim Bit Address (TRMADR) register contains the target address for an access to the trim option bits.

Table 85. Trim Bit Address Register (TRMADR)

BITS	7	6	5	4	3	2	1	0	
FIELD	TRMADR - Trim Bit Address (00H to 1FH)								
RESET	0	0	0	0	0	0	0	0	
R/W	R/W R/W R/W R/W R/W R/W R							R/W	
ADDR	FF6H								

Software Compensation Procedure on page 122. The location of each calibration byte is provided in Table 93 on page 148.

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
60	FE60	Offset	Single-Ended Unbuffered	Internal 2.0 V
08	FE08	Gain High Byte	Single-Ended Unbuffered	Internal 2.0 V
09	FE09	Gain Low Byte	Single-Ended Unbuffered	Internal 2.0 V
63	FE63	Offset	Single-Ended Unbuffered	Internal 1.0 V
0A	FE0A	Gain High Byte	Single-Ended Unbuffered	Internal 1.0 V
0B	FE0B	Gain Low Byte	Single-Ended Unbuffered	Internal 1.0 V
66	FE66	Offset	Single-Ended Unbuffered	External 2.0 V
0C	FE0C	Gain High Byte	Single-Ended Unbuffered	External 2.0 V
0D	FE0D	Gain Low Byte	Single-Ended Unbuffered	External 2.0 V

Table 93. ADC Calibration Data Location

Serialization Data

Table 94. Serial Number at 001C-001F (S_NUM)

BITS	7 6 5 4 3 2 1 0								
FIELD	S_NUM								
RESET									
R/W	R/W R/W								
ADDR	R Information Page Memory 001C-001F								
Note: U =	Note: U = Unchanged by Reset, R/W = Read/Write.								

S NUM— Serial Number Byte

The serial number is a unique four-byte binary value.

OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

- 1. Hold PA2/RESET Low.
- 2. Wait 5 ms for the internal reset sequence to complete.
- 3. Send the following bytes serially to the debug pin:

```
DBG \leftarrow 80H (autobaud)
DBG \leftarrow EBH
DBG \leftarrow 5AH
DBG \leftarrow 70H
DBG \leftarrow CDH (32-bit unlock key)
```

4. Release PA2/RESET. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20- or 28-pin device. To enter DEBUG mode, re-autobaud and write 80H to the OCD control register (see On-Chip Debugger Commands on page 157).

Breakpoints

Execution breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the OCD. If breakpoints are enabled, the OCD enters DEBUG mode and idles the eZ8 CPU. If breakpoints are not enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The OCD contains a 16-bit Runtime Counter. It counts system clock cycles between breakpoints. The counter starts counting when the OCD leaves DEBUG mode and stops counting when it enters DEBUG mode again or when it reaches the maximum count of FFFFH.

Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar non-maskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while searching for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

Caution: It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! XP F0823 Series device ceases functioning and can only be recovered by Power-On Reset.

Oscillator Control Register Definitions

The following section provides the bit definitions for the Oscillator Control register.

Oscillator Control Register

The Oscillator Control register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.

BITS	7	6	5	4	3	2	1	0
FIELD	INTEN	Reserved	WDTEN	POFEN	WDFEN		SCKSEL	
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				F8	6H			

Table 102. Oscillator Control Register (OSCCTL)

Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 26. Figure 27 and Figure 28 provide information about each of the eZ8 CPU instructions. Table 116 lists Opcode Map abbreviations.



Figure 26. Opcode Map Cell Description

Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
сс	Condition code	р	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
lr	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 116. Opcode Map Abbreviations

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Ordering Information

Number	Ę	5	ines	rrupts	8it Timers MM	sit A/D Channels	XT with IrDA	cription
Рац	Flas	RAN	101	Inte	16-E w/P\	10-E	UAF	Des
Z8 Encore! XP with 8 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0 °C to 70 °C								
Z8F0823PB005SC	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005SC	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005SC	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005SC	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005SC	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005SC	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005SC	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005SC	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005SC	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperatur	e: -40 °C	to 105 °C	0					
Z8F0823PB005EC	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005EC	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005EC	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005EC	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005EC	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005EC	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005EC	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005EC	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005EC	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lead	Replace C with G for Lead-Free Packaging							

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP with 2 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0 °C to 70 °C								
Z8F0223PB005SC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005SC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005SC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005SC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005SC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005SC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005SC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005SC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005SC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
Extended Temperatur	re: -40 °C	to 105 °C	2					
Z8F0223PB005EC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005EC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005EC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005EC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005EC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005EC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005EC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005EC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005EC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lea	Replace C with G for Lead-Free Packaging							

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