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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0813hj005ec">https://www.e-xfl.com/product-detail/zilog/z8f0813hj005ec</a>

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**Table 8. Register File Address Map (Continued)**

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F91–FBF	Reserved	—	XX	
<b>Interrupt Controller</b>				
FC0	Interrupt Request 0	IRQ0	00	58
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	60
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	61
FC3	Interrupt Request 1	IRQ1	00	59
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	62
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	62
FC6	Interrupt Request 2	IRQ2	00	60
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	63
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	63
FC9–FCC	Reserved	—	XX	
FCD	Interrupt Edge Select	IRQES	00	64
FCE	Shared Interrupt Select	IRQSS	00	64
FCF	Interrupt Control	IRQCTL	00	65
<b>GPIO Port A</b>				
FD0	Port A Address	PAADDR	00	43
FD1	Port A Control	PACTL	00	45
FD2	Port A Input Data	PAIN	XX	45
FD3	Port A Output Data	PAOUT	00	45
<b>GPIO Port B</b>				
FD4	Port B Address	PBADDR	00	43
FD5	Port B Control	PBCTL	00	45
FD6	Port B Input Data	PBIN	XX	45
FD7	Port B Output Data	PBOUT	00	45
<b>GPIO Port C</b>				
FD8	Port C Address	PCADDR	00	43
FD9	Port C Control	PCCTL	00	45
FDA	Port C Input Data	PCIN	XX	45
FDB	Port C Output Data	PCOUT	00	45
FDC–FEF	Reserved	—	XX	
<b>Watchdog Timer (WDT)</b>				
FF0	Reset Status	RSTSTAT	XX	90
	Watchdog Timer Control	WDTCTL	XX	90
FF1	Watchdog Timer Reload Upper Byte	WDTU	FF	91

# Reset and Stop Mode Recovery

The Reset Controller within the Z8 Encore! XP<sup>®</sup> F0823 Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brownout (VBO)
- Watchdog Timer time-out (when configured by the WDT\_RES Flash Option Bit to initiate a reset)
- External  $\overline{\text{RESET}}$  pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-chip Debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP mode, a Stop Mode Recovery is initiated by either of the following:

- Watchdog Timer time-out
- GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device performs the following function:

- Generates the VBO reset when the supply voltage drops below a minimum safe level

## Reset Types

Z8 Encore! XP F0823 Series provides several different types of Reset operation. Stop Mode Recovery is considered a form of Reset. Table 9 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

clock and reset signals, the required reset duration can be as short as three clock periods and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the  $\overline{\text{RESET}}$  input pin is asserted Low, the Z8 Encore! XP F0823 Series devices remain in the Reset state. If the  $\overline{\text{RESET}}$  pin is held Low beyond the System Reset time-out, the device exits the Reset state on the system clock rising edge following  $\overline{\text{RESET}}$  pin deassertion. Following a System Reset initiated by the external  $\overline{\text{RESET}}$  pin, the EXT status bit in the WDT Control (WDTCTL) register is set to 1.

## External Reset Indicator

During System Reset or when enabled by the GPIO logic (see Port A–C Control Registers on page 44), the  $\overline{\text{RESET}}$  pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows an Z8 Encore! XP F0823 Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO, or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the  $\overline{\text{RESET}}$  pin Low. The  $\overline{\text{RESET}}$  pin is held Low by the internal circuitry until the appropriate delay listed in Table 9 has elapsed.

## On-Chip Debugger Initiated Reset

A POR is initiated using the On-Chip Debugger by setting the RST bit in the OCD Control register. The OCD block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the System Reset. Following the System Reset, the POR bit in the Reset Status (RSTSTAT) register is set.

## Stop Mode Recovery

The device enters into STOP mode when eZ8 CPU executes a STOP instruction. For more details on STOP mode, see Low-Power Modes on page 31. During Stop Mode Recovery, the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay also included the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control register (WDTCTL) and the Oscillator Control register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required or IPO disabling is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset

# General-Purpose Input/Output

Z8 Encore! XP® F0823 Series products support a maximum of 24 port pins (Ports A–C) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality, and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

## GPIO Port Availability By Device

Table 14 lists the port pins available with each device and package type.

**Table 14. Port Availability by Device and Package Type**

Devices	Package	10-Bit ADC	Port A	Port B	Port C	Total I/O
Z8F0823SB, Z8F0823PB Z8F0423SB, Z8F0423PB Z8F0223SB, Z8F0223PB Z8F0123SB, Z8F0123PB	8-pin	Yes	[5:0]	No	No	6
Z8F0813SB, Z8F0813PB Z8F0413SB, Z8F0413PB Z8F0213SB, Z8F0213PB Z8F0113SB, Z8F011vPB	8-pin	No	[5:0]	No	No	6
Z8F0823PH, Z8F0823HH Z8F0423PH, Z8F0423HH Z8F0223PH, Z8F0223HH Z8F0123PH, Z8F0123HH	20-pin	Yes	[7:0]	[3:0]	[3:0]	16
Z8F0813PH, Z8F0813HH Z8F0413PH, Z8F0413HH Z8F0213PH, Z8F0213HH Z8F0113PH, Z8F0113HH	20-pin	No	[7:0]	[3:0]	[3:0]	16
Z8F0823PJ, Z8F0823SJ Z8F0423PJ, Z8F0423SJ Z8F0223PJ, Z8F0223SJ Z8F0123PJ, Z8F0123SJ	28-pin	Yes	[7:0]	[5:0]	[7:0]	22
Z8F0813PJ, Z8F0813SJ Z8F0413PJ, Z8F0413SJ Z8F0213PJ, Z8F0213SJ Z8F0113PJ, Z8F0113SJ	28-pin	No	[7:0]	[7:0]	[7:0]	24



**Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)**

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP/LED Drive	ADC or Comparator Input, or LED drive	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN/ LED Drive	ADC or Comparator Input, or LED drive	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/LED/ VREF*	ADC Analog Input or LED Drive or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		LED	LED drive	AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
		LED	LED Drive	AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
		LED	LED Drive	AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
		LED	LED Drive	AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
		LED	LED Drive	AFS1[7]: 1

**Note:** Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, Alternate Function selection as described in Port A–C Alternate Function Sub-Registers must also be enabled.

\*VREF is available on PC2 in 20-pin parts only.

## Interrupt Control Register Definitions

For all interrupts other than the Watchdog Timer interrupt, the Primary Oscillator Fail Trap, and the Watchdog Timer Oscillator Fail Trap, the interrupt control registers enable individual interrupts, set interrupt priorities, and indicate interrupt requests.

### Interrupt Request 0 Register

The Interrupt Request 0 (IRQ0) register (Table 34) stores the interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ0 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 0 register to determine if any interrupt requests are pending.

**Table 34. Interrupt Request 0 Register (IRQ0)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1I	T0I	U0RXI	U0TXI	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC0H							

Reserved—Must be 0

T1I—Timer 1 Interrupt Request

0 = No interrupt request is pending for Timer 1

1 = An interrupt request from Timer 1 is awaiting service

T0I—Timer 0 Interrupt Request

0 = No interrupt request is pending for Timer 0

1 = An interrupt request from Timer 0 is awaiting service

U0RXI—UART 0 Receiver Interrupt Request

0 = No interrupt request is pending for the UART 0 receiver

1 = An interrupt request from the UART 0 receiver is awaiting service

U0TXI—UART 0 Transmitter Interrupt Request

0 = No interrupt request is pending for the UART 0 transmitter

1 = An interrupt request from the UART 0 transmitter is awaiting service

ADCI—ADC Interrupt Request

0 = No interrupt request is pending for the ADC

1 = An interrupt request from the ADC is awaiting service

**Table 43. IRQ2 Enable and Priority Encoding (Continued)**

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
1	1	Level 3	High

where x indicates the register bits from 0–7.

**Table 44. IRQ2 Enable High Bit Register (IRQ2ENH)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC7H							

Reserved—Must be 0

C3ENH—Port C3 Interrupt Request Enable High Bit

C2ENH—Port C2 Interrupt Request Enable High Bit

C1ENH—Port C1 Interrupt Request Enable High Bit

C0ENH—Port C0 Interrupt Request Enable High Bit

**Table 45. IRQ2 Enable Low Bit Register (IRQ2ENL)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC8H							

Reserved—Must be 0

C3ENL—Port C3 Interrupt Request Enable Low Bit

C2ENL—Port C2 Interrupt Request Enable Low Bit

C1ENL—Port C1 Interrupt Request Enable Low Bit

C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 46) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin.

### **PWM SINGLE OUTPUT Mode**

In PWM SINGLE OUTPUT mode, the timer outputs a PWM output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.

Follow the steps below for configuring a timer for PWM Single Output mode and initiating the PWM operation:

1. Write to the Timer Control register to:
  - Disable the timer
  - Configure the timer for PWM mode
  - Set the prescale value
  - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
6. Configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 register is set to indicate the timer interrupt is because of an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 register is cleared to indicate the timer interrupt is not caused by an input capture event.

Follow the steps below for configuring a timer for CAPTURE RESTART mode and initiating the count:

1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for CAPTURE RESTART mode. Setting the mode also involves writing to TMODEHI bit in TxCTL1 register.
  - Set the prescale value.
  - Set the Capture edge (rising or falling) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a Capture or a Reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input Capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input Capture event or the Reload event by setting TICONFIG field of the TxCTL1 register.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

### **COMPARE Mode**

In COMPARE mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the

**Table 59. Watchdog Timer Reload Upper Byte Register (WDTU)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTU							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF1H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTU—WDT Reload Upper Byte  
Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

**Table 60. Watchdog Timer Reload High Byte Register (WDTH)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	04H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF2H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTH—WDT Reload High Byte  
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 61. Watchdog Timer Reload Low Byte Register (WDTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF3H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTL—WDT Reload Low  
Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

# Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. The features of UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two STOP bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit baud rate generator (BRG)
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes
- BRG can be configured and used as a basic 16-bit timer
- Driver Enable output for external bus transceivers

## Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 displays the UART architecture.

## Flash Sector Protect Register

The Flash Sector Protect (FPROT) register is shared with the Flash Page Select Register. When the Flash Control Register is written with 73H followed by 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the 8 available Flash memory sectors to be protected. The reset state of each Sector Protect bit is an unprotected state. After a sector is protected by setting its corresponding register bit, it cannot be unprotected (the register bit cannot be cleared) without powering down the device.

**Table 82. Flash Sector Protect Register (FPROT)**

BITS	7	6	5	4	3	2	1	0
FIELD	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1	SPROT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

SPROT7-SPROT0—Sector Protection

Each bit corresponds to a 512 bytes Flash sector. For the Z8F08x3 devices, the upper 3 bits must be zero. For the Z8F04x3 devices all bits are used. For the Z8F02x3 devices, the upper 4 bits are unused. For the Z8F01x3 devices, the upper 6 bits are unused.

## Flash Frequency High and Low Byte Registers

The Flash Frequency High (FFREQH) and Low Byte (FFREQL) registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz) and is calculated using the following equation:

$$\text{FFREQ}[15:0] = \{\text{FFREQH}[7:0], \text{FFREQL}[7:0]\} = \frac{\text{System Clock Frequency}}{1000}$$

**! Caution:** *The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device. Also, Flash programming and erasure is not supported for system clock frequencies below 20 kHz or above 20 MHz.*



The randomized lot identifier is a 32 byte binary value, stored in the flash information page (for more details, see Reading the Flash Information Page on page 143 and Randomized Lot Identifier on page 149) and is unaffected by mass erasure of the device's flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash Information Area.

```
; get value at info address 60 (FE60h)

ldx FPS, #80 ; enable access to flash info page

ld R0, #FE

ld R1, #60

ldc R2, @RR0 ; R2 now contains the calibration value
```

Flash Option Bit Control Register Definitions

Trim Bit Address Register

The Trim Bit Address (TRMADR) register contains the target address for an access to the trim option bits.

Table 85. Trim Bit Address Register (TRMADR)

BITS	7	6	5	4	3	2	1	0
FIELD	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF6H							

- **Note:** *This bit only enables the crystal oscillator. Its selection as system clock must be done manually.*  
*0 = Crystal oscillator is enabled during reset, resulting in longer reset timing*  
*1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing*

- ⚡ **Warning:** *Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin. This is due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.*

## Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 89 through Table 91.

### Trim Bit Address 0000H—Reserved

Table 89. Trim Options Bits at Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 0020H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Reserved—Altering this register may result in incorrect device operation.

### Trim Bit Address 0001H—Reserved

Table 90. Trim Option Bits at 0001H

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 0021H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

## OCD Status Register

The OCD Status register reports status information about the current state of the debugger and the system.

**Table 100. OCD Status Register (OCDSTAT)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	DBG	HALT	FRPENB	Reserved				
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R	R	R	R	R	R	R	R

DBG—Debug Status

0 = NORMAL mode

1 = DEBUG mode

HALT—HALT Mode

0 = Not in HALT mode

1 = In HALT mode

FRPENB—Flash Read Protect Option Bit Enable

0 = FRP bit enabled, that allows disabling of many OCD commands

1 = FRP bit has no effect

Reserved—0 when read

Figure 42 displays the 28-pin Small Shrink Outline Package (SSOP) available for Z8 Encore! XP F0823 Series devices.

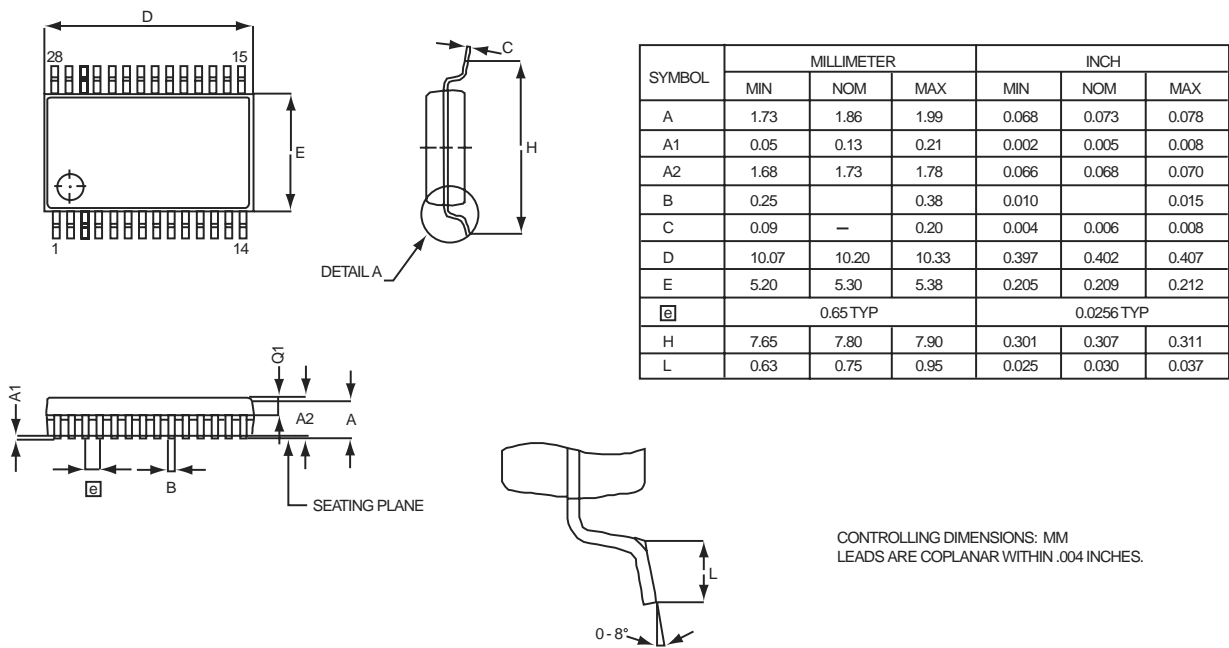


Figure 42. 28-Pin Small Shrink Outline Package (SSOP)

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