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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0823hj005ec">https://www.e-xfl.com/product-detail/zilog/z8f0823hj005ec</a>

# Low-Power Modes

Z8 Encore! XP<sup>®</sup> F0823 Series products contain power-saving features. The highest level of power reduction is provided by the STOP mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in ACTIVE mode (defined as being in neither STOP nor HALT mode).

## STOP Mode

Executing the eZ8 CPU's Stop instruction places the device into STOP mode, powering down all peripherals except the Voltage Brownout detector, and the Watchdog Timer. These two blocks may also be disabled for additional power savings. In STOP mode, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; XIN and XOUT (if previously enabled) are disabled, and PA0/PA1 revert to the states programmed by the GPIO registers.
- System clock is stopped.
- eZ8 CPU is stopped.
- Program counter (PC) stops incrementing.
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control Register.
- If enabled, the Watchdog Timer logic continues to operate.
- If enabled for operation in STOP mode by the associated Flash Option Bit, the Voltage Brownout protection circuit continues to operate.
- All other on-chip peripherals are idle.

To minimize current in STOP mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails ( $V_{CC}$  or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP mode using Stop Mode Recovery. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 21.

**Table 28. Port A–C Input Data Registers (PxIN)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
<b>RESET</b>	X	X	X	X	X	X	X	X
<b>R/W</b>	R	R	R	R	R	R	R	R
<b>ADDR</b>	FD2H, FD6H, FDAH							

PIN[7:0]—Port Input Data

Sampled data from the corresponding port pin input.

0 = Input data is logical 0 (Low)

1 = Input data is logical 1 (High)

## Port A–C Output Data Register

The Port A–C Output Data register (Table 29) controls the output data to the pins.

**Table 29. Port A–C Output Data Register (PxOUT)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>ADDR</b>	FD3H, FD7H, FDBH							

POUT[7:0]—Port Output Data

These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation.

0 = Drive a logical 0 (Low).

1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control register bit to 1.

## LED Drive Enable Register

The LED Drive Enable register (Table 30) activates the controlled current drive. The Port C pin must first be enabled by setting the Alternate Function register to select the LED function.

**Table 30. LED Drive Enable (LEDEN)**

BITS	7	6	5	4	3	2	1	0
FIELD	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F82H							

LEDEN[7:0]—LED Drive Enable

These bits determine which Port C pins are connected to an internal current sink.

0 = Tristate the Port C pin.

1= Connect controlled current sink to the Port C pin.

## LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 31).

These two bits select between four programmable drive levels. Each pin is individually programmable.

**Table 31. LED Drive Level High Register (LEDLVLH)**

BITS	7	6	5	4	3	2	1	0
FIELD	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F83H							

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA

01= 7 mA

10= 13 mA

11= 20 mA

## LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 32).

These two bits select between four programmable drive levels. Each pin is individually programmable.

Table 32. LED Drive Level Low Register (LEDLVLL)

BITS	7	6	5	4	3	2	1	0
FIELD	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F84H							

LEDLVLH[7:0]—LED Level High Bit  
{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.  
00 = 3 mA  
01 = 7 mA  
10 = 13 mA  
11 = 20 mA



## Receiving IrDA Data

Data received from the infrared transceiver using the IR\_RXD signal through the RXD pin is decoded by the Infrared Endec and passed to the UART. The UART's baud rate clock is used by the Infrared Endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 18 displays data reception. When the Infrared Endec is enabled, the UART's RXD signal is internal to the Z8 Encore! XP® F0823 Series products while the IR\_RXD signal is received through the RXD pin.

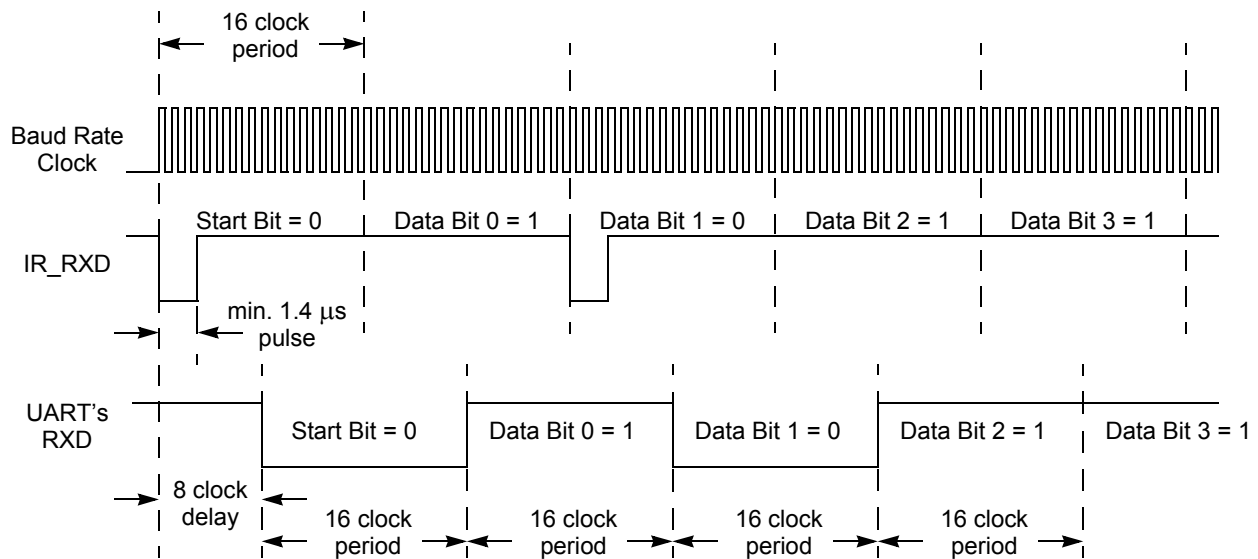


Figure 18. IrDA Data Reception

## Infrared Data Reception

**! Caution:** *The system clock frequency must be at least 1.0 MHz to ensure proper reception of the 1.4 μs minimum width pulses allowed by the IrDA standard.*

## Endec Receiver Synchronization

The IrDA receiver uses a local baud rate clock counter (0 to 15 clock periods) to generate an input stream for the UART and to create a sampling window for detection of incoming pulses. The generated UART input (UART RXD) is delayed by 8 baud rate clock periods with respect to the incoming IrDA data stream. When a falling edge in the input data stream is detected, the Endec counter is reset. When the count reaches a value of 8, the UART RXD value is updated to reflect the value of the decoded data. When the count reaches 12 baud clock periods, the sampling window for the next incoming pulse opens. The window remains open until the count again reaches 8 (that is, 24 baud clock periods since the previous pulse was detected), giving the Endec a sampling window of minus four

bits of resolution are lost because of a rounding error. As a result, the final value is an 11-bit number.

## **Automatic Powerdown**

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered down. From this powerdown state, the ADC requires 40 system clock cycles to powerup. The ADC powers up when a conversion is requested by the ADC Control register.

## **Single-Shot Conversion**

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. Follow the steps below for setting up the ADC and initiating a single-shot conversion:

1. Enable the acceptable analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
2. Write the ADC Control/Status Register 1 to configure the ADC
  - Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
3. Write to the ADC Control Register 0 to configure the ADC and begin the conversion. The bit fields in the ADC Control register can be written simultaneously:
  - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
  - Clear CONT to 0 to select a single-shot conversion.
  - If the internal voltage reference must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
  - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in the ADC Control Register 0.
  - Set CEN to 1 to start the conversion.
4. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power-up before beginning the 5129 cycle conversion.



REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL};

► **Note:** *This reference is independent of the Comparator reference.*

00= Internal Reference Disabled, reference comes from external pin.

01= Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

REFEXT—External Reference Select

0 = External reference buffer is disabled;  $V_{ref}$  pin is available for GPIO functions

1 = The internal ADC reference is buffered and connected to the  $V_{ref}$  pin

CONT

0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles.

1 = Continuous conversion. ADC data updated every 256 system clock cycles.

ANAIN[3:0]—Analog Input Select

These bits select the analog input for conversion. Not all port pins in this list are available in all packages for Z8 Encore! XP<sup>®</sup> F0823 Series. For information on the port pins available with each package style, see Pin Description on page 7. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

Single-Ended:

0000 = ANA0

0001 = ANA1

0010 = ANA2

0011 = ANA3

0100 = ANA4

0101 = ANA5

0110 = ANA6

0111 = ANA7

1000 = Reserved

1001 = Reserved

1010 = Reserved

1011 = Reserved

1100 = Reserved

1101 = Reserved

1110 = Reserved

1111 = Reserved

## ADC Data Low Bits Register

The ADC Data Low Byte register contains the lower bits of the ADC output as well as an overflow status bit. The output is a 11-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data Low Byte register is read-only. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

**Table 75. ADC Data Low Bits Register (ADCD\_L)**

BITS	7	6	5	4	3	2	1	0
FIELD	ADCDL			Reserved				OVF
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F73H							

ADCDL—ADC Data Low Bits

These bits are the least significant three bits of the 11-bits of the ADC output. These bits are undefined after a Reset.

Reserved—Undefined when read

OVF—Overflow Status

0= An overflow did not occur in the digital filter for the current sample

1= An overflow did occur in the digital filter for the current sample

## Flash Sector Protect Register

The Flash Sector Protect (FPROT) register is shared with the Flash Page Select Register. When the Flash Control Register is written with 73H followed by 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the 8 available Flash memory sectors to be protected. The reset state of each Sector Protect bit is an unprotected state. After a sector is protected by setting its corresponding register bit, it cannot be unprotected (the register bit cannot be cleared) without powering down the device.

**Table 82. Flash Sector Protect Register (FPROT)**

BITS	7	6	5	4	3	2	1	0
FIELD	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1	SPROT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

SPROT7-SPROT0—Sector Protection

Each bit corresponds to a 512 bytes Flash sector. For the Z8F08x3 devices, the upper 3 bits must be zero. For the Z8F04x3 devices all bits are used. For the Z8F02x3 devices, the upper 4 bits are unused. For the Z8F01x3 devices, the upper 6 bits are unused.

## Flash Frequency High and Low Byte Registers

The Flash Frequency High (FFREQH) and Low Byte (FFREQL) registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz) and is calculated using the following equation:

$$\text{FFREQ}[15:0] = \{\text{FFREQH}[7:0], \text{FFREQL}[7:0]\} = \frac{\text{System Clock Frequency}}{1000}$$

**! Caution:** *The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device. Also, Flash programming and erasure is not supported for system clock frequencies below 20 kHz or above 20 MHz.*

## OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

1. Hold PA2/ $\overline{\text{RESET}}$  Low.
2. Wait 5 ms for the internal reset sequence to complete.
3. Send the following bytes serially to the debug pin:  
DBG  $\leftarrow$  80H (autobaud)  
DBG  $\leftarrow$  EBH  
DBG  $\leftarrow$  5AH  
DBG  $\leftarrow$  70H  
DBG  $\leftarrow$  CDH (32-bit unlock key)
4. Release PA2/ $\overline{\text{RESET}}$ . The PA0/DBG pin is now identical in function to that of the DBG pin on the 20- or 28-pin device. To enter DEBUG mode, re-autobaud and write 80H to the OCD control register (see On-Chip Debugger Commands on page 157).

## Breakpoints

Execution breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the OCD. If breakpoints are enabled, the OCD enters DEBUG mode and idles the eZ8 CPU. If breakpoints are not enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

### Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

## Runtime Counter

The OCD contains a 16-bit Runtime Counter. It counts system clock cycles between breakpoints. The counter starts counting when the OCD leaves DEBUG mode and stops counting when it enters DEBUG mode again or when it reaches the maximum count of FFFFH.

## Assembly Language Syntax

For proper instruction execution, eZ8 CPU assembly language syntax requires that the operands be written as ‘destination, source’. After assembly, the object code usually has the operands in the order ‘source, destination’, but ordering is opcode-dependent. The following instruction examples illustrate the format of some basic assembly instructions and the resulting object code produced by the assembler. You must follow this binary format if you prefer manual program coding or intend to implement your own assembler.

### Example 1

If the contents of Registers 43H and 08H are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 103. Assembly Language Syntax Example 1

Assembly Language Code	ADD	43H,	08H	(ADD dst, src)
Object Code	04	08	43	(OPC src, dst)

### Example 2

In general, when an instruction format requires an 8-bit register address, that address can specify any register location in the range 0–255 or, using Escaped Mode Addressing, a Working Register R0–R15. If the contents of Register 43H and Working Register R8 are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 104. Assembly Language Syntax Example 2

Assembly Language Code	ADD	43H,	R8	(ADD dst, src)
Object Code	04	E8	43	(OPC src, dst)

See the device-specific Product Specification to determine the exact register file range available. The register file size varies, depending on the device type.

## eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags, and address modes are represented by a notational shorthand that is described in Table 105.

- Rotate and Shift

Tables 107 through Table 114 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction can be considered as a subset of more than one category. Within these tables, the source operand is identified as ‘src’, the destination operand is ‘dst’ and a condition code is ‘cc’.

**Table 107. Arithmetic Instructions**

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using Extended Addressing
ADD	dst, src	Add
ADDX	dst, src	Add using Extended Addressing
CP	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using Extended Addressing
CPX	dst, src	Compare using Extended Addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment
INCW	dst	Increment Word
MULT	dst	Multiply
SBC	dst, src	Subtract with Carry
SBCX	dst, src	Subtract with Carry using Extended Addressing
SUB	dst, src	Subtract
SUBX	dst, src	Subtract using Extended Addressing

Table 115. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LDC dst, src	$dst \leftarrow src$	r	lrr	C2	–	–	–	–	–	–	2	5
		lr	lrr	C5							2	9
		lrr	r	D2							2	5
LDCI dst, src	$dst \leftarrow src$ $r \leftarrow r + 1$ $rr \leftarrow rr + 1$	lr	lrr	C3	–	–	–	–	–	–	2	9
		lrr	lr	D3							2	9
LDE dst, src	$dst \leftarrow src$	r	lrr	82	–	–	–	–	–	–	2	5
		lrr	r	92							2	5
LDEI dst, src	$dst \leftarrow src$ $r \leftarrow r + 1$ $rr \leftarrow rr + 1$	lr	lrr	83	–	–	–	–	–	–	2	9
		lrr	lr	93							2	9
LDWX dst, src	$dst \leftarrow src$	ER	ER	1FE8	–	–	–	–	–	–	5	4
LDX dst, src	$dst \leftarrow src$	r	ER	84	–	–	–	–	–	–	3	2
		lr	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	lr	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$dst \leftarrow src + X$	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	$dst[15:0] \leftarrow dst[15:8] * dst[7:0]$	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
Flags Notation:	* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1							

**Table 119. Power Consumption (Continued)**

Symbol	Parameter	V <sub>DD</sub> = 2.7 V to 3.6 V			Units	Conditions
		Typical <sup>1</sup>	Maximum <sup>2</sup> Std Temp	Maximum <sup>3</sup> Ext Temp		
I <sub>DD</sub> BG	Band Gap Supply Current	320	480	500	μA	For 20-/28-pin devices
						For 8-pin devices

**Notes**

1. Typical conditions are defined as V<sub>DD</sub> = 3.3 V and +30 °C.
2. Standard temperature is defined as T<sub>A</sub> = 0 °C to +70 °C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as T<sub>A</sub> = -40 °C to +105 °C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

## AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50 pF on all outputs.

**Table 120. AC Characteristics**

Symbol	Parameter	V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = -40 °C to +105 °C (unless otherwise stated)		Units	Conditions
		Minimum	Maximum		
F <sub>SYSCLK</sub>	System Clock Frequency	–	20.0 <sup>1</sup>	MHz	Read-only from Flash memory
		0.032768	20.0 <sup>1</sup>	MHz	Program or erasure of the Flash memory
T <sub>XIN</sub>	System Clock Period	50	–	ns	T <sub>CLK</sub> = 1/F <sub>sysclk</sub>
T <sub>XINH</sub>	System Clock High Time	20	30	ns	T <sub>CLK</sub> = 50 ns
T <sub>XINL</sub>	System Clock Low Time	20	30	ns	T <sub>CLK</sub> = 50 ns
T <sub>XINR</sub>	System Clock Rise Time	–	3	ns	T <sub>CLK</sub> = 50 ns
T <sub>XINF</sub>	System Clock Fall Time	–	3	ns	T <sub>CLK</sub> = 50 ns

<sup>1</sup>System Clock Frequency is limited by the Internal Precision Oscillator on the Z8 Encore! XP<sup>®</sup> F0823 Series. See Table 121 on page 198.



**Table 123. Flash Memory Electrical Characteristics and Timing**

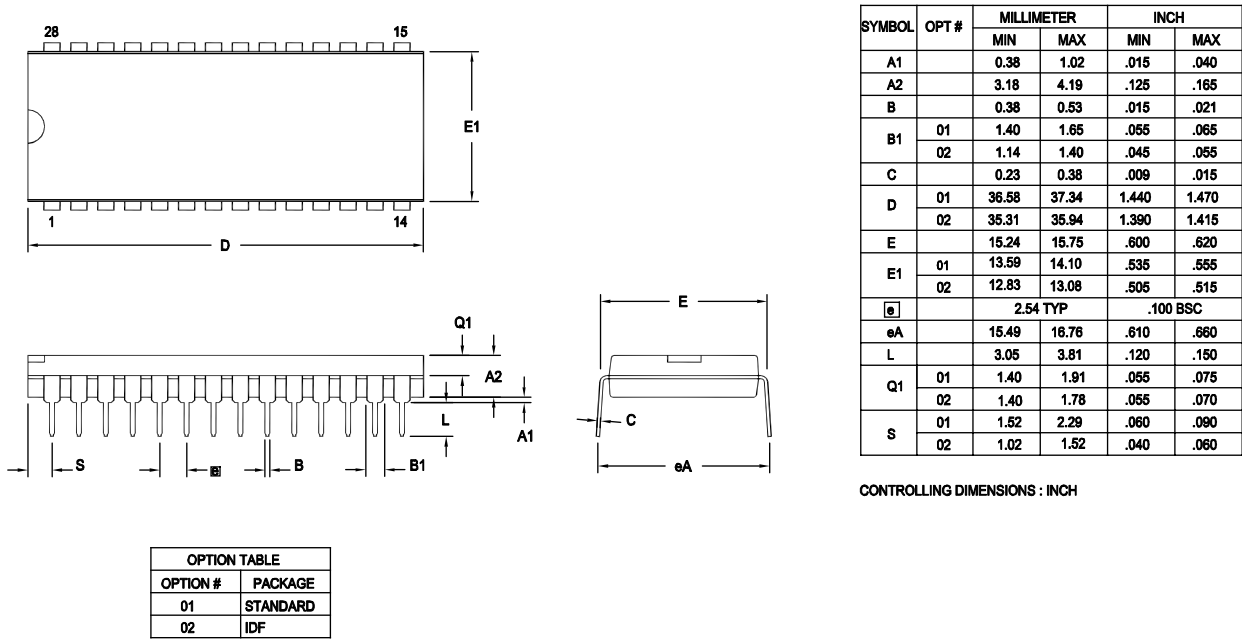
Parameter	$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$ (unless otherwise stated)			Units	Notes
	Minimum	Typical	Maximum		
Flash Byte Read Time	100	–	–	ns	
Flash Byte Program Time	20	–	40	$\mu\text{s}$	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25 $^{\circ}\text{C}$
Endurance	10,000	–	–	cycles	Program/erase cycles

**Table 124. Watchdog Timer Electrical Characteristics and Timing**

Symbol	Parameter	$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$ (unless otherwise stated)			Units	Conditions
		Minimum	Typical	Maximum		
$F_{WDT}$	WDT Oscillator Frequency		10		kHz	
$F_{WDT}$	WDT Oscillator Error			$\pm 50$	%	
$T_{WDT\text{CAL}}$	WDT Calibrated Timeout	0.98	1	1.02	s	$V_{DD} = 3.3 \text{ V};$ $T_A = 30 \text{ }^{\circ}\text{C}$
		0.70	1	1.30	s	$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = 0 \text{ }^{\circ}\text{C to } 70 \text{ }^{\circ}\text{C}$
		0.50	1	1.50	s	$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$



Figure 40 displays the 28-pin Plastic Dual Inline Package (PDIP) available for Z8 Encore! XP F0823 Series devices.



Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 40. 28-Pin Plastic Dual Inline Package (PDIP)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
<b>Z8 Encore! XP with 4 KB Flash, 10-Bit Analog-to-Digital Converter</b>								
<b>Standard Temperature: 0 °C to 70 °C</b>								
Z8F0423PB005SC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005SC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005SC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005SC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005SC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005SC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005SC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005SC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005SC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>								
Z8F0423PB005EC	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005EC	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005EC	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005EC	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005EC	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005EC	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005EC	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005EC	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005EC	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
<b>Z8 Encore! XP with 1 KB Flash</b>								
<b>Standard Temperature: 0 °C to 70 °C</b>								
Z8F0113PB005SC	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005SC	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005SC	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005SC	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005SC	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005SC	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005SC	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005SC	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005SC	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>								
Z8F0113PB005EC	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005EC	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005EC	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005EC	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005EC	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005EC	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005EC	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005EC	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005EC	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								