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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0823hj005sc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 3.	Signal	Descriptions	(Continued)	
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Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	I	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD.
		Caution: The DBG pin is open-drain and requires an external pull- up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V _{DD}	Ι	Digital Power Supply.
AV _{DD}	I	Analog Power Supply.
V _{SS}	I	Digital Ground.
AV _{SS}	Ι	Analog Ground.
Note: The AV _{DD} and A PB7 on 28-pin pa	.V _{SS} sigr ackages	nals are available only in 28-pin packages with ADC. They are replaced by PB6 and without ADC.

Pin Characteristics

Table 4 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 20- and 28-pin devices. Data in Table 4 is sorted alphabetically by the pin symbol mnemonic.

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! $XP^{\text{(R)}}$ F0823 Series 8-pin devices.

Note: All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 4 below describes 5 V-tolerance for the 20- and 28-pin packages only.

Symbol		Reset	Active Low or Active	Tristate	Internal Pull-un	Schmitt-	Open Drain	5 V
Mnemonic	Direction	Direction	High	Output	or Pull-down	Input	Output	Tolerance
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PB[7:6] only
PC[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PC[7:3] only
RESET	I/O	I/O (d <u>efaults</u> to RESET)	Low (in Reset mode)	Yes (PD0 only)	Always on for RESET	Yes	Always on for RESET	Yes
VDD	N/A	N/A	N/A	N/A			N/A	N/A
VSS	N/A	N/A	N/A	N/A			N/A	N/A

Table 4. Pin Characteristics (20- and 28-pin Devices)

Note: *PB6 and PB7 are available only in the devices without ADC.*

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP/LED Drive	ADC or Comparator Input, or LED drive	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN/ LED Drive	ADC or Comparator Input, or LED drive	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/LED/ VREF*	ADC Analog Input or LED Drive or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		LED	LED drive	AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
	_	LED	LED Drive	AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
	_	LED	LED Drive	AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
	_	LED	LED Drive	AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
		LED	LED Drive	AFS1[7]: 1

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Note: Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, Alternate Function selection as described in Port A–C Alternate Function Sub-Registers must also be enabled. *VREF is available on PC2 in 20-pin parts only. Caution:

To avoid missing interrupts, use the following coding style to clear bits in the Interrupt Request 0 register:

Good coding style that avoids lost interrupt requests: ANDX IRQ0, MASK

Software Interrupt Assertion

Program code generates interrupts directly. Writing a 1 to the correct bit in the Interrupt Request register triggers an interrupt (assuming that interrupt is enabled). When the interrupt request is acknowledged by the eZ8 CPU, the bit in the Interrupt Request register is automatically cleared to 0.

Caution: The following coding style used to generate software interrupts by setting bits in the Interrupt Request registers is not recommended. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost.

Poor coding style that can result in lost interrupt requests: LDX r0, IRQ0 OR r0, MASK LDX IRQ0, r0

Caution: To avoid missing interrupts, use the following coding style to set bits in the Interrupt Request registers:

Good coding style that avoids lost interrupt requests: ORX IRQ0, MASK

Watchdog Timer Interrupt Assertion

The Watchdog Timer interrupt behavior is different from interrupts generated by other sources. The Watchdog Timer continues to assert an interrupt as long as the timeout condition continues. As it operates on a different (and usually slower) clock domain than the rest of the device, the Watchdog Timer continues to assert this interrupt for many system clocks until the counter rolls over.

Caution: To avoid re-triggerings of the Watchdog Timer interrupt after exiting the associated interrupt service routine, it is recommended that the service routine continues to read from the RSTSTAT register until the WDT bit is cleared as given in the following coding sample:

> CLEARWDT: LDX r0, RSTSTAT ; read reset status register to clear wdt bit BTJNZ 5, r0, CLEARWDT ; loop until bit is cleared

Interrupt Control Register Definitions

For all interrupts other than the Watchdog Timer interrupt, the Primary Oscillator Fail Trap, and the Watchdog Timer Oscillator Fail Trap, the interrupt control registers enable individual interrupts, set interrupt priorities, and indicate interrupt requests.

Interrupt Request 0 Register

The Interrupt Request 0 (IRQ0) register (Table 34) stores the interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ0 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 0 register to determine if any interrupt requests are pending.

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1I	ТОІ	U0RXI	U0TXI	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	0H			

Table 34. Interrupt Request 0 Register (IRQ0)

Reserved—Must be 0

T1I—Timer 1 Interrupt Request

- 0 = No interrupt request is pending for Timer 1
- 1 = An interrupt request from Timer 1 is awaiting service

T0I—Timer 0 Interrupt Request

- 0 = No interrupt request is pending for Timer 0
- 1 = An interrupt request from Timer 0 is awaiting service

U0RXI-UART 0 Receiver Interrupt Request

- 0 = No interrupt request is pending for the UART 0 receiver
- 1 = An interrupt request from the UART 0 receiver is awaiting service

U0TXI-UART 0 Transmitter Interrupt Request

- 0 = No interrupt request is pending for the UART 0 transmitter
- 1 = An interrupt request from the UART 0 transmitter is awaiting service

ADCI—ADC Interrupt Request

- 0 = No interrupt request is pending for the ADC
- 1 = An interrupt request from the ADC is awaiting service

Timer Control Register Definitions

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 49 and Table 50) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from the TxL reads the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0	
FIELD		TH							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W							
ADDR		F00H, F08H							

Table 49. Timer 0–1 High Byte Register (TxH)

Table 50. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0	
FIELD		TL							
RESET	0	0	0	0	0	0	0	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR				F01H,	F09H				

TH and TL—Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 51 and Table 52) store a 16-bit Reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte register occurs, the temporary holding register value is written to the Timer High Byte register. This operation allows simultaneous updates of the 16-bit Timer Reload value.

- 0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events
- 10 = Timer Interrupt only on defined Input Capture/Deassertion Events
- 11 = Timer Interrupt only on defined Reload/Compare Events

Reserved-Must be 0

PWMD—PWM Delay value

This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state.

000 = No delay 001 = 2 cycles delay 010 = 4 cycles delay 011 = 8 cycles delay 100 = 16 cycles delay 101 = 32 cycles delay 110 = 64 cycles delay111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event

1 = Previous timer interrupt is a result of Timer Input Capture Event

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	TPOL	PRES TMODE					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR		F07H, F0FH						

Table 56. Timer 0–1 Control Register 1 (TxCTL1)

TEN—Timer Enable

0 = Timer is disabled

1 = Timer enabled to count

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer

ONE-SHOT Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER Mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

- 0 =Count occurs on the rising edge of the Timer Input signal
- 1 = Count occurs on the falling edge of the Timer Input signal

PWM SINGLE OUTPUT Mode

0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload.

1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload.

CAPTURE Mode

0 = Count is captured on the rising edge of the Timer Input signal

1 = Count is captured on the falling edge of the Timer Input signal

COMPARE Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

GATED Mode

0 = Timer counts when the Timer Input signal is High (1) and interrupts are generated on the falling edge of the Timer Input.

1 = Timer counts when the Timer Input signal is Low (0) and interrupts are generated on the rising edge of the Timer Input.

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! XP[®] F0823 Series operation. The feature configuration data is stored in the Flash program memory and loaded into holding registers during Reset. The features available for control through the Flash Option Bits include:

- Watchdog Timer time-out response selection-interrupt or system reset
- Watchdog Timer always on (enabled at Reset)
- The ability to prevent unwanted read access to user code in Program Memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in Program Memory
- Voltage Brownout configuration-always enabled or disabled during STOP mode to reduce STOP mode power consumption
- Factory trimming information for the internal precision oscillator
- Factory calibration values for ADC
- Factory serialization and randomized lot identifier (optional)

Operation

Option Bit Configuration By Reset

Each time the Flash Option Bits are programmed or erased, the device must be Reset for the change to take effect. During any reset operation (System Reset, Power-On Reset, or Stop Mode Recovery), the Flash Option Bits are automatically read from the Flash Program Memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP F0823 Series. Option Bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

Option Bit Types

User Option Bits

The user option bits are contained in the first two bytes of program memory. Access to these bits has been provided because these locations contain application-specific device

The randomized lot identifier is a 32 byte binary value, stored in the flash information page (for more details, see Reading the Flash Information Page on page 143 and Randomized Lot Identifier on page 149) and is unaffected by mass erasure of the device's flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash Information Area.

; get value at info address 60 (FE60h)
ldx FPS, #%80 ; enable access to flash info page
ld R0, #%FE
ld R1, #%60
ldc R2, @RR0 ; R2 now contains the calibration value

Flash Option Bit Control Register Definitions

Trim Bit Address Register

The Trim Bit Address (TRMADR) register contains the target address for an access to the trim option bits.

Table 85. Trim Bit Address Register (TRMADR)

BITS	7	6	5	4	3	2	1	0
FIELD	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FF	6H			

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INTEN—Internal Precision Oscillator Enable

1 = Internal precision oscillator is enabled

0 = Internal precision oscillator is disabled

Reserved—R/W bits must be 0 during writes; 0 when read

WDTEN—Watchdog Timer Oscillator Enable

1 = Watchdog Timer oscillator is enabled

0 = Watchdog Timer oscillator is disabled

POFEN—Primary Oscillator Failure Detection Enable

1 = Failure detection and recovery of primary oscillator is enabled

0 = Failure detection and recovery of primary oscillator is disabled

WDFEN—Watchdog Timer Oscillator Failure Detection Enable

1 = Failure detection of Watchdog Timer oscillator is enabled

0 = Failure detection of Watchdog Timer oscillator is disabled

SCKSEL—System Clock Oscillator Select

000 = Internal precision oscillator functions as system clock at 5.53 MHz

001 = Internal precision oscillator functions as system clock at 32 kHz

010 = Reserved

011 = Watchdog Timer oscillator functions as system clock

100 = External clock signal on PB3 functions as system clock

101 = Reserved

110 = Reserved

111 = Reserved

Z8 Encore! XP[®] F0823 Series Product Specification

Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
сс	Condition code	р	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
lr	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 116. Opcode Map Abbreviations

Electrical Characteristics

The data in this chapter is pre-qualification and pre-characterization and is subject to change. Additional electrical characteristics may be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed in Table 117 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		220	mW	
Maximum current into V_{DD} or out of V_{SS}		60	mA	
20-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		430	mW	
Maximum current into V _{DD} or out of V _{SS}		120	mA	
28-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		450	mW	

Table 117. Absolute Maximum Ratings

On-Chip Debugger Timing

Figure 31 and Table 129 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 ns maximum rise and fall time.



		Delay (ns)		
Parameter	Abbreviation	Minimum	Maximum	
DBG				
T ₁	XIN Rise to DBG Valid Delay	_	15	
T ₂	XIN Rise to DBG Output Hold Time	2	_	
T ₃	DBG to XIN Rise Input Setup Time	5	-	
T ₄	DBG to XIN Rise Input Hold Time	5	-	

Table 129. On-Chip Debugger Timing

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP with 2 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0 °C to 70 °C								
Z8F0223PB005SC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005SC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005SC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005SC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005SC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005SC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005SC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005SC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005SC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C								
Z8F0223PB005EC	2 KB	512 B	6	12	2	4	1	PDIP 8-pin package
Z8F0223QB005EC	2 KB	512 B	6	12	2	4	1	QFN 8-pin package
Z8F0223SB005EC	2 KB	512 B	6	12	2	4	1	SOIC 8-pin package
Z8F0223SH005EC	2 KB	512 B	16	18	2	7	1	SOIC 20-pin package
Z8F0223HH005EC	2 KB	512 B	16	18	2	7	1	SSOP 20-pin package
Z8F0223PH005EC	2 KB	512 B	16	18	2	7	1	PDIP 20-pin package
Z8F0223SJ005EC	2 KB	512 B	22	18	2	8	1	SOIC 28-pin package
Z8F0223HJ005EC	2 KB	512 B	22	18	2	8	1	SSOP 28-pin package
Z8F0223PJ005EC	2 KB	512 B	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

er					ers	Channels	IrDA	c
Part Numb	Flash	RAM	I/O Lines	Interrupts	16-Bit Tim w/PWM	10-Bit A/D	UART with	Descriptio
Z8 Encore! XP with 2 KB Flash								
Standard Temperature	e: 0 °C to	70 °C						
Z8F0213PB005SC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005SC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005SC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005SC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005SC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005SC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005SC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005SC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005SC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C								
Z8F0213PB005EC	2 KB	512 B	6	12	2	0	1	PDIP 8-pin package
Z8F0213QB005EC	2 KB	512 B	6	12	2	0	1	QFN 8-pin package
Z8F0213SB005EC	2 KB	512 B	6	12	2	0	1	SOIC 8-pin package
Z8F0213SH005EC	2 KB	512 B	16	18	2	0	1	SOIC 20-pin package
Z8F0213HH005EC	2 KB	512 B	16	18	2	0	1	SSOP 20-pin package
Z8F0213PH005EC	2 KB	512 B	16	18	2	0	1	PDIP 20-pin package
Z8F0213SJ005EC	2 KB	512 B	24	18	2	0	1	SOIC 28-pin package
Z8F0213HJ005EC	2 KB	512 B	24	18	2	0	1	SSOP 28-pin package
Z8F0213PJ005EC	2 KB	512 B	24	18	2	0	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging								

TM 176

HALT 176 INC 175 INCW 175 IRET 178 JP 178 LD 177 LDC 177 LDCI 176, 177 LDE 177 LDEI 176 LDX 177 LEA 177 load 177 logical 177 **MULT 175** NOP 176 OR 177 ORX 178 POP 177 POPX 177 program control 178 **PUSH 177** PUSHX 177 **RCF 176 RET 178** RL 178 **RLC 178** rotate and shift 178 RR 178 **RRC 178** SBC 175 SCF 176, 177 SRA 179 SRL 179 **SRP 177 STOP 177** SUB 175 **SUBX 175 SWAP 179 TCM 176 TCMX 176**

DJNZ 178

EI 176

Z8 Encore! XP[®] F0823 Series Product Specification

TMX 176 **TRAP 178** Watchdog Timer refresh 177 XOR 178 **XORX 178** instructions, eZ8 classes of 174 interrupt control register 64 interrupt controller 53 architecture 53 interrupt assertion types 56 interrupt vectors and priority 56 operation 55 register definitions 58 software interrupt assertion 57 interrupt edge select register 63 interrupt request 0 register 58 interrupt request 1 register 59 interrupt request 2 register 59 interrupt return 178 interrupt vector listing 53 interrupts **UART 101** IR 173 lr 173 **IrDA** architecture 113 block diagram 113 control register definitions 116 operation 113 receiving data 115 transmitting data 114 **IRET 178** IRQ0 enable high and low bit registers 60 IRQ1 enable high and low bit registers 61 IRQ2 enable high and low bit registers 62 **IRR 173** Irr 173

J

JP 178 jump, conditional, relative, and relative conditional 178

Т

TCM 176 TCMX 176 test complement under mask 176 test complement under mask - extended addressing 176 test under mask 176 test under mask - extended addressing 176 timer signals 9 timers 67 architecture 67 block diagram 67 CAPTURE mode 74, 75, 84, 85 CAPTURE/COMPARE mode 78, 85 COMPARE mode 76, 84 CONTINUOUS mode 69, 84 COUNTER mode 70, 71 COUNTER modes 84 GATED mode 77, 84 ONE-SHOT mode 68, 84 operating mode 68 PWM mode 72, 73, 84, 85 reading the timer count values 79 reload high and low byte registers 80 timer control register definitions 80 timer output signal operation 79 timers 0-3 control registers 82, 83 high and low byte registers 80, 81 TM 176 TMX 176 tools, hardware and software 226 transmit IrDA data 114 transmitting UART data-polled method 95 transmitting UART dat-interrupt-driven method 96 **TRAP 178**

U

UART 4 architecture 93 baud rate generator 103

control register definitions 104 controller signals 9 data format 94 interrupts 101 MULTIPROCESSOR mode 99 receiving data using interrupt-driven method 98 receiving data using the polled method 97 transmitting data using the interrupt-driven method 96 transmitting data using the polled method 95 x baud rate high and low registers 110 x control 0 and control 1 registers 107 x status 0 and status 1 registers 105, 106 **UxBRH** register 110 UxBRL register 110 UxCTL0 register 107, 110 UxCTL1 register 108 UxRXD register 105 UxSTAT0 register 105 UxSTAT1 register 106 UxTXD register 104

V

vector 173 Voltage Brownout reset (VBR) 24

W

Watchdog Timer approximate time-out delay 87 CNTL 24 control register 89, 127, 167 electrical characteristics and timing 200, 202 interrupt in normal operation 88 interrupt in STOP mode 88 refresh 88, 177 reload unlock sequence 89 reload upper, high and low registers 90 reset 25 reset in normal operation 89