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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0823pj005sc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Overview

Zilog's Z8 Encore! XP[®] microcontroller unit (MCU) family of products are the first Zilog[®] microcontroller products based on the 8-bit eZ8 CPU core. Z8 Encore! XP F0823 Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8[®] instructions. The rich peripheral set of Z8 Encore! XP F0823 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The key features of Z8 Encore! XP F0823 Series include:

- 5 MHz eZ8 CPU
- 1 KB, 2 KB, 4 KB, or 8 KB Flash memory with in-circuit programming capability
- 256 B, 512 B, or 1 KB register RAM
- 6 to 24 I/O pins depending upon package
- Internal precision oscillator (IPO)
- Full-duplex UART
- The universal asynchronous receiver/transmitter (UART) baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared data association (IrDA)-compliant infrared encoder/decoders, integrated with UART
- Two enhanced 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- On-Chip Debugger (OCD)
- Optional 8-channel, 10-bit Analog-to-Digital Converter (ADC)
- On-Chip analog comparator
- Up to 20 vectored interrupts
- Direct LED drive with programmable drive strengths
- Voltage Brownout (VBO) protection
- Power-On Reset (POR)

Program Memory Address (Hex)	Function
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–003D	Oscillator Fail Traps*
003E-03FF	Program Memory
*See Table 33 on page 54 for a list of the int	terrupt vectors and traps.

Table 6. Z8 Encore! XP F0823 Series Program Memory Maps (Continued)

Data Memory

Z8 Encore! XP[®] F0823 Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 7 lists the Z8 Encore! XP F0823 Series Flash Information Area. This 128 B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

Program Memory Address	
(Hex)	Function
FE00–FE3F	Zilog Option Bits.
FE40–FE53	Part Number. 20-character ASCII alphanumeric code Left justified and filled with FH.
FE54–FE5F	Reserved.
FE60–FE7F	Zilog Calibration Data.
FE80–FFFF	Reserved.

Table 7. Z8 Encore! XP F0823 Series Flash Memory Information Area Map

HALT Mode

Executing the eZ8 CPU's HALT instruction places the device into HALT mode, which powers down the CPU but leaves all other peripherals active. In HALT mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate.
- System clock is enabled and continues to operate.
- eZ8 CPU is stopped.
- Program counter stops incrementing.
- Watchdog Timer's internal RC oscillator continues to operate.
- If enabled, the Watchdog Timer continues to operate.
- All other on-chip peripherals continue to operate.

The eZ8 CPU can be brought out of HALT mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brownout reset
- External **RESET** pin assertion

To minimize current in HALT mode, all GPIO pins that are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

Peripheral-Level Power Control

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! XP F0823 Series devices. Disabling a given peripheral minimizes its power consumption.

Power Control Register Definitions

The following sections describe the power control registers.

Power Control Register 0

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block.

Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.



Figure 7. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins are used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The port A–D Alternate Function sub-registers configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. Table 15 on page 39 lists the alternate functions possible with each port pin. The alternate function associated at a pin is defined through Alternate Function Sets sub-registers AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

Table 19. Port A–C Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0	
FIELD		PCTL							
RESET		00H							
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W							
ADDR				FD1H, FD	5H, FD9H				

PCTL[7:0]—Port Control

The Port Control register provides access to all sub-registers that configure the GPIO Port operation.

Port A-C Data Direction Sub-Registers

The Port A–C Data Direction sub-register is accessed through the Port A–C Control register by writing 01H to the Port A–C Address register (Table 20).

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 01H i	n Port A–C	Address Reg	gister, acces	sible throug	n the Port A-	-C Control F	Register

Table 20. Port A–C Data Direction Sub-Registers (PxDD)

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–C Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–C Input Data Register. The output driver is tristated.

Port A–C Alternate Function Sub-Registers

The Port A–C Alternate Function sub-register (Table 21) is accessed through the Port A–C Control register by writing 02H to the Port A–C Address register. The Port A–C Alternate Function sub-registers enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the Port A–C Alternate Function Set 1 Sub-Registers on page 48 and Port A–C Alternate Function Set 2 Sub-Registers on

	Program Memory	
Priority	Vector Address	Interrupt or Trap Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see Watchdog Timer on page 87)
	003AH	Primary Oscillator Fail Trap (not an interrupt)
	003CH	Watchdog Timer Oscillator Fail Trap (not an interrupt)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	Reserved
	0014H	Reserved
	0016H	ADC
	0018H	Port A Pin 7, selectable rising or falling input edge
	001AH	Port A Pin 6, selectable rising or falling input edge or Comparator Output
	001CH	Port A Pin 5, selectable rising or falling input edge
	001EH	Port A Pin 4, selectable rising or falling input edge
	0020H	Port A Pin 3 or Port D Pin 3, selectable rising or falling input edge
	0022H	Port A Pin 2 or Port D Pin 2, selectable rising or falling input edge
	0024H	Port A Pin 1, selectable rising or falling input edge
	0026H	Port A Pin 0, selectable rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C Pin 3, both input edges
	0032H	Port C Pin 2, both input edges
	0034H	Port C Pin 1, both input edges

Table 33. Trap and Interrupt Vectors in Order of Priority

Interrupt Control Register Definitions

For all interrupts other than the Watchdog Timer interrupt, the Primary Oscillator Fail Trap, and the Watchdog Timer Oscillator Fail Trap, the interrupt control registers enable individual interrupts, set interrupt priorities, and indicate interrupt requests.

Interrupt Request 0 Register

The Interrupt Request 0 (IRQ0) register (Table 34) stores the interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ0 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 0 register to determine if any interrupt requests are pending.

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1I	ТОІ	U0RXI	U0TXI	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	0H			

Table 34. Interrupt Request 0 Register (IRQ0)

Reserved—Must be 0

T1I—Timer 1 Interrupt Request

- 0 = No interrupt request is pending for Timer 1
- 1 = An interrupt request from Timer 1 is awaiting service

T0I—Timer 0 Interrupt Request

- 0 = No interrupt request is pending for Timer 0
- 1 = An interrupt request from Timer 0 is awaiting service

U0RXI-UART 0 Receiver Interrupt Request

- 0 = No interrupt request is pending for the UART 0 receiver
- 1 = An interrupt request from the UART 0 receiver is awaiting service

U0TXI-UART 0 Transmitter Interrupt Request

- 0 = No interrupt request is pending for the UART 0 transmitter
- 1 = An interrupt request from the UART 0 transmitter is awaiting service

ADCI—ADC Interrupt Request

- 0 = No interrupt request is pending for the ADC
- 1 = An interrupt request from the ADC is awaiting service

Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Follow the steps below to configure the UART receiver for interrupt-driven operation:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
- 5. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
- 6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
 - Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR mode
 - Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme
 - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! XP devices without a DMA block)
- 7. Write the device address to the Address Compare Register (automatic MULTIPROCESSOR modes only).
- 8. Write to the UART Control 0 register to:
 - Set the receive enable bit (REN) to enable the UART for data reception
 - Enable parity, if appropriate and if multiprocessor mode is not enabled, and select either even or odd parity
- 9. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

- 1. Checks the UART Status 0 register to determine the source of the interrupt error, break, or received data.
- 2. Reads the data from the UART Receive Data register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) mode, further actions may be required depending on the MULTIPROCESSOR mode bits MPMD[1:0].

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No

If the Baud Rate Generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

Receiver Ready

Receiver Interrupt

Read Status

Errors?

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value



Infrared Encoder/Decoder

Z8 Encore! XP[®] F0823 Series products contain a fully-functional, high-performance UART with Infrared Encoder/Decoder (Endec). The Infrared Endec is integrated with an on-chip UART to allow easy communication between the Z8 Encore! XP and IrDA Physical Layer Specification, Version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers and other infrared enabled devices.

Architecture



Figure 16 displays the architecture of the Infrared Endec.

Figure 16. Infrared Data Communication System Block Diagram

Operation

When the Infrared Endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver through the TXD pin. Similarly, data received from the infrared transceiver is passed to the Infrared Endec through the RXD pin, decoded by the Infrared

Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to its digital representation. The features of this sigma-delta ADC include:

- 10-bit resolution
- Eight single-ended analog input sources are multiplexed with general-purpose I/O ports
- Interrupt upon conversion complete
- Bandgap generated internal voltage reference generator with two selectable levels
- Factory offset and gain calibration

Architecture

Figure 19 displays the major functional blocks of the ADC. An analog multiplexer network selects the ADC input from the available analog pins, ANA0 through ANA7.

Table 83. Flash Frequency High Byte Register (FFREQH)

BITS	7	6	5	4	3	2	1	0
FIELD				FFR	EQH			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FF	AH			

FFREQH—Flash Frequency High Byte High byte of the 16-bit Flash Frequency value

Table 84. Flash Frequency Low Byte Register (FFREQL)

BITS	7	6	5	4	3	2	1	0		
FIELD	FFREQL									
RESET				()					
R/W		R/W								
ADDR				FF	BH					

FFREQL—Flash Frequency Low Byte Low byte of the 16-bit Flash Frequency value

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! XP[®] F0823 Series operation. The feature configuration data is stored in the Flash program memory and loaded into holding registers during Reset. The features available for control through the Flash Option Bits include:

- Watchdog Timer time-out response selection-interrupt or system reset
- Watchdog Timer always on (enabled at Reset)
- The ability to prevent unwanted read access to user code in Program Memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in Program Memory
- Voltage Brownout configuration-always enabled or disabled during STOP mode to reduce STOP mode power consumption
- Factory trimming information for the internal precision oscillator
- Factory calibration values for ADC
- Factory serialization and randomized lot identifier (optional)

Operation

Option Bit Configuration By Reset

Each time the Flash Option Bits are programmed or erased, the device must be Reset for the change to take effect. During any reset operation (System Reset, Power-On Reset, or Stop Mode Recovery), the Flash Option Bits are automatically read from the Flash Program Memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP F0823 Series. Option Bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

Option Bit Types

User Option Bits

The user option bits are contained in the first two bytes of program memory. Access to these bits has been provided because these locations contain application-specific device



Note:

- *This bit only enables the crystal oscillator. Its selection as system clock must be done manually.*
 - 0 = Crystal oscillator is enabled during reset, resulting in longer reset timing
 - *I* = *Crystal oscillator is disabled during reset, resulting in shorter reset timing*
- *¥* Warning: Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin. This is due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.

Trim Bit Address Space

All available Trim bit addresses and their functions are listed in Table 89 through Table 91.

Trim Bit Address 0000H—Reserved

Table 89. Tri	im Options	Bits at A	Address	0000H

BITS	7	6	5	4	3	2	1	0	
FIELD	Reserved								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	Information Page Memory 0020H								
Note: U =	Unchanged by	y Reset. R/W	= Read/Write).					

Reserved—Altering this register may result in incorrect device operation.

Trim Bit Address 0001H—Reserved

Table 90. Trim Option Bits at 0001H

BITS	7	6	5	4	3	2	1	0	
FIELD	Reserved								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	Information Page Memory 0021H								
Note: U =	Unchanged by	y Reset. R/W	= Read/Write) .					



Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)

DEBUG Mode

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP mode
- All enabled on-chip peripherals operate unless in STOP mode
- Automatically exits HALT mode
- Constantly refreshes the Watchdog Timer, if enabled.

Entering DEBUG Mode

The device enters DEBUG mode following the operations below:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (breakpoint) instruction
- If the DBG pin is held Low during the most recent clock cycle of System Reset, the part enters DEBUG mode upon exiting System Reset

Note: Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see OCD Auto-Baud Detector/Generator on page 154).

• If the PA2/RESET pin is held Low while a 32-bit key sequence is issued to the PA0/DBG pin, the DBG feature is unlocked. After releasing PA2/RESET, it is pulled high. At this

Table 117. Absolute Maximum Ratings (Continued)

Parameter	Minimum Maximum	Units	Notes
Maximum current into V_{DD} or out of V_{SS}	125	mA	

Operating temperature is specified in DC Characteristics.

- This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.
- This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

DC Characteristics

Table 118 lists the DC characteristics of the Z8 Encore! $XP^{\ensuremath{\mathbb{R}}}$ F0823 Series products. All voltages are referenced to V_{SS}, the primary system ground.

Table 118. DC Characteristics

		T _A = -40 °C to +105 °C (unless otherwise specified)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
V _{DD}	Supply Voltage	2.7	-	3.6	V	
V _{IL1}	Low Level Input Voltage	-0.3	_	0.3*V _{DD}	V	
V _{IH1}	High Level Input Voltage	0.7*V _{DD}	_	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.
V _{IH2}	High Level Input Voltage	0.7*V _{DD}	_	V _{DD} +0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.
V _{OL1}	Low Level Output Voltage	-	-	0.4	V	I _{OL} = 2 mA; V _{DD} = 3.0 V High Output Drive disabled.
V _{OH1}	High Level Output Voltage	2.4	-	-	V	I _{OH} = -2 mA; V _{DD} = 3.0 V High Output Drive disabled.
V _{OL2}	Low Level Output Voltage	-	-	0.6	V	I _{OL} = 20 mA; V _{DD} = 3.3 V High Output Drive enabled.





Table 127. GFIO FOIL IIIpul Tilling	Table	127.	GPIO	Port	Input	Timing
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		Delay (ns)		
Parameter	Abbreviation	Minimum	Maximum	
T _{S_PORT}	Port Input Transition to XIN Rise Setup Time (Not pictured)	5	_	
T _{H_PORT}	XIN Rise to Port Input Transition Hold Time (Not pictured)	0	_	
T _{SMR}	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1 μs		



Figure 33 and Table 131 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.



Figure 33. UART Timing Without CTS

Table 131. UART	Timing Without CTS	

		Delay (ns)		
Parameter	Abbreviation	Minimum	Maximum	
UART				
T ₁	DE assertion to TXD falling edge (start bit) delay	1 * XIN period	1 bit time	
T ₂	End of Stop Bit(s) to DE deassertion delay (Tx data register is empty)	± 5		

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Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP with 1 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperatur	e: 0 °C to	70 °C						
Z8F0123PB005SC	1 KB	256 B	6	12	2	4	1	PDIP 8-pin package
Z8F0123QB005SC	1 KB	256 B	6	12	2	4	1	QFN 8-pin package
Z8F0123SB005SC	1 KB	256 B	6	12	2	4	1	SOIC 8-pin package
Z8F0123SH005SC	1 KB	256 B	16	18	2	7	1	SOIC 20-pin package
Z8F0123HH005SC	1 KB	256 B	16	18	2	7	1	SSOP 20-pin package
Z8F0123PH005SC	1 KB	256 B	16	18	2	7	1	PDIP 20-pin package
Z8F0123SJ005SC	1 KB	256 B	22	18	2	8	1	SOIC 28-pin package
Z8F0123HJ005SC	1 KB	256 B	22	18	2	8	1	SSOP 28-pin package
Z8F0123PJ005SC	1 KB	256 B	22	18	2	8	1	PDIP 28-pin package
Extended Temperatur	re: -40 °C	to 105 °C	2					
Z8F0123PB005EC	1 KB	256 B	6	12	2	4	1	PDIP 8-pin package
Z8F0123QB005EC	1 KB	256 B	6	12	2	4	1	QFN 8-pin package
Z8F0123SB005EC	1 KB	256 B	6	12	2	4	1	SOIC 8-pin package
Z8F0123SH005EC	1 KB	256 B	16	18	2	7	1	SOIC 20-pin package
Z8F0123HH005EC	1 KB	256 B	16	18	2	7	1	SSOP 20-pin package
Z8F0123PH005EC	1 KB	256 B	16	18	2	7	1	PDIP 20-pin package
Z8F0123SJ005EC	1 KB	256 B	22	18	2	8	1	SOIC 28-pin package
Z8F0123HJ005EC	1 KB	256 B	22	18	2	8	1	SSOP 28-pin package
Z8F0123PJ005EC	1 KB	256 B	22	18	2	8	1	PDIP 28-pin package
Replace C with G for Lea	d-Free Pac	kaging						

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