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#### Details

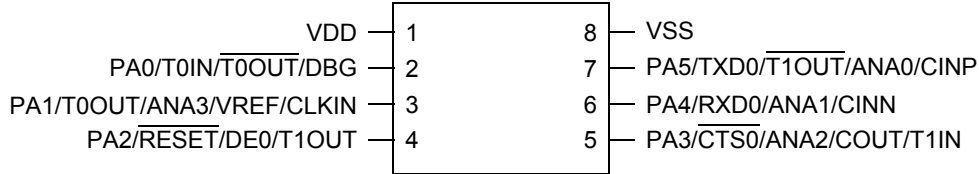
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-QFN (5x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0823qb005ec">https://www.e-xfl.com/product-detail/zilog/z8f0823qb005ec</a>

# Revision History

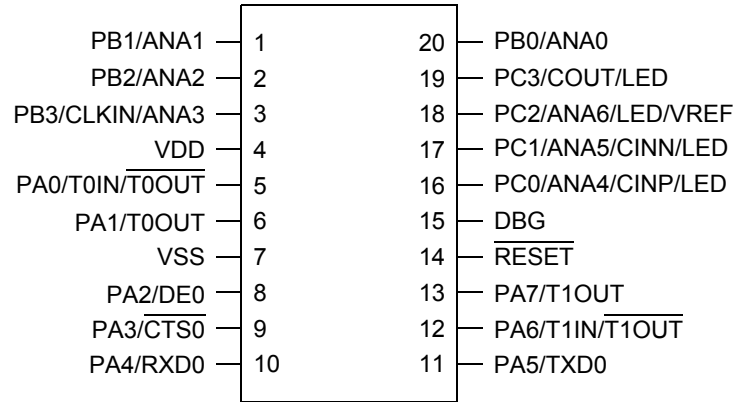
Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

<b>Date</b>	<b>Revision Level</b>	<b>Description</b>	<b>Page No</b>
March 2008	14	Changed title to Z8 Encore! XP F0823 Series and the contents to match the title.	All
December 2007	13	Updated title from Z8 Encore! 8K and 4K Series to Z8 Encore! XP Z8F0823 Series. Updated Figure 3, Table 15, Table 35, Table 59 through Table 61, Table 119, and Part Number Suffix Designations section.	8, 39, 59, 91, 196, and 226
August 2007	12	Updated Table 1, Table 16, and Program Memory section.	2, 42, and 13
June 2007	11	Updated to combine Z8 Encore! 8K and Z8 Encore! 4K Series.	All
December 2006	10	Updated Ordering Information chapter.	217

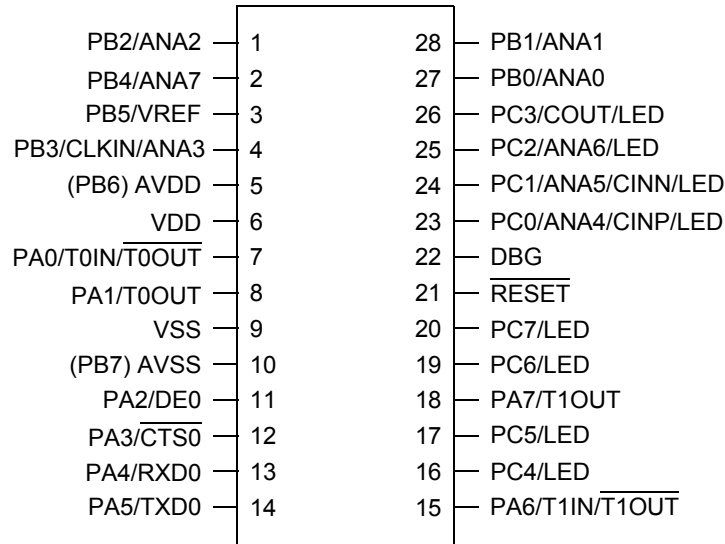
The pin configurations listed are preliminary and subject to change based on manufacturing limitations.



**Figure 2. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 8-Pin SOIC, QFN/MLF-S, or PDIP Package\***



**Figure 3. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 20-Pin SOIC, SSOP or PDIP Package\***



**Figure 4. Z8F08x3, Z8F04x3, F02x3 and Z8F01x3 in 28-Pin SOIC, SSOP or PDIP Package\***

# Address Space

The eZ8 CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more detailed information regarding the eZ8 CPU and its address space, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Register File

The Register File address space in the Z8 Encore! XP<sup>®</sup> MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. Z8 Encore! XP F0823 Series devices contain 256 B-1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

## Program Memory

The eZ8 CPU supports 64 KB of Program Memory address space. Z8 Encore! XP F0823 Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space. Reading from Program Memory addresses outside the available Flash

**Table 26. Port A–C Alternate Function Set 1 Sub-Registers (PxAFS1)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	PAFS17	PAFS16	PAFS15	PAFS14	PAFS13	PAFS12	PAFS11	PAFS10
<b>RESET</b>	00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device)							
<b>R/W</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>ADDR</b>	If 07H in Port A–C Address Register, accessible through the Port A–C Control Register							

PAFS1[7:0]—Port Alternate Function Set to 1

0 = Port Alternate Function selected as defined in Table 14 (see GPIO Alternate Functions on page 36).

1 = Port Alternate Function selected as defined in Table 14 (see GPIO Alternate Functions on page 36).

#### **Port A–C Alternate Function Set 2 Sub-Registers**

The Port A–C Alternate Function Set 2 sub-register (Table 27) is accessed through the Port A–C Control register by writing 08H to the Port A–C Address register. The Alternate Function Set 2 sub-registers selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register is defined in Table 14 in the section GPIO Alternate Functions on page 36.

**Table 27. Port A–C Alternate Function Set 2 Sub-Registers (PxAFS2)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	PAFS27	PAFS26	PAFS25	PAFS24	PAFS23	PAFS22	PAFS21	PAFS20
<b>RESET</b>	00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device)							
<b>R/W</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>ADDR</b>	If 08H in Port A–C Address Register, accessible through the Port A–C Control Register							

PAFS2[7:0]—Port Alternate Function Set 2

0 = Port Alternate Function selected as defined in Table 14 (see GPIO Alternate Functions on page 36).

1 = Port Alternate Function selected as defined in Table 14.

### **Port A–C Input Data Registers**

Reading from the Port A–C Input Data registers (Table 28) returns the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

**Table 28. Port A–C Input Data Registers (PxIN)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
<b>RESET</b>	X	X	X	X	X	X	X	X
<b>R/W</b>	R	R	R	R	R	R	R	R
<b>ADDR</b>	FD2H, FD6H, FDAH							

PIN[7:0]—Port Input Data

Sampled data from the corresponding port pin input.

0 = Input data is logical 0 (Low)

1 = Input data is logical 1 (High)

## Port A–C Output Data Register

The Port A–C Output Data register (Table 29) controls the output data to the pins.

**Table 29. Port A–C Output Data Register (PxOUT)**

<b>BITS</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>FIELD</b>	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
<b>RESET</b>	0	0	0	0	0	0	0	0
<b>R/W</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>ADDR</b>	FD3H, FD7H, FDBH							

POUT[7:0]—Port Output Data

These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation.

0 = Drive a logical 0 (Low).

1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control register bit to 1.

## LED Drive Enable Register

The LED Drive Enable register (Table 30) activates the controlled current drive. The Port C pin must first be enabled by setting the Alternate Function register to select the LED function.

# Interrupt Controller

The interrupt controller on the Z8 Encore! XP® F0823 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 unique interrupt vectors
  - 12 GPIO port pin interrupt sources (two are shared)
  - 8 on-chip peripheral interrupt sources (two are shared)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information on interrupt servicing by the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Interrupt Vector Listing

Table 33 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

► **Note:** *Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.*

Reserved—Must be 0

T1ENH—Timer 1 Interrupt Request Enable High Bit

T0ENH—Timer 0 Interrupt Request Enable High Bit

U0RENH—UART 0 Receive Interrupt Request Enable High Bit

U0TENH—UART 0 Transmit Interrupt Request Enable High Bit

ADCENH—ADC Interrupt Request Enable High Bit

**Table 39. IRQ0 Enable Low Bit Register (IRQ0ENL)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1ENL	T0ENL	U0RENL	U0TENL	Reserved	Reserved	ADCENL
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W
ADDR	FC2H							

Reserved—0 when read

T1ENL—Timer 1 Interrupt Request Enable Low Bit

T0ENL—Timer 0 Interrupt Request Enable Low Bit

U0RENL—UART 0 Receive Interrupt Request Enable Low Bit

U0TENL—UART 0 Transmit Interrupt Request Enable Low Bit

ADCENL—ADC Interrupt Request Enable Low Bit

## IRQ1 Enable High and Low Bit Registers

Table 40 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers (Table 41 and Table 42) form a priority encoded enabling for interrupts in the Interrupt Request 1 register. Priority is generated by setting bits in each register.

**Table 40. IRQ1 Enable and Priority Encoding**

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

where x indicates the register bits from 0–7.



## COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin Timer Input alternate function. The TPOL bit in the Timer Control register selects whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER mode, the prescaler is disabled.

**! Caution:** *The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.*

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Follow the steps below for configuring a timer for COUNTER mode and initiating the count:

1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for COUNTER mode.
  - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER mode. After the first timer Reload in COUNTER mode, counting always begins at the reset value of 0001H. In COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

$$\text{COUNTER Mode Timer Input Transitions} = \text{Current Count Value} - \text{Start Value}$$

**Table 59. Watchdog Timer Reload Upper Byte Register (WDTU)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTU							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF1H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTU—WDT Reload Upper Byte  
Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

**Table 60. Watchdog Timer Reload High Byte Register (WDTH)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	04H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF2H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTH—WDT Reload High Byte  
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 61. Watchdog Timer Reload Low Byte Register (WDTL)**

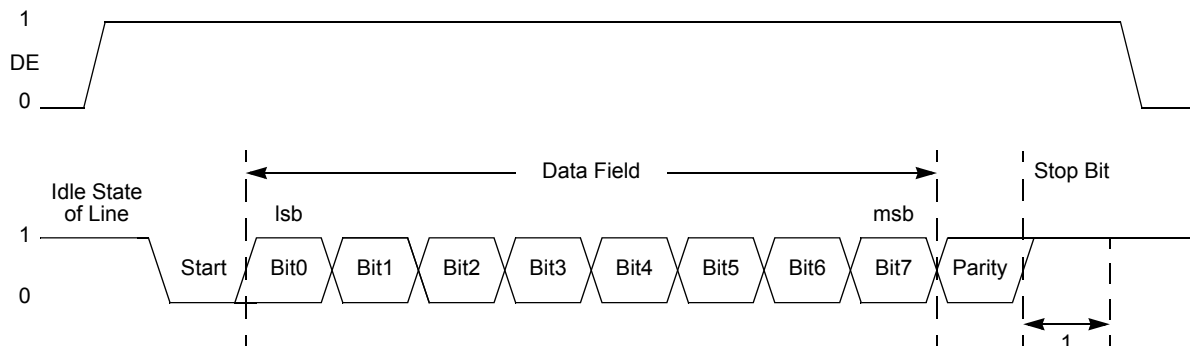
BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
ADDR	FF3H							
R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTL—WDT Reload Low  
Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

## External Driver Enable

The UART provides a Driver Enable (DE) signal for off-chip bus transceivers. This feature reduces the software overhead associated with using a GPIO pin to control the transceiver when communicating on a multi-transceiver bus, such as RS-485.

Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The `DEPOL` bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.



**Figure 14. UART Driver Enable Signal Timing (shown with 1 Stop Bit and Parity)**

The Driver Enable to Start bit setup time is calculated as follows:

$$\left( \frac{1}{\text{Baud Rate (Hz)}} \right) \leq \text{DE to Start Bit Setup Time (s)} \leq \left( \frac{2}{\text{Baud Rate (Hz)}} \right)$$

## UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL};

► **Note:** *This reference is independent of the Comparator reference.*

00= Internal Reference Disabled, reference comes from external pin.

01= Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

REFEXT—External Reference Select

0 = External reference buffer is disabled;  $V_{ref}$  pin is available for GPIO functions

1 = The internal ADC reference is buffered and connected to the  $V_{ref}$  pin

CONT

0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles.

1 = Continuous conversion. ADC data updated every 256 system clock cycles.

ANAIN[3:0]—Analog Input Select

These bits select the analog input for conversion. Not all port pins in this list are available in all packages for Z8 Encore! XP<sup>®</sup> F0823 Series. For information on the port pins available with each package style, see Pin Description on page 7. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

Single-Ended:

0000 = ANA0

0001 = ANA1

0010 = ANA2

0011 = ANA3

0100 = ANA4

0101 = ANA5

0110 = ANA6

0111 = ANA7

1000 = Reserved

1001 = Reserved

1010 = Reserved

1011 = Reserved

1100 = Reserved

1101 = Reserved

1110 = Reserved

1111 = Reserved

**Table 76. Comparator Control Register (CMP0)**

BITS	7	6	5	4	3	2	1	0
FIELD	INPSEL	INNSEL	REFLVL				Reserved	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F90H							

INPSEL—Signal Select for Positive Input

0 = GPIO pin used as positive comparator input

1 = temperature sensor used as positive comparator input

INNSEL—Signal Select for Negative Input

0 = internal reference disabled, GPIO pin used as negative comparator input

1 = internal reference enabled as negative comparator input

REFLVL—Internal Reference Voltage Level

► **Note:** *This reference is independent of the ADC voltage reference.*

0000 = 0.0 V

0001 = 0.2 V

0010 = 0.4 V

0011 = 0.6 V

0100 = 0.8 V

0101 = 1.0 V (Default)

0110 = 1.2 V

0111 = 1.4 V

1000 = 1.6 V

1001 = 1.8 V

1010–1111 = Reserved

Reserved—R/W bits must be 0 during writes; 0 when read



# Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a non-standard frequency or use the automatic factory-trimmed version to achieve a 5.53 MHz frequency. The features of IPO include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53 MHz or 32.8 kHz (contains both a fast and a slow mode)
- Trimming possible through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

## Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53 MHz (fast mode) or 32.8 kHz (slow mode) is required. This trimming is done at +30 °C and a supply voltage of 3.3 V, so accuracy of this operating point is optimal.

Power down this block for minimum system power. By default, the oscillator is configured through the Flash Option bits. However, the user code can override these trim values as described in Trim Bit Address Space on page 146.

Select one of the two frequencies for the oscillator: 5.53 MHz and 32.8 kHz, using the OSCSEL bits in the Oscillator Control on page 165.

**Table 110. CPU Control Instructions (Continued)**

Mnemonic	Operands	Instruction
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

**Table 111. Load Instructions**

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

**Table 112. Logical Instructions**

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR



**Table 115. eZ8 CPU Instruction Summary (Continued)**

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
HALT	HALT Mode			7F	–	–	–	–	–	–	1	2
INC dst	dst ← dst + 1	R		20	–	*	*	–	–	–	2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	dst ← dst + 1	RR		A0	–	*	*	*	–	–	2	5
		IRR		A1							2	6
IRET	FLAGS ← @SP SP ← SP + 1 PC ← @SP SP ← SP + 2 IRQCTL[7] ← 1			BF	*	*	*	*	*	*	1	5
JP dst	PC ← dst	DA		8D	–	–	–	–	–	–	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true PC ← dst	DA		0D-FD	–	–	–	–	–	–	3	2
JR dst	PC ← PC + X	DA		8B	–	–	–	–	–	–	2	2
JR cc, dst	if cc is true PC ← PC + X	DA		0B-FB	–	–	–	–	–	–	2	2
LD dst, rc	dst ← src	r	IM	0C-FC	–	–	–	–	–	–	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	lr	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	4
		R	IM	E6							3	2
		IR	IM	E7							3	3
		lr	r	F3							2	3
		IR	R	F5							3	3
Flags Notation:		* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1						

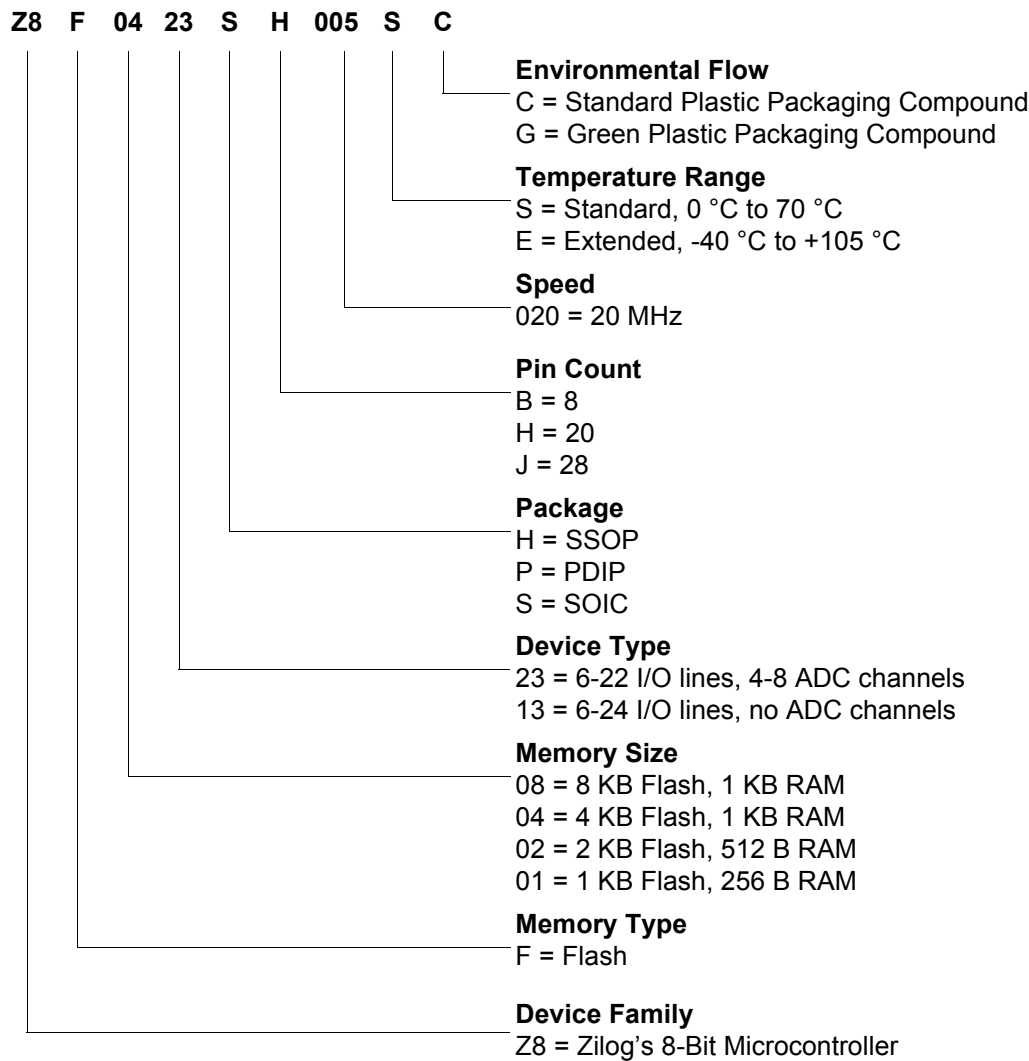
**Table 116. Opcode Map Abbreviations**

<b>Abbreviation</b>	<b>Description</b>	<b>Abbreviation</b>	<b>Description</b>
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 118. DC Characteristics (Continued)

Symbol	Parameter	T <sub>A</sub> = -40 °C to +105 °C (unless otherwise specified)			Units	Conditions
		Minimum	Typical	Maximum		
V <sub>OH2</sub>	High Level Output Voltage	2.4	–	–	V	I <sub>OH</sub> = -20 mA; V <sub>DD</sub> = 3.3 V High Output Drive enabled.
I <sub>IH</sub>	Input Leakage Current	–	±0.002	±5	µA	V <sub>IN</sub> = V <sub>DD</sub> V <sub>DD</sub> = 3.3 V;
I <sub>IL</sub>	Input Leakage Current	–	±0.007	±5	µA	V <sub>IN</sub> = V <sub>SS</sub> V <sub>DD</sub> = 3.3 V;
I <sub>TL</sub>	Tristate Leakage Current	–	–	±5	µA	
I <sub>LED</sub>	Controlled Current Drive	1.8	3	4.5	mA	{AFS2,AFS1} = {0,0}
		2.8	7	10.5	mA	{AFS2,AFS1} = {0,1}
		7.8	13	19.5	mA	{AFS2,AFS1} = {1,0}
		12	20	30	mA	{AFS2,AFS1} = {1,1}
C <sub>PAD</sub>	GPIO Port Pad Capacitance	–	8.0 <sup>2</sup>	–	pF	
C <sub>XIN</sub>	XIN Pad Capacitance	–	8.0 <sup>2</sup>	–	pF	
C <sub>XOUT</sub>	XOUT Pad Capacitance	–	9.5 <sup>2</sup>	–	pF	
I <sub>PU</sub>	Weak Pull-up Current	30	100	350	µA	V <sub>DD</sub> = 3.0 V–3.6 V
V <sub>RAM</sub>	RAM Data Retention Voltage	TBD			V	Voltage at which RAM retains static values; no reading or writing is allowed.
<b>Notes</b> 1. This condition excludes all pins that have on-chip pull-ups, when driven Low. 2. These values are provided for design guidance only and are not tested in production.						

Part Number Suffix Designations



- ADC data high byte (ADCDH) 124
- ADC data low bits (ADCDL) 125
- flash control (FCTL) 137, 143, 144
- flash high and low byte (FFREQH and FREEQL) 139
- flash page select (FPS) 138, 139
- flash status (FSTAT) 137
- GPIO port A-H address (PxADDR) 44
- GPIO port A-H alternate function sub-registers 46
- GPIO port A-H control address (PxCTL) 45
- GPIO port A-H data direction sub-registers 45
- OCD control 161
- OCD status 163
- UARTx baud rate high byte (UxBRH) 110
- UARTx baud rate low byte (UxBRL) 110
- UARTx Control 0 (UxCTL0) 107, 110
- UARTx control 1 (UxCTL1) 108
- UARTx receive data (UxRXD) 105
- UARTx status 0 (UxSTAT0) 105
- UARTx status 1 (UxSTAT1) 106
- UARTx transmit data (UxTXD) 104
- Watchdog Timer control (WDTCTL) 90, 128
- watch-dog timer control (WDTCTL) 167
- Watchdog Timer reload high byte (WDTH) 91
- Watchdog Timer reload low byte (WDTL) 91
- Watchdog Timer reload upper byte (WD-TU) 91
- register file 13
- register pair 173
- register pointer 174
- reset
  - and stop mode characteristics 22
  - and stop mode recovery 21
  - carry flag 176
  - sources 22
- RET 178
- return 178
- RL 178
- RLC 178
- rotate and shift instructions 178
- rotate left 178
- rotate left through carry 178
- rotate right 178
- rotate right through carry 178
- RP 174
- RR 173, 178
- rr 173
- RRC 178
- S**
- SBC 175
- SCF 176, 177
- second opcode map after 1FH 191
- set carry flag 176, 177
- set register pointer 177
- shift right arithmetic 179
- shift right logical 179
- signal descriptions 9
- single-sho conversion (ADC) 119
- software trap 178
- source operand 174
- SP 174
- SRA 179
- src 174
- SRL 179
- SRP 177
- stack pointer 174
- STOP 177
- STOP mode 31, 177
- Stop Mode Recovery
  - sources 26
  - using a GPIO port pin transition 27, 28
  - using Watchdog Timer time-out 27
- SUB 175
- subtract 175
- subtract - extended addressing 175
- subtract with carry 175
- subtract with carry - extended addressing 175
- SUBX 175
- SWAP 179
- swap nibbles 179
- symbols, additional 174