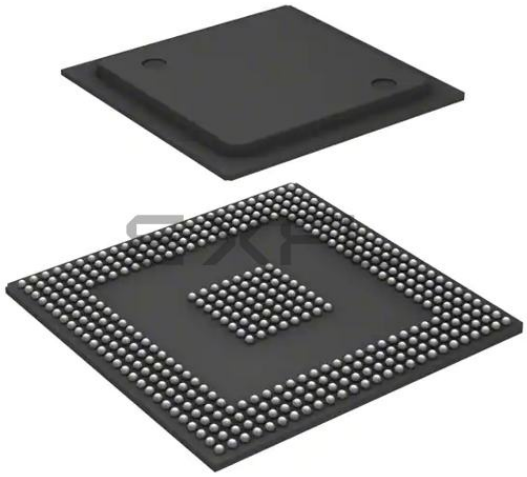

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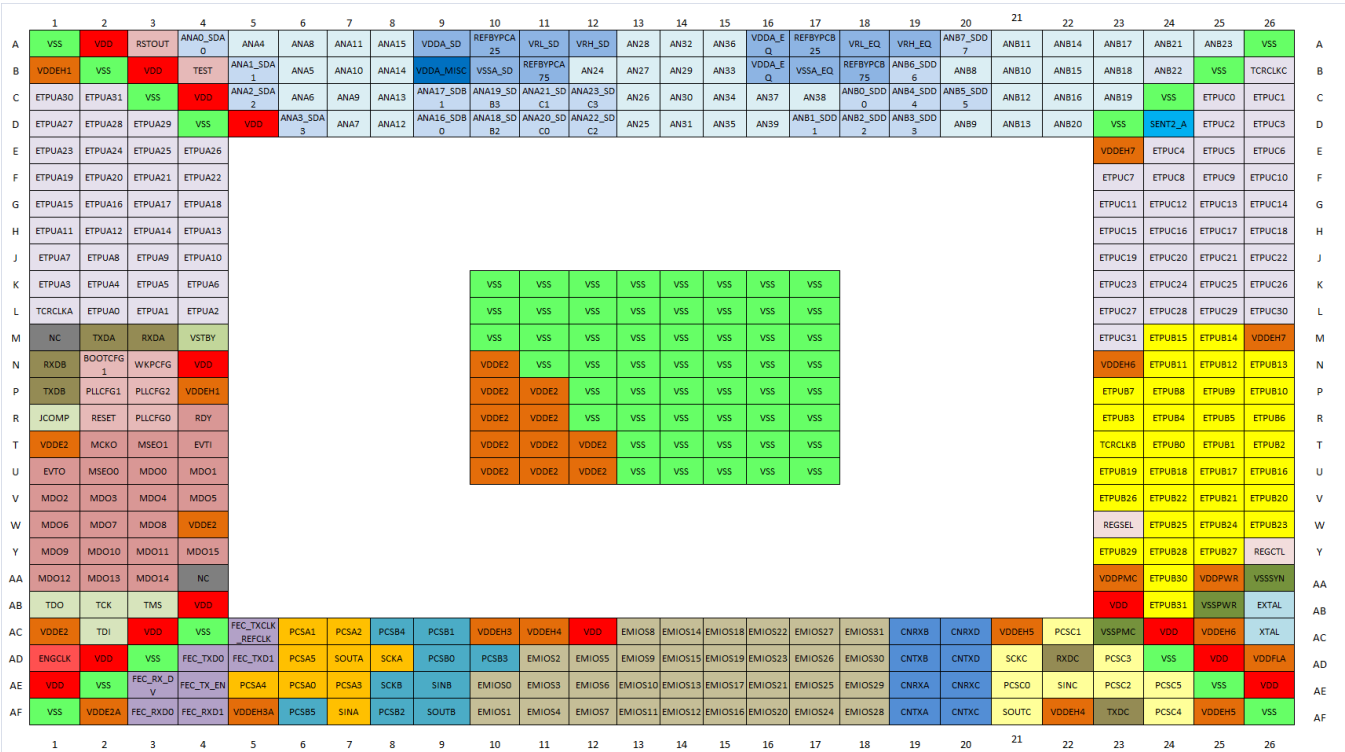
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck2mme3

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	AN87_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	AN88	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.

3.4 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted.

If the device operating conditions are exceeded, the functionality of the device is not guaranteed.

Table 3. Device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
f_{SYS}	Device operating frequency[1]	—	—	—	264[2]	MHz
f_{PLATF}	Platform operating frequency	—	—	—	132	MHz
f_{ETPU}	eTPU operating frequency	—	—	—	200	MHz
f_{EBI}	EBI operating frequency	—	—	—	66	MHz
f_{PER}	Peripheral block operating frequency	—	—	—	132	MHz
f_{FM_PER}	Frequency-modulated peripheral block operating frequency	—	—	—	132	MHz
t_{CYC}	Platform clock period	—	—	—	$1/f_{PLATF}$	ns
t_{CYC_ETPU}	eTPU clock period	—	—	—	$1/f_{ETPU}$	ns
t_{CYC_PER}	Peripheral clock period	—	—	—	$1/f_{PER}$	ns
Temperature						
T_J	Junction operating temperature range	Packaged devices	–40.0	—	150.0	°C
T_A (T_L to T_H)	Ambient operating temperature range	Packaged devices	–40.0	—	125.0[3]	°C
Voltage						
V_{DD}	External core supply voltage[4, 5]	LVD/HVD enabled	1.2	—	1.32	V
		LVD/HVD disabled[6, 7, 8, 9]	1.2	—	1.38	
V_{DDA_MISC}	TRNG and IRC supply voltage	—	3.5	—	5.5	V
V_{DDEx}	I/O supply voltage (fast I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEHx}[9]	I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEH1}	eTPU_A, eSCI_A, eSCI_B, and configuration I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
V_{DDPMC}[10]	Power Management Controller (PMC) supply voltage	Full functionality	3.15	—	5.5	V
V_{DDPWR}	SMPS driver supply voltage	Reference to V_{SSPWR}	3.0	—	5.5	V
V_{DDFLA}	Flash core voltage	—	3.15	—	3.6	V
V_{STBY}	RAM standby supply voltage	—	0.95[11]	—	5.5	V

Table continues on the next page...

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be “clipped.”
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5*V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range 3.6 V < V_{DDA_SD} < 4.0 V: SNR parameter degrades by 3 dB. SDADC is functional in the range 3.0 V < V_{RH_SD} < 4.0 V: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} – f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of (V_{RH_SD} - V_{RL_SD}) / 2.
14. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

The following table shows the recommended components to be used in LDO regulation mode.

Table 25. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	NPN BJT	h_{FE} = 400	NJD2873: ON Semiconductor LDO voltage regulator controller (VRC)
CI	Capacitor	4.7 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.047–0.049 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to NPN collector)
CB	Capacitor	0.1 µF - 7 V	Ceramic V_{DDPWR}
R	Resistor	Application specific	Optional; reduces thermal loading on the NPN with high V_{DDPMC} levels

The following diagram shows the LDO configuration connection.

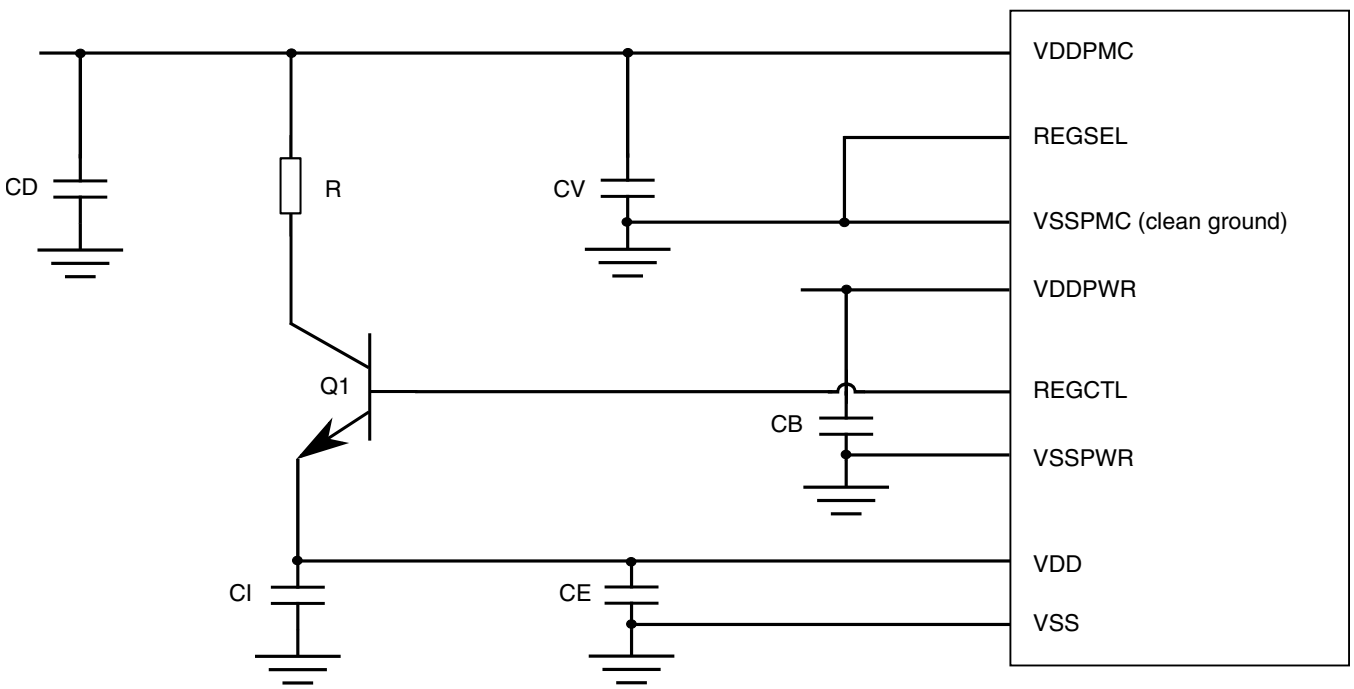


Figure 12. VRC 1.2 V LDO configuration

3.11.1.2 SMPS mode recommended external components and characteristics

The following table shows the recommended components to be used in SMPS regulation mode.

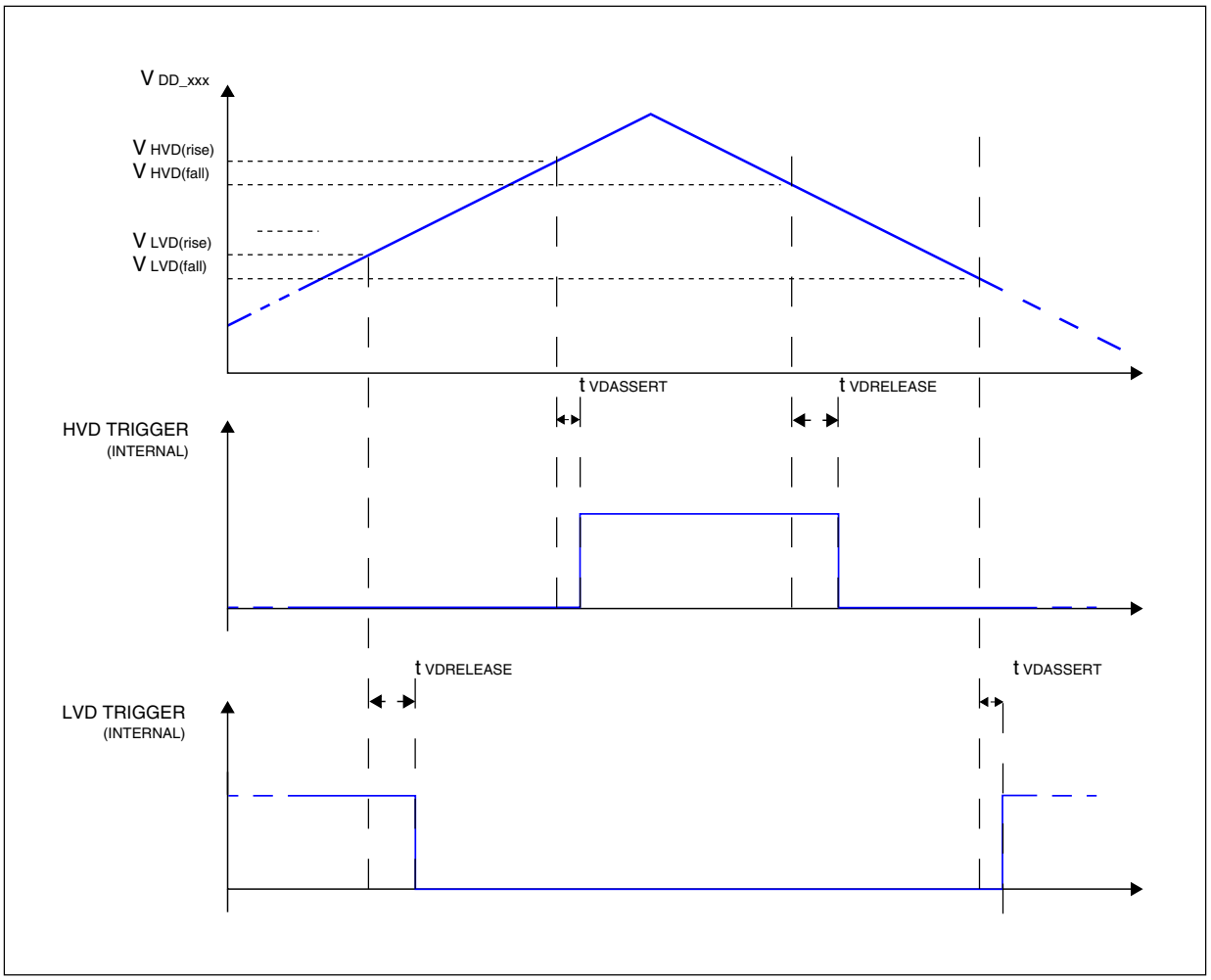


Figure 15. Voltage monitor threshold definition

Table 29. Voltage monitor electrical characteristics[1, 2]

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR098_c[3]	LV internal supply power on reset	Rising voltage (powerup)	N/A	No	Enab.	960	1010	1060	mV
		Falling voltage (power down)				940	990	1040	
LVD_core_hot	LV internal[4] supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	1100	1140	1183	mV
		Falling voltage (untrimmed)				1080	1120	1163	
		Rising voltage (trimmed)				1142	1165	1183	
		Falling voltage (trimmed)				1122	1145	1163	
LVD_core_cold	LV external[5] supply low voltage monitoring	Rising voltage	4bit	Yes	Disab.	1165	1180	1198	mV
		Falling voltage				1136	1160	1178	
HVD_core	LV internal cold supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	1338	1365	1385	mV
		Falling voltage				1318	1345	1365	

Table continues on the next page...

Table 29. Voltage monitor electrical characteristics[1, 2] (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR_HV	HV V_{DDPMC} supply power on reset threshold	Rising voltage (powerup)	N/A	No	Enab.	2444	2600	2756	mV
		Falling voltage (power down)				2424	2580	2736	
LVD_HV	HV internal V_{DDPMC} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2946	3010	3066	
		Falling voltage (trimmed)				2934	2998	3044	
HVD_HV	HV internal V_{DDPMC} supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	5696	5860	5968	mV
		Falling voltage				5666	5830	5938	
LVD_FLASH	FLASH supply low voltage monitoring[6]	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2956	3010	3053	
		Falling voltage (trimmed)				2944	2998	3041	
HVD_FLASH	FLASH supply high voltage monitoring[6]	Rising voltage	4bit	Yes	Disab.	3456	3530	3584	mV
		Falling voltage				3426	3500	3554	
LVD_IO	Main I/O V_{DDEH1} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	3250	3350	3488	mV
		Falling voltage (untrimmed)				3220	3320	3458	
		Rising voltage (trimmed)				3347	3420	3468	
		Falling voltage (trimmed)				3317	3390	3438	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	µs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	µs

1. LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed; LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.
2. HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed; HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.
3. POR098_c threshold is an untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
6. V_{DDFLA} range is guaranteed when internal flash memory regulator is used.

3.11.4 Power sequencing requirements

Requirements for power sequencing include the following.

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
   - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

   During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

   During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

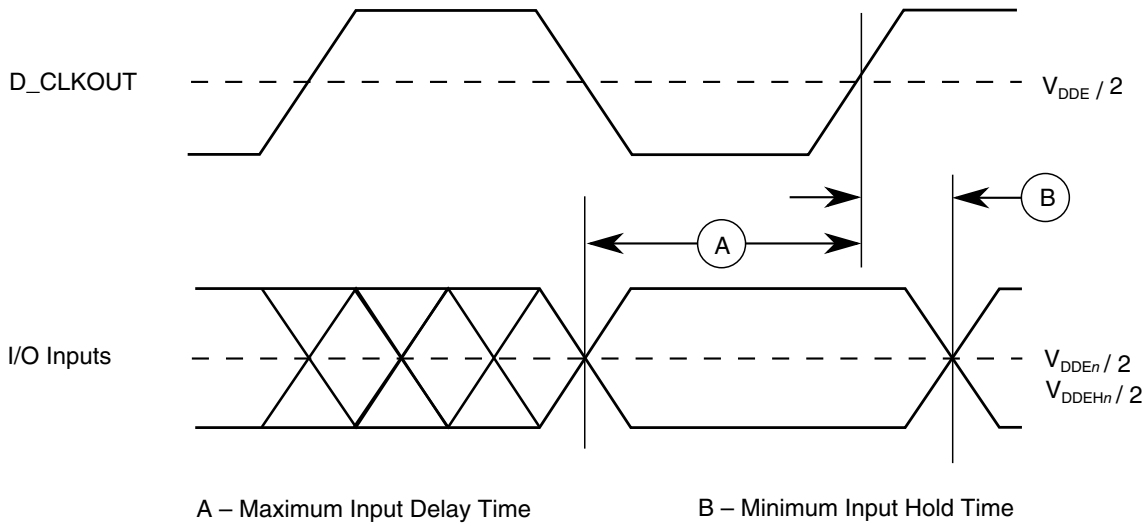


Figure 17. Generic input setup/hold timing

3.13.2 Reset and configuration pin timing

Table 35. Reset and configuration pin timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, TA = TL to TH.
2. For further information on t_{cyc}, see Table 3.

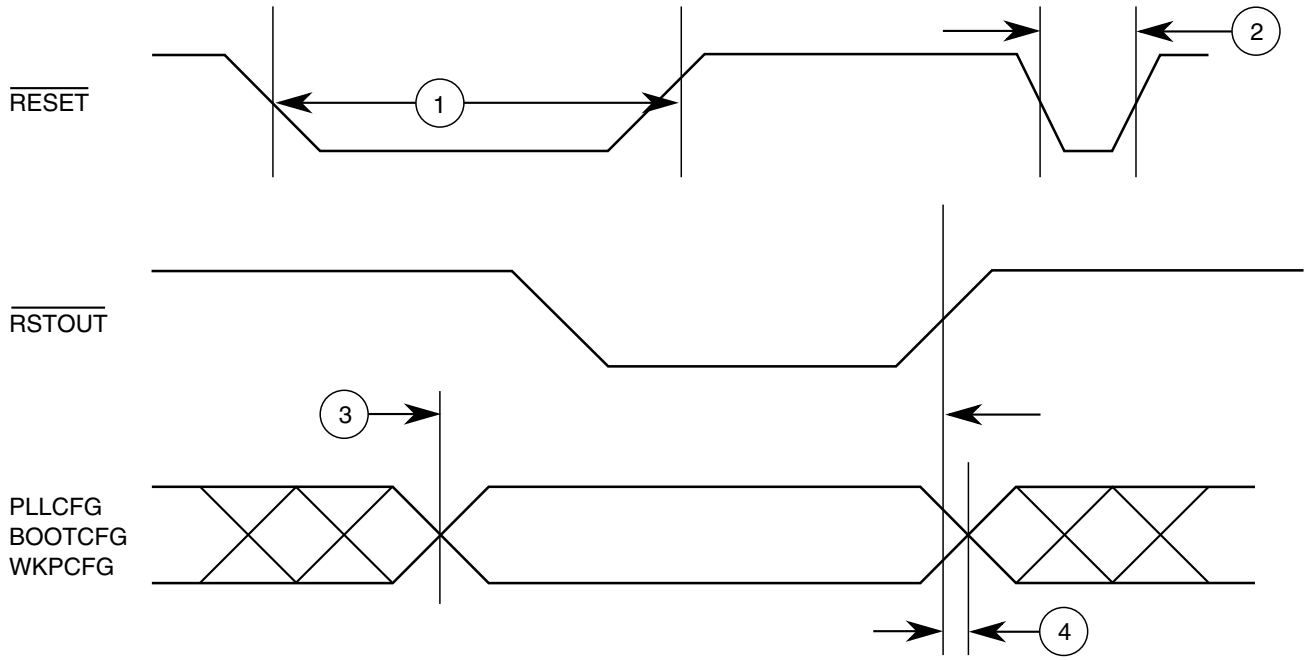


Figure 18. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

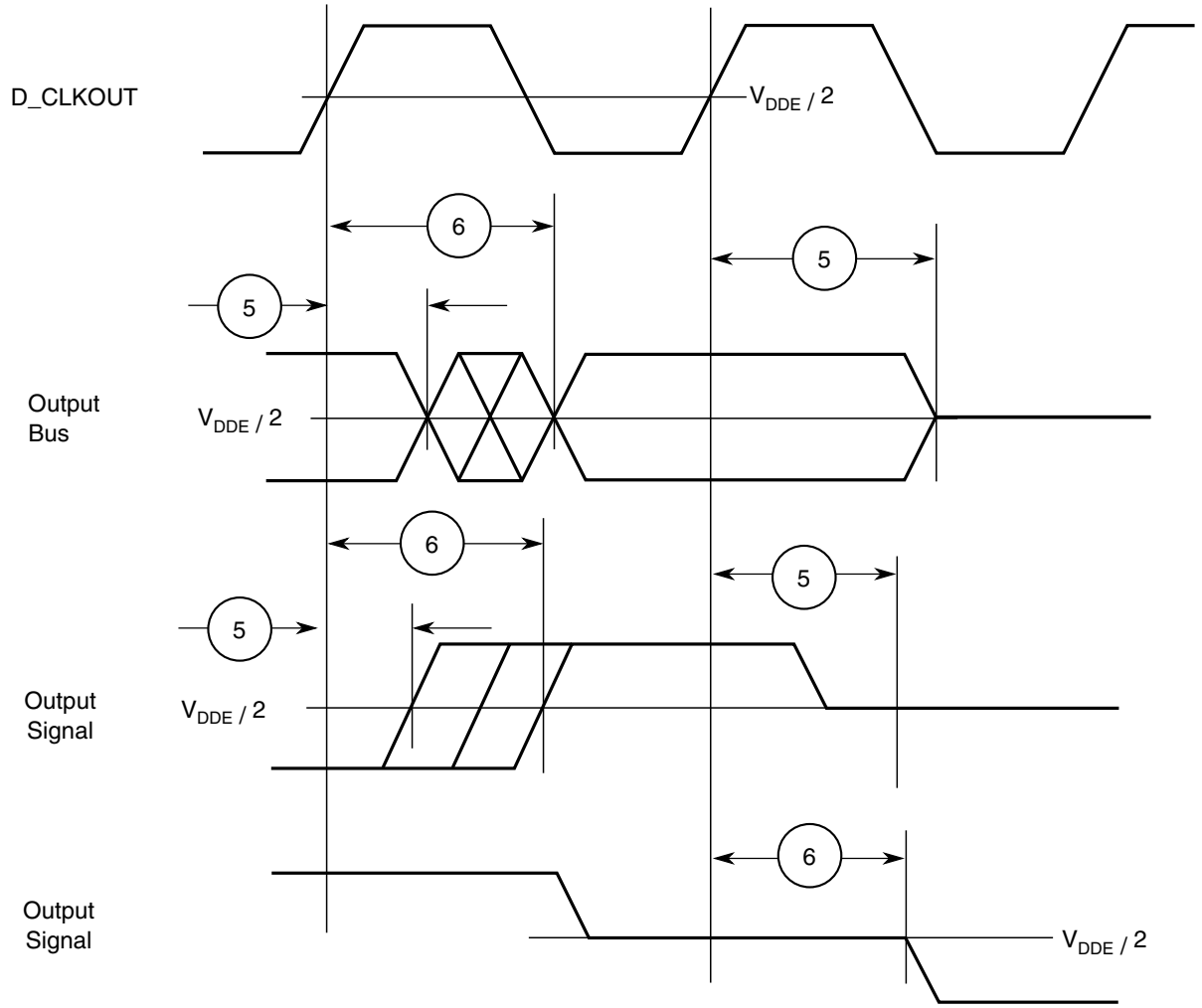


Figure 26. Synchronous output timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
8. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
9. PCSx and $\overline{\text{PCSS}}$ using same pad configuration.
10. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

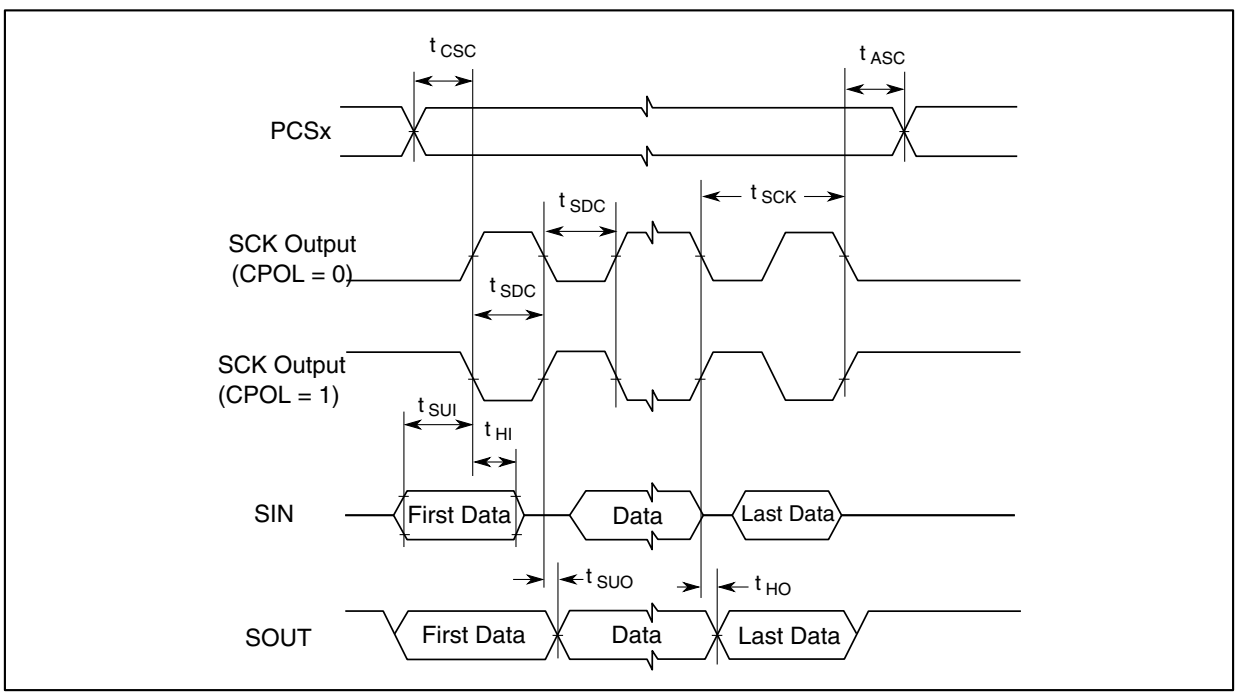


Figure 32. DSPI CMOS master mode – classic timing, CPHA = 0

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2] (continued)

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
3	t_{CSH}	PCS hold after SCK[6]	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	–33	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–35	—	ns
4	t_{SDC}	SCK duty cycle[7]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	ns
			PCR[SRC]=01b	50 pF	—	18.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	ns
			PCR[SRC]=01b	50 pF	–21.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

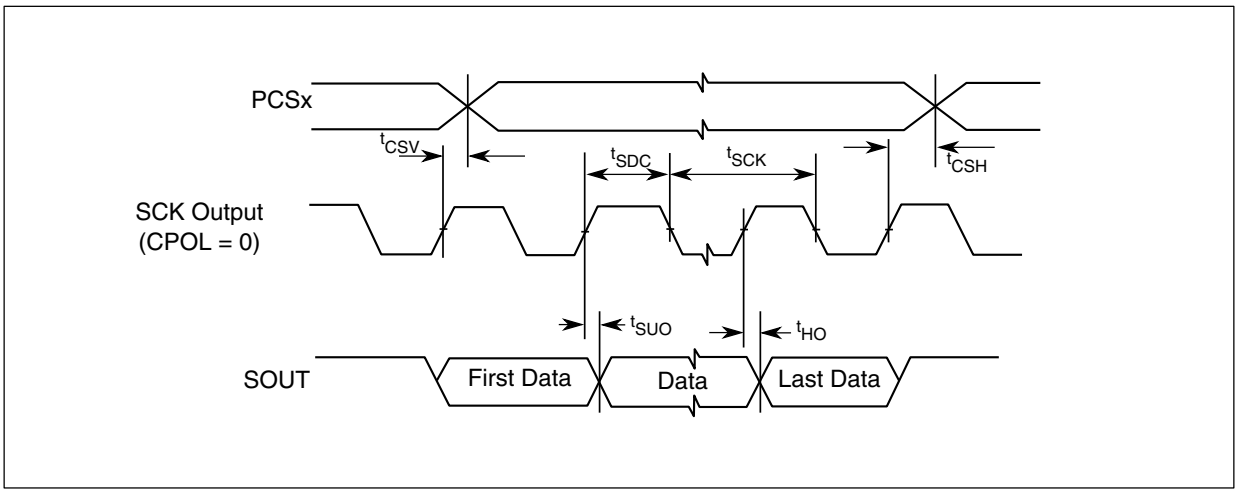


Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

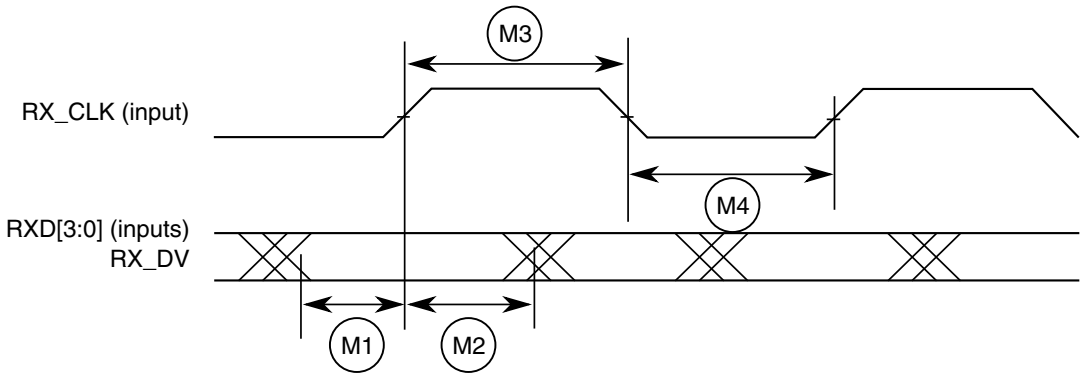


Figure 41. MII receive signal timing diagram

3.13.10.2 MII transmit signal timing (TXD[3:0], TX_EN, and TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of noncompliant MII PHYs.

Refer to the *MPC5777C Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 49. MII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN invalid	4.5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately