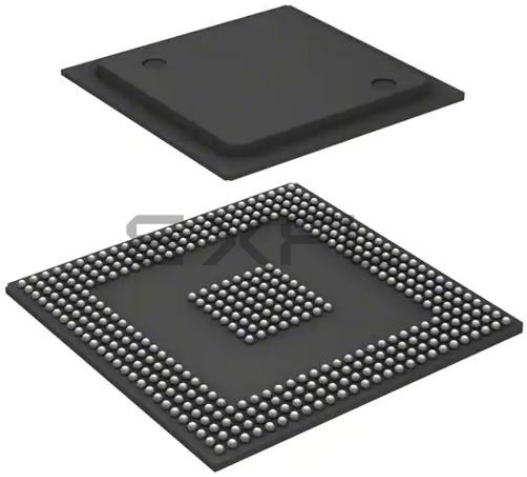

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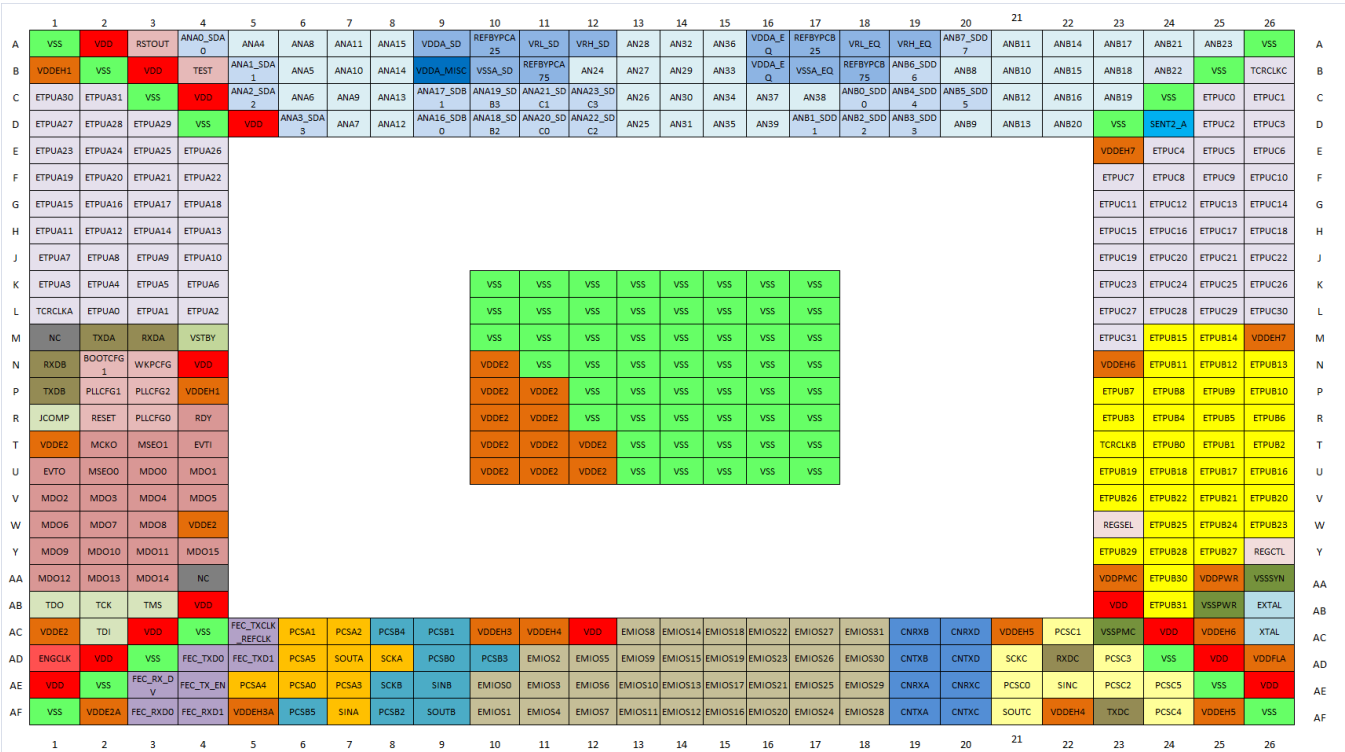
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck2mme3r



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	AN87_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	AN88	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
MSL	Moisture sensitivity level[11]	—	—	3	—

1. Voltages are referred to V_{SS} if not specified otherwise
2. Allowed 1.45 V – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C; remaining time as defined in note 3 and note 4
3. Allowed 1.375 V – 1.45 V for 10 hours cumulative time at maximum T_J = 150 °C; remaining time as defined in note 4
4. 1.32 V – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J = 150 °C
5. Allowed 5.5 V – 6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C; remaining time at or below 5.5 V
6. Allowed 3.6 V – 4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C; remaining time at or below 3.6 V
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
9. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.
10. Solder profile per IPC/JEDEC J-STD-020D
11. Moisture sensitivity per JEDEC test method A112

3.2 Electromagnetic interference (EMI) characteristics

Test reports with EMC measurements to IC-level IEC standards are available on request.

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to nxp.com and perform a keyword search for "radiated emissions."

3.3 Electrostatic discharge (ESD) characteristics

Table 2. ESD Ratings[1, 2]

Symbol	Parameter	Conditions	Value	Unit
V_{HBM}	ESD for Human Body Model (HBM)	All pins	2000	V
V_{CDM}	ESD for Charged Device Model (CDM)	Corner pins	750	V
		Non-corner pins	500	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 5 shows output DC electrical characteristics.

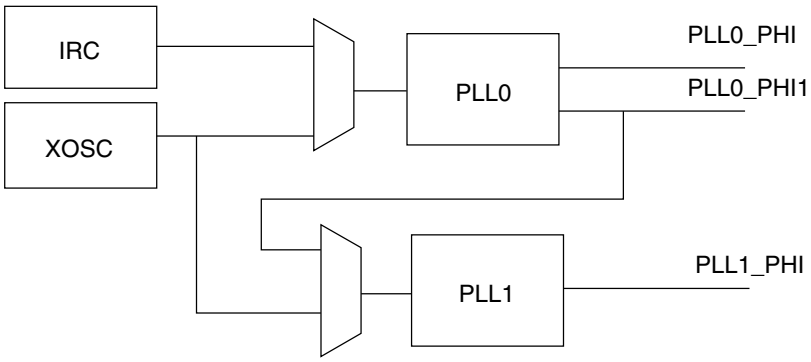


Figure 6. PLL integration

3.7.1 PLL electrical specifications

Table 12. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1, 2]	—	8	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	PLL0 output frequency	—	4.762	—	200	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 200 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[3]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	7.5	mA

1. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz to 20 MHz.
2. PLL0IN clock retrieved directly from either internal IRC or external XOSC clock. Input characteristics are granted when using internal IRC or external oscillator is used in functional mode.
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

Table 14. External oscillator (XOSC) electrical specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

1. This value is determined by the crystal manufacturer and board design.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
4. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating in a "low" transconductance range. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating in a "medium" or "high" transconductance range, the integrated load capacitor value is selected via software to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
5. Select a "low," "medium," or "high" setting using the UTEST Miscellaneous DCF client's XOSC_LF_EN and XOSC_EN_HIGH fields. "Low" is the setting commonly used for crystals at 8 MHz, "medium" is commonly used for crystals greater than 8 MHz to 20 MHz, and "high" is commonly used for crystals greater than 20 MHz to 40 MHz. However, the user must characterize carefully to determine the best g_m setting for the intended application because crystal load capacitance, board layout, and other factors affect the g_m value that is needed. The user may need an additional Rshunt to optimize g_m depending on the system environment. Use of overtone crystals is not recommended.
6. Amplitude on the EXTAL pin after startup is determined by the ALC block (that is, the Automatic Level Control Circuit). The function of the ALC is to provide high drive current during oscillator startup, while reducing current after oscillation to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
7. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 7.

Table 15. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
00000	1.8
00001	2.8
00010	3.7
00011	4.6
00100	5.6
00101	6.5
00110	7.4
00111	8.4
01000	9.3
01001	10.2
01010	11.2
01011	12.1
01100	13.0
01101	13.9

Table continues on the next page...

3.10.1 LFAST interface timing diagrams

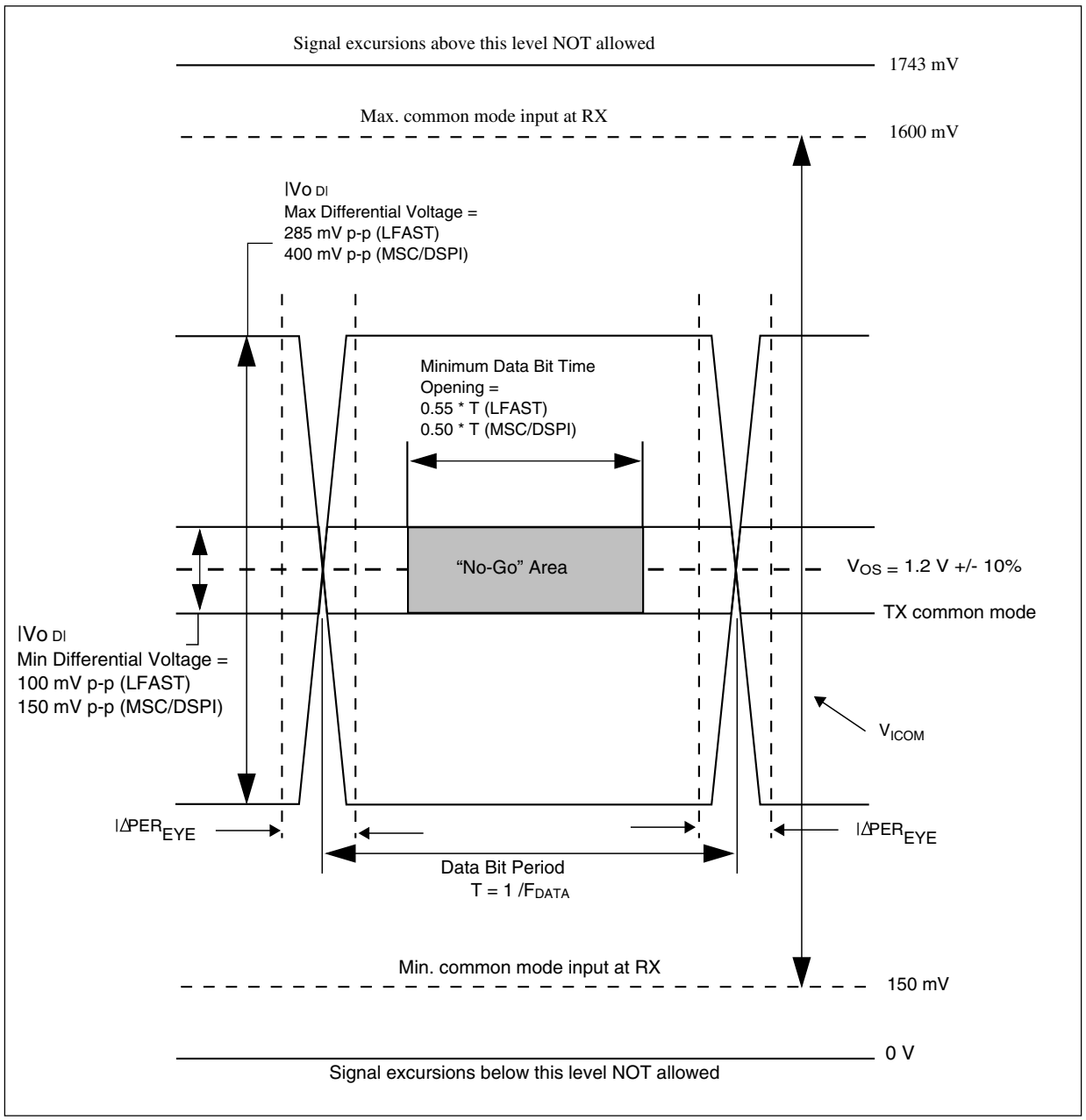


Figure 8. LFAST and MSC/DSPI LVDS timing definition

Table 20. LVDS pad startup and receiver electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to Normal mode)[5]	—	—	0.4	2.75	µs
t_{SM2NM_TX}	Transmitter startup time (Sleep mode to Normal mode)[6]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	Receiver startup time (power down to Normal mode)[7]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to Sleep mode)[8]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[9]	—	1.6[10]	V
$\|\Delta VI\|$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	V_{DDEH} = 3.0 V to 5.5 V	80	125	150	Ω
C_{IN}	Differential input capacitance[11]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules.
3. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
4. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
5. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
6. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
7. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
8. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
9. Absolute min = 0.15 V – (285 mV/2) = 0 V
10. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
11. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in Figure 11.

Table 21. LFAST transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	240	Mbps

Table continues on the next page...

Table 21. LFAST transmitter electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	110	200	285	mV
t_{TR}	Rise/fall time (10% – 90% of swing)[2,3]	—	0.26	—	1.5	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	12.0	pF
		V_{DDE} = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst-case internal capacitance values shown in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load CL.

Table 22. MSC/DSPI LVDS transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing)[2,3]	—	0.8	—	4.0	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	50	pF
		V_{DDE} = 3.0 V	—	—	39	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst-case internal capacitance values given in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load C_L.

Table 26. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	p-MOS	3 A - 20 V	SQ2301ES / FDC642P or equivalent: low threshold p-MOS, Vth < 2.0 V, Rdson @ 4.5 V < 100 mΩ, Cg < 5 nF
D1	Schottky	2 A - 20 V	SS8P3L or equivalent: Vishay™ low Vf Schottky diode
L	Inductor	3−4 µH - 1.5 A	Buck shielded coil low ESR
CI	Capacitor	22 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.1 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF capacitor in parallel)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to the p-MOS source)
R	Resistor	2.0-4.7 kΩ	Pullup for power p-MOS gate
CB	Capacitor	22 µF - 20 V	Ceramic, connect 100 nF capacitor in parallel (as close as possible to package to reduce current loop from V_{DDPWR} to V_{SSPWR})

The following diagram shows the SMPS configuration connection.

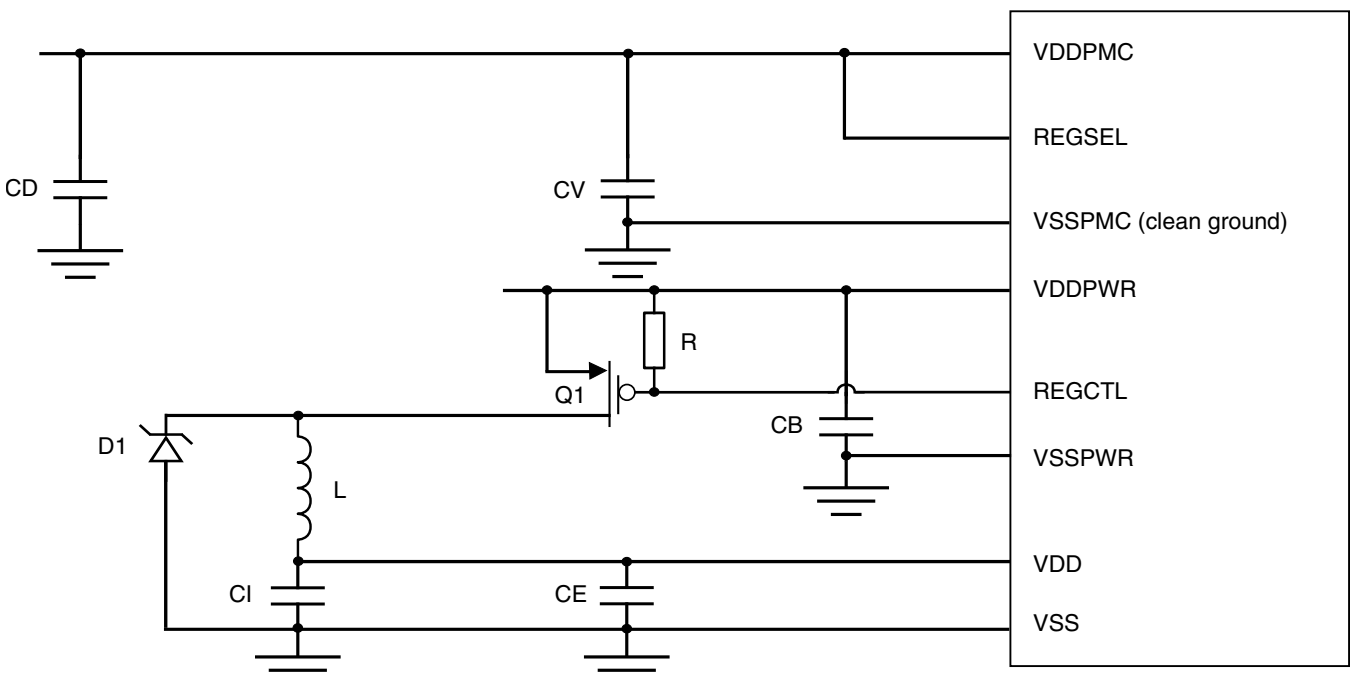


Figure 13. SMPS configuration

NOTE

The REGSEL pin is tied to V_{DDPMC} to select SMPS. If REGSEL is 0, the chip boots with the linear regulator.

See Power sequencing requirements for details about V_{DDPMC} and V_{DDPWR}.

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

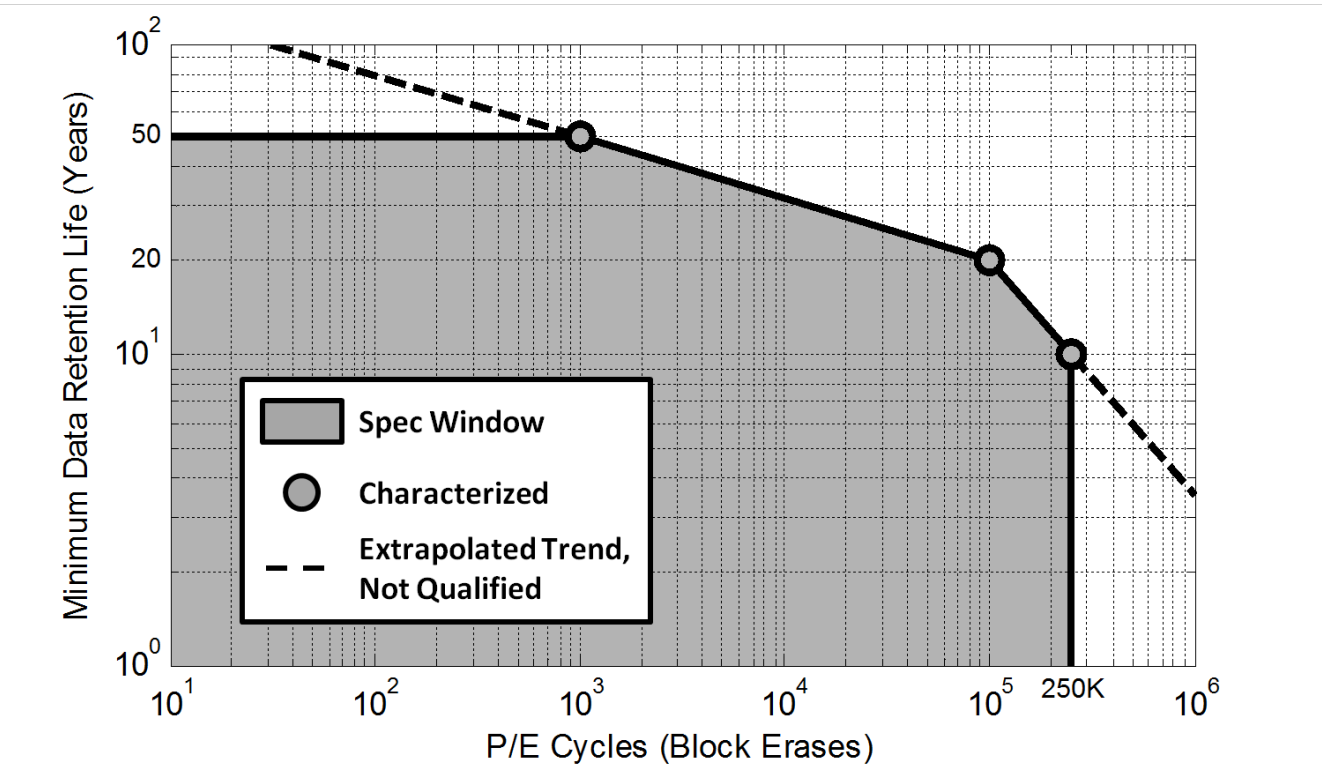
1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
   - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

   During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

   During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

3.12.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.12.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns

Table continues on the next page...

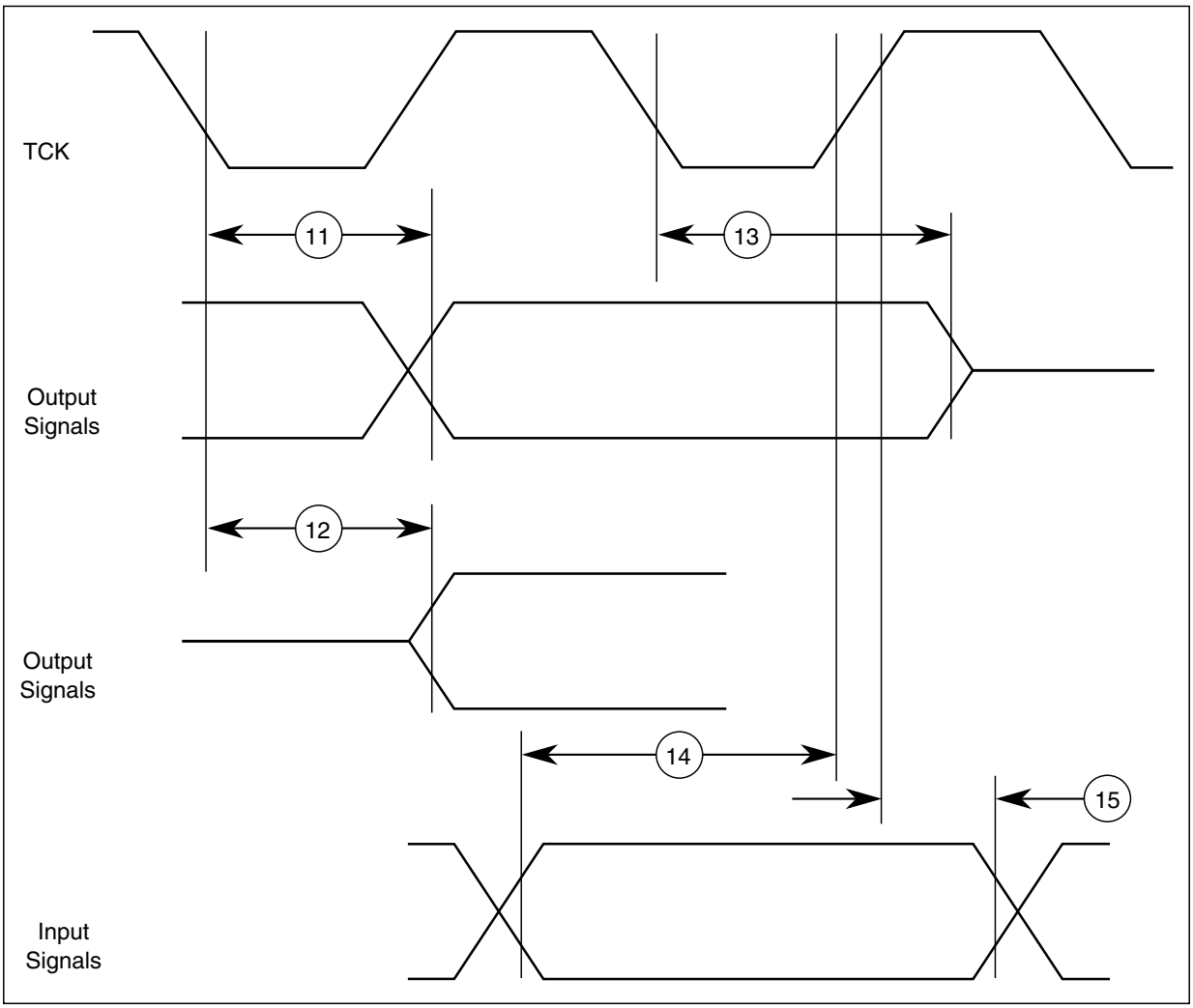


Figure 22. JTAG boundary scan timing

3.13.4 Nexus timing

Table 37. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	2[3]	—	t_{CYC}

Table continues on the next page...

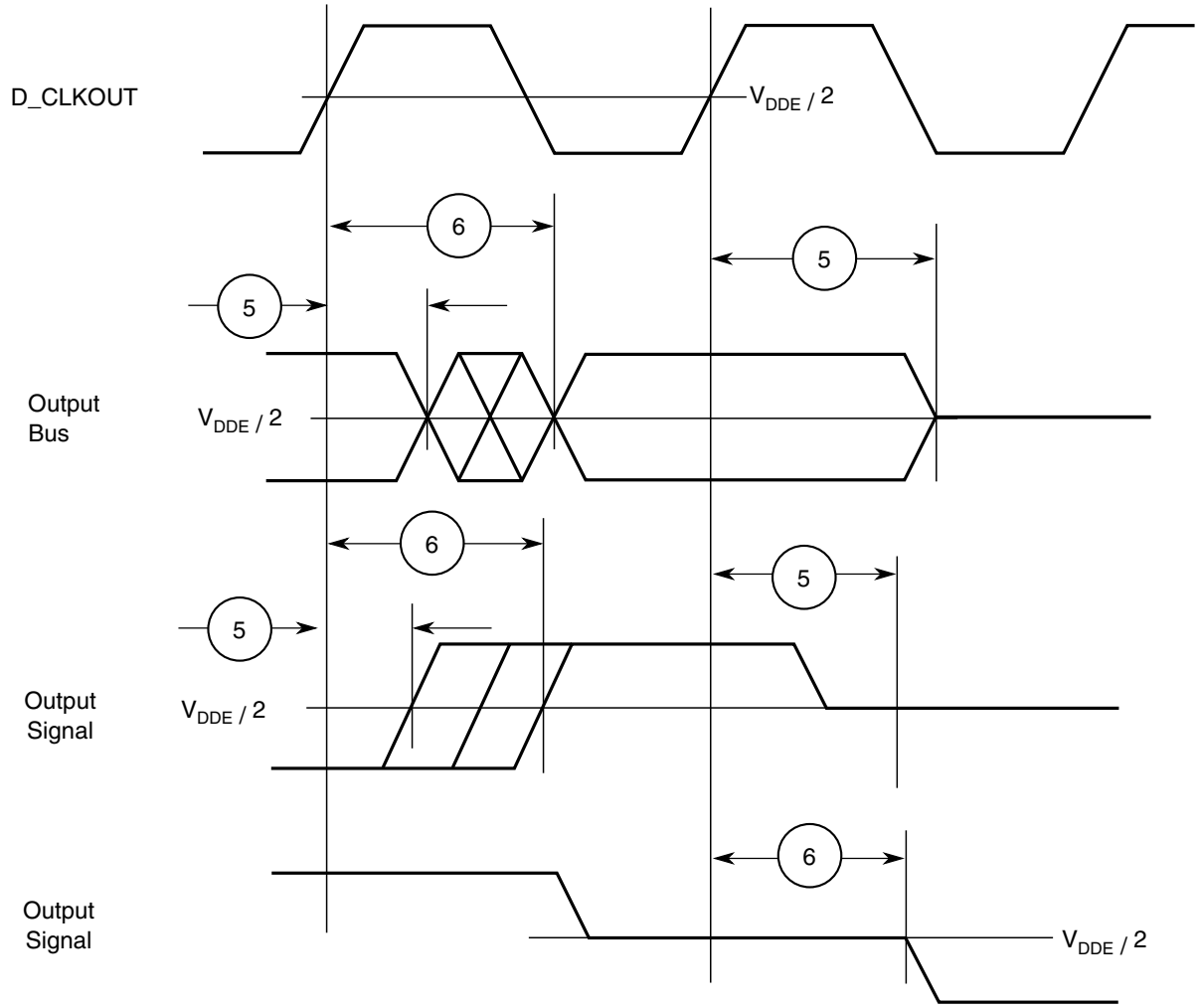


Figure 26. Synchronous output timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK}$ – 5	$1/2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	50 pF	31 – ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	50 pF	62 – ($P^{11} \times t_{SYS}$, 6)	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							

Table continues on the next page...

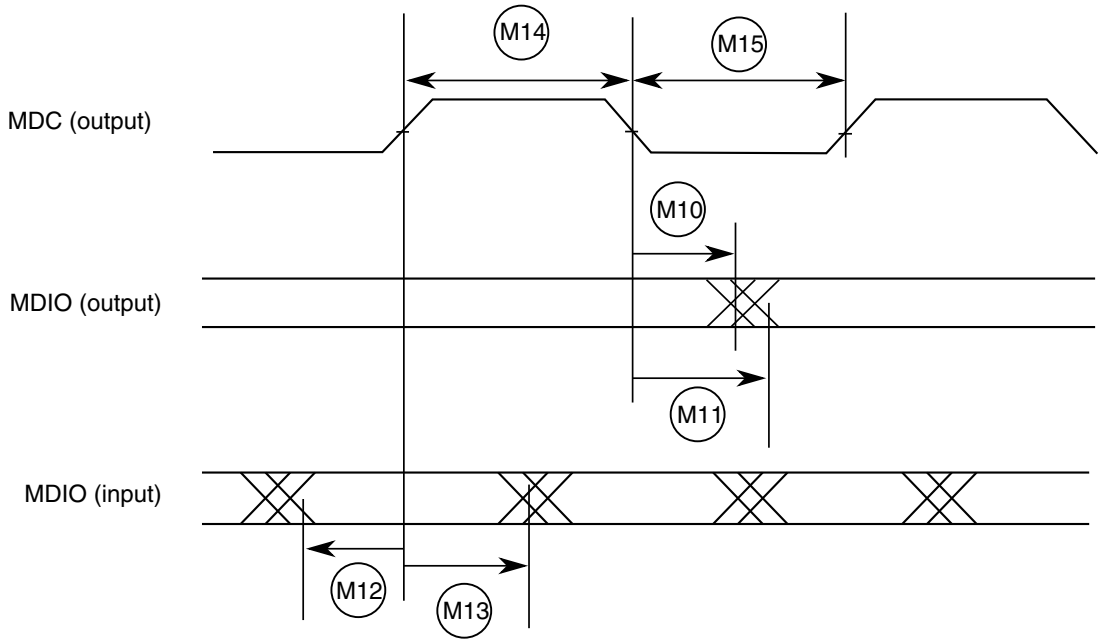


Figure 44. MII serial management channel timing diagram

3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 52. RMII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Table 56. Orderable part numbers

Part number[1]	Package description	Speed (MHz)[2]	Operating temperature[3]	
			Min (T_L)	Max (T_H)
SPC5777CK2MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK2MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 57. Revision history

Revision	Date	Description of changes
9	06/2016	For I_{MAXSEG} in Table 1 of Absolute maximum ratings • Changed Parameter description from "Maximum DC current per power segment" to "Maximum current per I/O power segment" • Added two footnotes In Electromagnetic interference (EMI) characteristics removed references to Freescale In Table 3 of Operating conditions • In third-to-last row, changed "Injection current" to "Current" • Added I_{MAXSEG} specification In Table 6 of Input pad specifications • For I_{LKG} and I_{LKG_FAST}, added Condition: $V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}$ • For I_{LKGA}, added Condition: $V_{SSA\_SD} < V_{IN} < V_{DDA\_SD}$, $V_{SSA\_EQ} < V_{IN} < V_{DDA\_EQA/B}$

Table continues on the next page...

Table 57. Revision history (continued)

Revision	Date	Description of changes

9 (continued)	06/2016	In I/O pad current specifications
		• Removed sentence: "Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table. The sum of all pad usage ratio within a segment should remain below 100%."
		• Added sentence: "To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1."
		• Added sentence: "To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3."
		
		In Table 18 of Sigma-Delta ADC (SDADC)
		• Removed Z_{IN} specification
		• Added Z_{DIFF}, Z_{CM}, and ΔV_{INTCM} specifications
		• For R_{BIAS}
		  • Changed Parameter description from "Bias resistance" to "Bare bias resistance"
		  • Changed Min from 100 kΩ to 110 kΩ
		  • Changed Typ from 125 kΩ to 144 kΩ
		  • Changed Max from 160 kΩ to 180 kΩ
		
		In Table 24 of LDO mode recommended power transistors
		• For I_{CMaxDC}: Changed Parameter description from "Minimum peak collector current" to "Maximum DC collector current"
		
		In Table 26 of SMPS mode recommended external components and characteristics
		• For part R (Resistor): Changed Nominal value range from 50–100 kΩ to 2.0-4.7 kΩ
		
		In Table 29 of Device voltage monitoring
		• For LVD_core_cold, falling voltage: Changed Min from 1145 mV to 1136 mV
		
		In Power sequencing requirements added new final requirement: "When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device."
		
		In Table 37 of Nexus timing
		• For existing specification 8, TCK Cycle Time (t_{TCYC}):
		  • Changed Min from $4 \times t_{CYC}$ to $2 \times t_{CYC}$
		  • Changed associated footnote from "Lower frequency is required to be fully compliant to standard" to "This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification."
		• Added another row (containing two sub-rows and associated footnotes) for specification 8, TCK Cycle Time (t_{TCYC}):
		  • Absolute minimum TCK cycle time (TDO sampled on posedge of TCK)
		  • Absolute minimum TCK cycle time (TDO sampled on negedge of TCK)
		• For specification 12, TCK Low to TDO Data Valid (t_{NTDOV}): Changed Max from 14 ns to 18 ns
		
		In Package information
		• Added sentence and table explaining how to download latest package drawings
		• Removed subsections: "416-ball package" and "516-ball package"
		
		In Table 55 of Thermal characteristics corrected numbering of footnotes and display of footnote references
		
		In Ordering information removed reference to Freescale

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