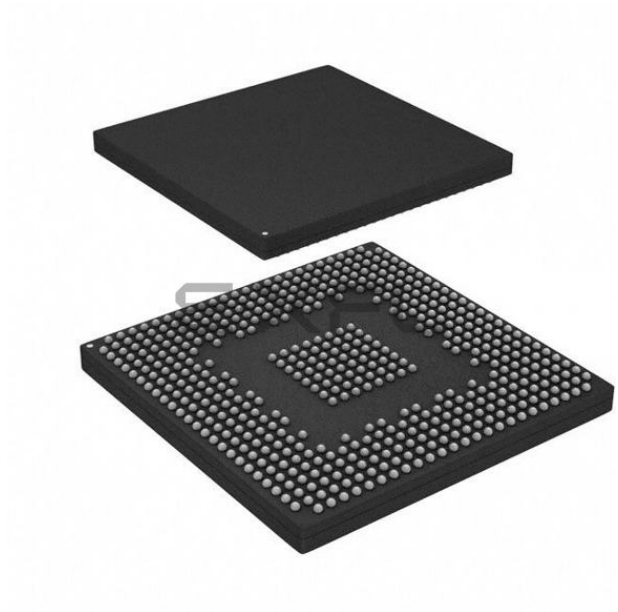

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck2mmo3

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[12]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[13]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[14, 15, 16]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[17, 18]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
4. Core voltage as measured on device pin to guarantee published silicon performance
5. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
6. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
7. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
8. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
9. This spec does not apply to V_{DDEH1}.
10. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.
11. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
12. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 5 shows output DC electrical characteristics.

2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

The following table shows the EBI CLKOUT, address, and control signal pad electrical characteristics. These pads can also be used for GPIO.

Table 10. GPIO and EBI CLKOUT, address, and control signal pad output buffer electrical characteristics (FC pads)

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications: valid for 3.0 V < V_{DDEx} < 3.6 V							
C_{DRV}	External bus load capacitance	PCR[DSC] = 01b		—	—	10	pF
		PCR[DSC] = 10b		—	—	20	
		PCR[DSC] = 11b		—	—	30	
f_{MAX_EBI}	External bus maximum operating frequency	C_{DRV} = 10/20/30 pF		—	—	66	MHz
GPIO and EBI Mode Output Specifications							
I_{OH_EBI}	GPIO and external bus pad output high current	V_{OH} = 0.8 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	30	—	—	mA
			PCR[DSC] = 10b	22	—	—	
			PCR[DSC] = 01b	13	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OH} = 0.8 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	16	—	—	
			PCR[DSC] = 10b	12	—	—	
			PCR[DSC] = 01b	7	—	—	
			PCR[DSC] = 00b	1	—	—	
I_{OL_EBI}	GPIO and external bus pad output low current	V_{OL} = 0.2 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	54	—	—	mA
			PCR[DSC] = 10b	25	—	—	
			PCR[DSC] = 01b	16	—	—	
			PCR[DSC] = 00b	2	—	—	
		V_{OL} = 0.2 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	17	—	—	
			PCR[DSC] = 10b	14	—	—	
			PCR[DSC] = 01b	8	—	—	
			PCR[DSC] = 00b	1	—	—	
$t_{R\_F\_EBI}$	GPIO and external bus pad output transition time (rise/fall)	PCR[DSC] = 11b	C_L = 30 pF	—	—	1.5	ns
			C_L = 50 pF	—	—	2.4	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	1.5	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	1.85	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	45	
t_{PD_EBI}	GPIO and external bus pad output propagation delay time	PCR[DSC] = 11b	C_L = 30 pF	—	—	4.2	ns
			C_L = 50 pF	—	—	5.5	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	4.2	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	4.4	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	59	

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	72	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	69	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	66	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	62	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 21. LFAST transmitter electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	110	200	285	mV
t_{TR}	Rise/fall time (10% – 90% of swing)[2,3]	—	0.26	—	1.5	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	12.0	pF
		V_{DDE} = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst-case internal capacitance values shown in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load CL.

Table 22. MSC/DSPI LVDS transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	Differential output voltage swing (terminated)[2,3]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing)[2,3]	—	0.8	—	4.0	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	50	pF
		V_{DDE} = 3.0 V	—	—	39	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst-case internal capacitance values given in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load C_L.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

Table 34. Flash memory read wait-state and address-pipeline control combinations (continued)

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
100 MHz < f_{PLATF} ≤ 133 MHz	3	1	6	1

3.13 AC timing

3.13.1 Generic timing diagrams

The generic timing diagrams in Figure 16 and Figure 17 apply to all I/O pins with pad types SR and FC. See the associated MPC5777C Microsoft Excel® file in the Reference Manual for the pad type for each pin.

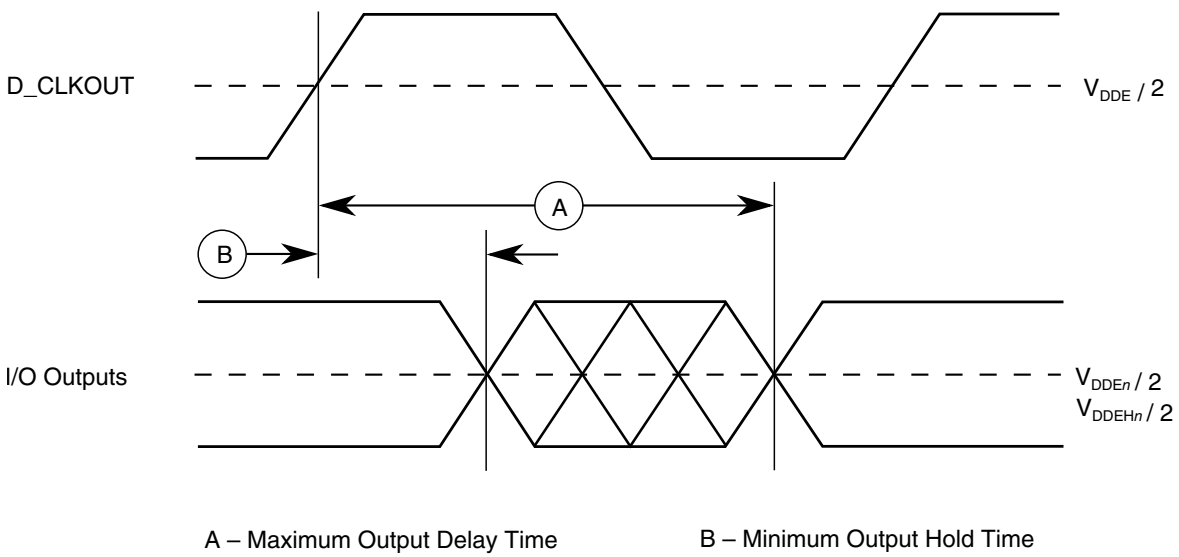

Figure 16. Generic output delay/hold timing

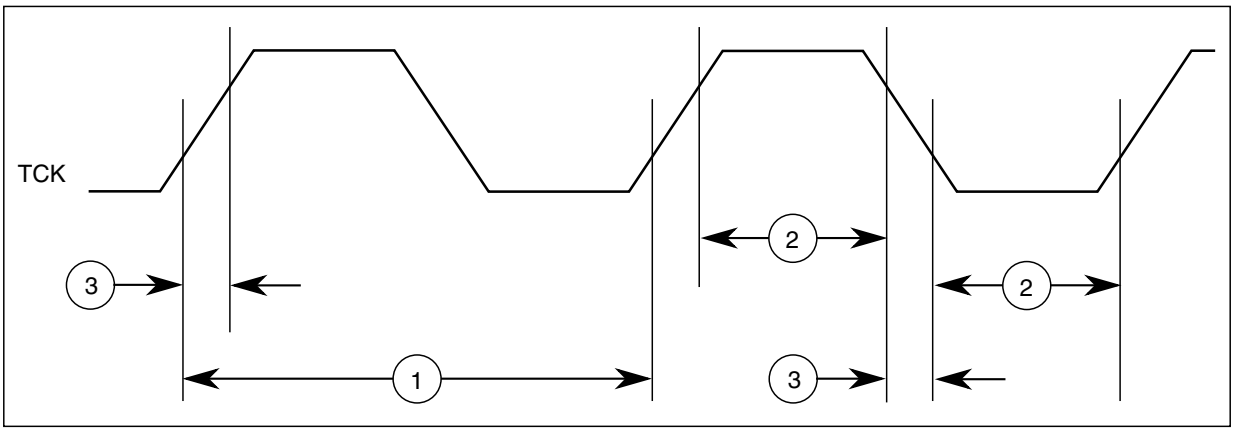

Figure 19. JTAG test clock input timing

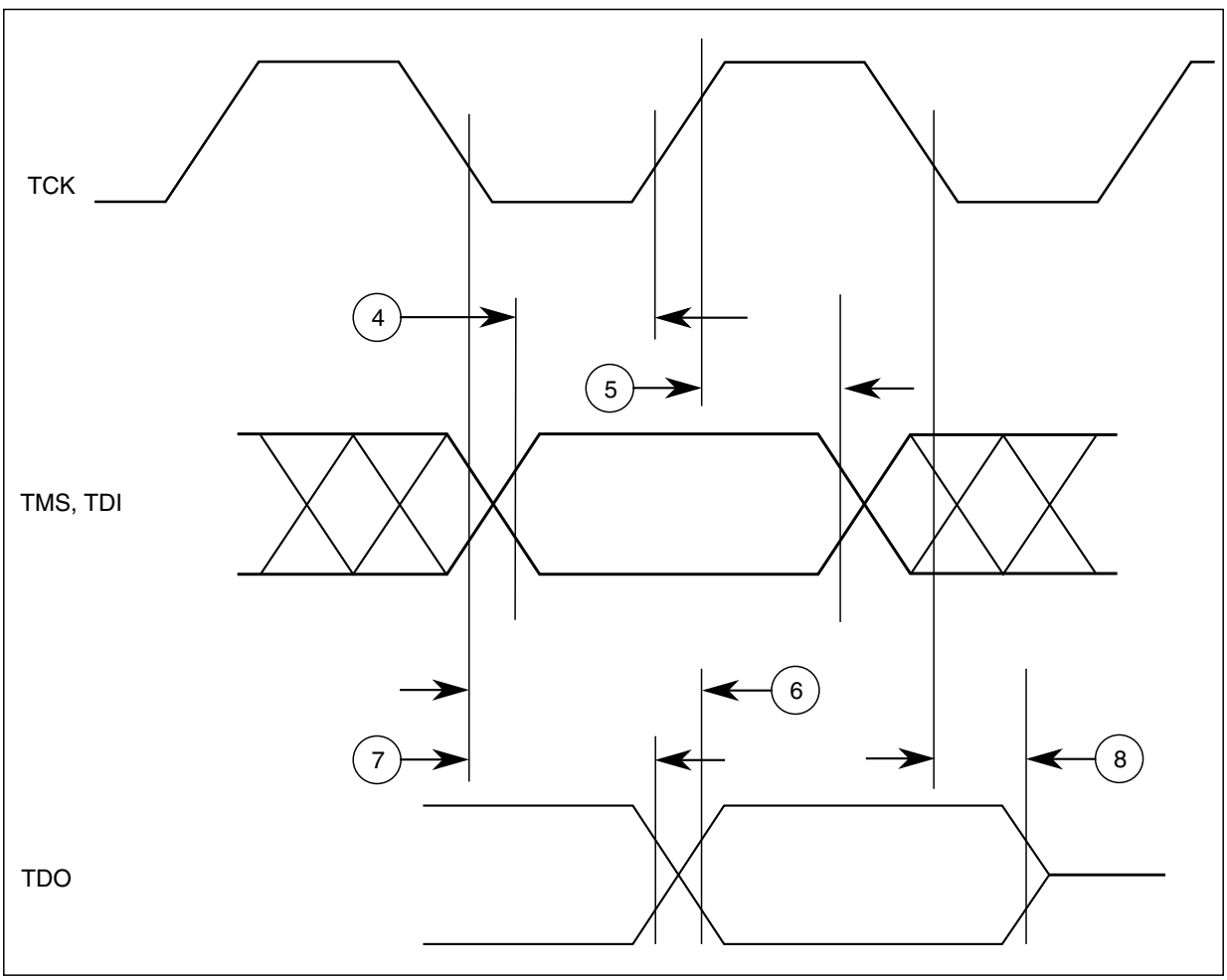

Figure 20. JTAG test access port timing

Table 37. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{RDY}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

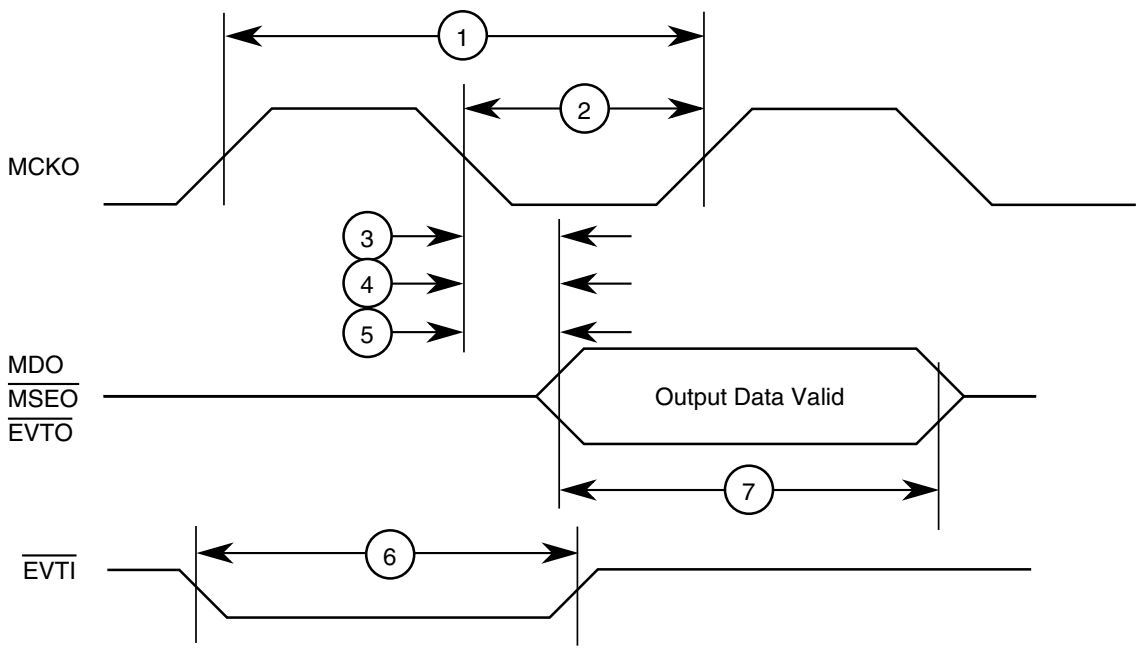

Figure 23. Nexus timings

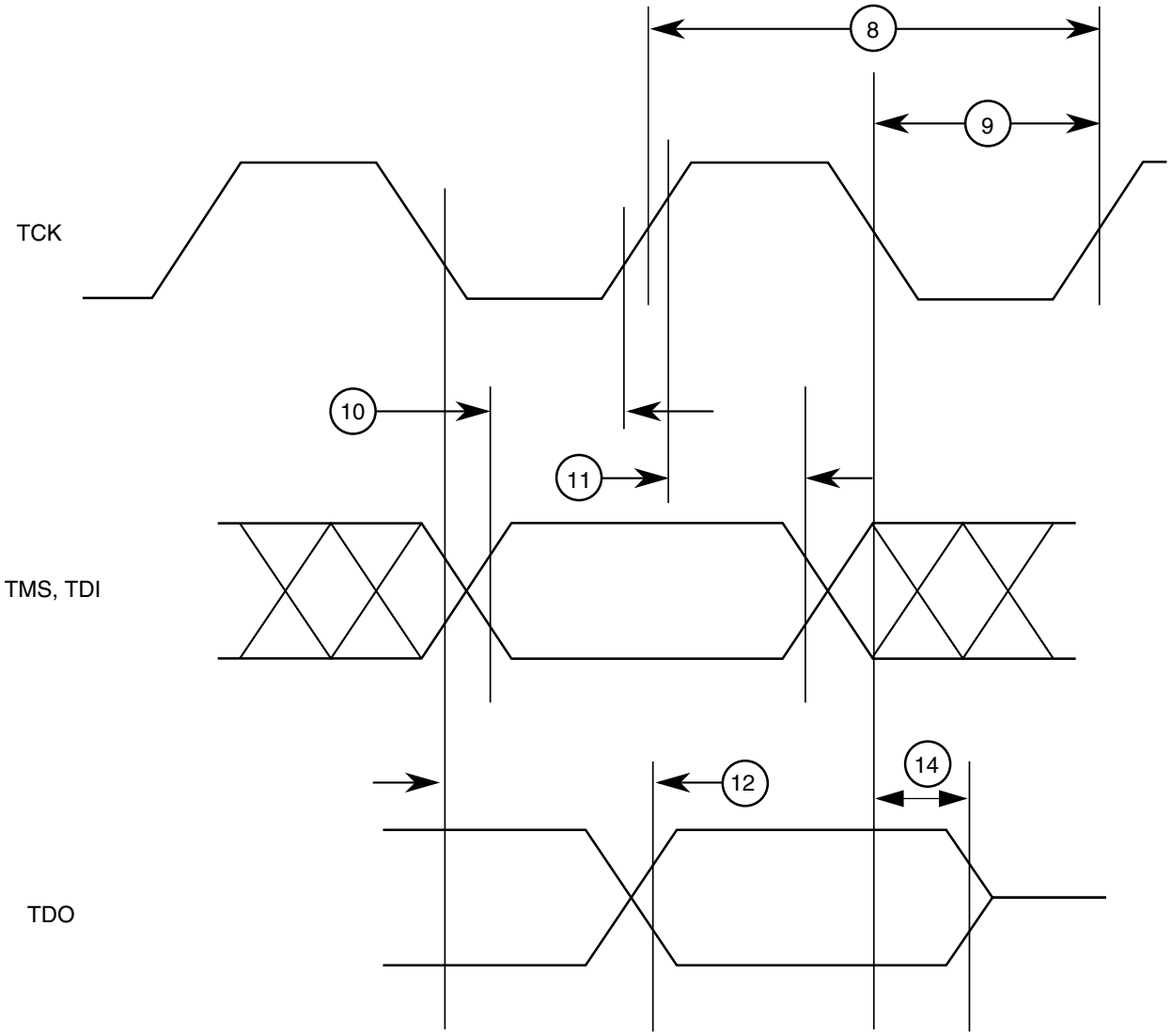

Figure 24. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External Bus Interface (EBI) timing

Table 38. Bus operation timing[1]

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	—
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	—
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	—

Table continues on the next page...

3.13.9 DSPI timing with CMOS and LVDS pads

NOTE

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 42. Timing specifications are shown in Table 43, Table 44, Table 45, Table 46, and Table 47.

Table 42. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1, 2]
CMOS (Master mode)	Full duplex – Classic timing (Table 43)	17
	Full duplex – Modified timing (Table 44)	30
	Output only mode (SCK/SOUT/PCS) (Table 43 and Table 44)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 47)	30
LVDS (Master mode)	Full duplex – Modified timing (Table 45)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 46)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.13.9.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.13.9.1.1 DSPI CMOS Master Mode — Classic Timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^5 \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^5 \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, [6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} – 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

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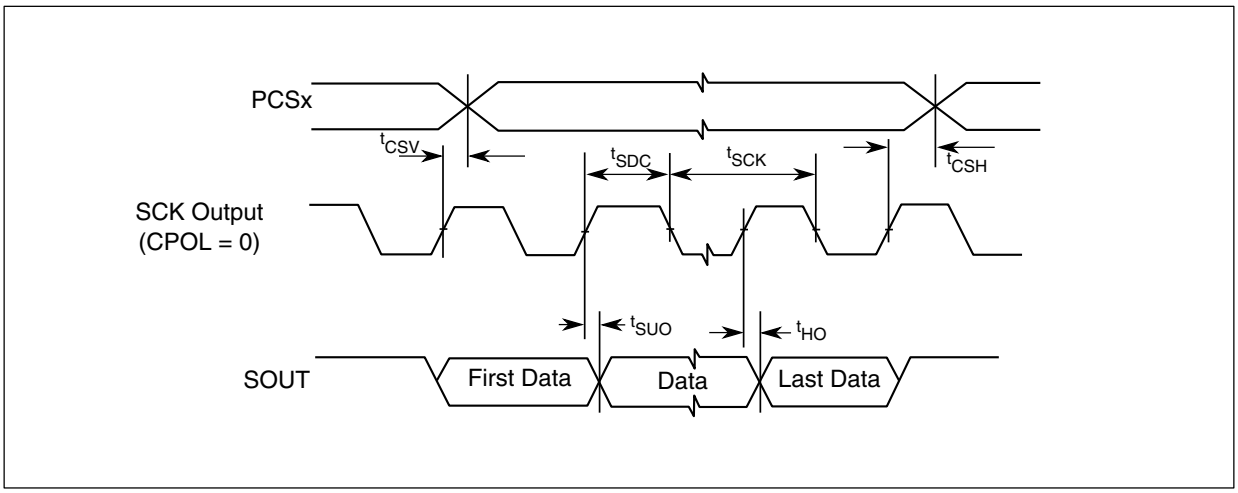

Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

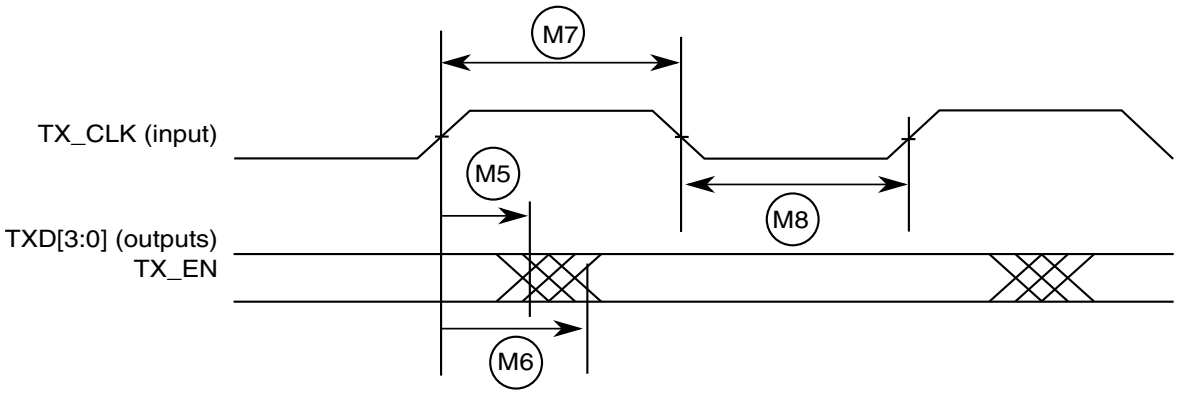

Figure 42. MII transmit signal timing diagram

3.13.10.3 MII async inputs signal timing (CRS)

Table 50. MII async inputs signal timing

Symbol	Characteristic	Value		Unit
		Min	Max	
M9	CRS minimum pulse width	1.5	—	TX_CLK period

Figure 43. MII async inputs timing diagram

3.13.10.4 MII and RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 51. MII serial management channel timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

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