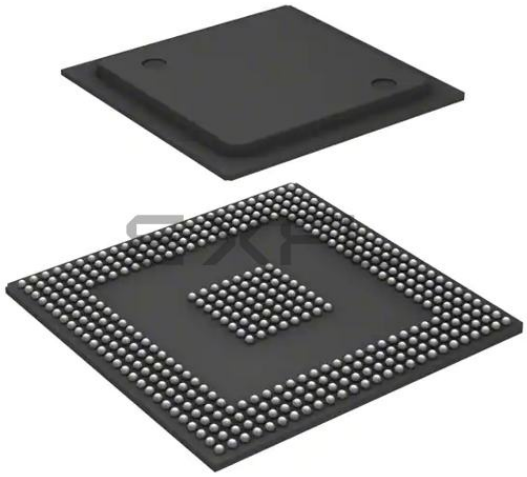

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck3mme3

1 Introduction

1.1 Features summary

On-chip modules available within the family include the following features:

- Three dual issue, 32-bit CPU core complexes (e200z7), two of which run in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - On the two computational cores: Signal processing extension (SPE1.1) instruction support for digital signal processing (DSP)
  - Single-precision floating point operations
  - On the two computational cores: 16 KB I-Cache and 16 KB D-Cache
  - Hardware cache coherency between cores
- 16 hardware semaphores
- 3-channel CRC module
- 8 MB on-chip flash memory
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 512 KB on-chip general-purpose SRAM including 64 KB standby RAM
- Two multichannel direct memory access controllers (eDMA)
  - 64 channels per eDMA
- Dual core Interrupt Controller (INTC)
- Dual phase-locked loops (PLLs) with stable clock domain for peripherals and frequency modulation (FM) domain for computational shell
- Crossbar Switch architecture for concurrent access to peripherals, flash memory, or RAM from multiple bus masters with End-To-End ECC
- External Bus Interface (EBI) for calibration and application use
- System Integration Unit (SIU)
- Error Injection Module (EIM) and Error Reporting Module (ERM)
- Four protected port output (PPO) pins
- Boot Assist Module (BAM) supports serial bootload via CAN or SCI
- Three second-generation Enhanced Time Processor Units (eTPUs)
  - 32 channels per eTPU
  - Total of 36 KB code RAM
  - Total of 9 KB parameter RAM

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
Cycle	Lifetime power cycles	—	—	1000k	—
V_{DD}	1.2 V core supply voltage[2, 3, 4]	—	–0.3	1.5	V
V_{DDEHx}	I/O supply voltage (medium I/O pads)[5]	—	–0.3	6.0	V
V_{DDEx}	I/O supply voltage (fast I/O pads)[5]	—	–0.3	6.0	V
V_{DDPMC}	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
V_{DDFLA}	Decoupling pin for flash regulator[6]	—	–0.3	4.5	V
V_{STBY}	RAM standby supply voltage[5]	—	–0.3	6.0	V
V_{SSA_SD}	SDADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
V_{SSA_EQ}	eQADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	Reference to V_{SSA_EQ}	–0.3	6.0	V
V_{DDA_SD}	SDADC supply voltage	Reference to V_{SSA_SD}	–0.3	6.0	V
V_{RL_SD}	SDADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RL_EQ}	eQADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RH_EQ}	eQADC alternate reference	Reference to V_{RL_EQ}	–0.3	6.0	V
V_{RH_SD}	SDADC alternate reference	Reference to V_{RL_SD}	–0.3	6.0	V
$V_{REFBYPC}$	eQADC reference decoupling capacitor pins	REFBYPCA25, REFBYPCA75, REFBYPCB25, REFBYPC75	–0.3	6.0	V
V_{DDA_MISC}	TRNG and IRC supply voltage	—	–0.3	6.0	V
V_{DDPWR}	SMPS driver supply pin	—	–0.3	6.0	V
V_{SSPWR}	SMPS driver supply pin	Reference to V_{SS}	–0.3	0.3	V
$V_{SS} – V_{SSA\_EQ}$	V_{SSA_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SSA\_SD}$	V_{SSA_SD} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–0.3	0.3	V
V_{IN}	I/O input voltage range[7]	—	–0.3	6.0	V
		Relative to V_{DDEx}/V_{DDEHx}	—	0.3	V
		Relative to V_{SS}	–0.3	—	V
I_{INJD}	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[8, 9]	Maximum current per I/O power segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	Maximum solder temperature[10] Pb-free package	—	—	260	°C

Table continues on the next page...

13. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
14. Full device lifetime without performance degradation
15. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
16. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
17. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
18. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

3.5 DC electrical specifications

NOTE

I_{DDA_MISC} is the sum of current consumption of IRC, I_{TRNG}, and I_{STBY} in the 5 V domain. IRC current is provided in the IRC specifications.

NOTE

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

Table 4. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD}	Operating current on the V_{DD} core logic supply[1]	LVD/HVD enabled, V_{DD} = 1.2 V to 1.32 V	—	0.65	1.35	A
		LVD/HVD disabled, V_{DD} = 1.2 V to 1.38 V	—	0.65	1.4	
I_{DD_PE}	Operating current on the V_{DD} supply for flash memory program/erase	—	—	—	85	mA
I_{DDPMC}	Operating current on the V_{DDPMC} supply[2]	Flash memory read	—	—	40	mA
		Flash memory program/erase	—	—	70	
		PMC only	—	—	35	
	Operating current on the V_{DDPMC} supply (internal core regulator bypassed)	Flash memory read	—	—	10	mA
		Flash memory program/erase	—	—	40	
		PMC only	—	—	5	
I_{REGCTL}	Core regulator DC current output on V_{REGCTL} pin	—	—	—	25	mA
I_{STBY}	Standby RAM supply current (T_J = 150°C)	1.08 V	—	—	1140	µA
		1.25 V to 5.5 V	—	—	1170	
I_{DD_PWR}	Operating current on the V_{DDPWR} supply	—	—	—	50	mA
I_{BG_REF}	Bandgap reference current consumption[3]		—	—	600	µA
I_{TRNG}	True Random Number Generator current	—	—	—	2.1	mA

Table 14. External oscillator (XOSC) electrical specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

1. This value is determined by the crystal manufacturer and board design.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
4. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating in a "low" transconductance range. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating in a "medium" or "high" transconductance range, the integrated load capacitor value is selected via software to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
5. Select a "low," "medium," or "high" setting using the UTEST Miscellaneous DCF client's XOSC_LF_EN and XOSC_EN_HIGH fields. "Low" is the setting commonly used for crystals at 8 MHz, "medium" is commonly used for crystals greater than 8 MHz to 20 MHz, and "high" is commonly used for crystals greater than 20 MHz to 40 MHz. However, the user must characterize carefully to determine the best g_m setting for the intended application because crystal load capacitance, board layout, and other factors affect the g_m value that is needed. The user may need an additional Rshunt to optimize g_m depending on the system environment. Use of overtone crystals is not recommended.
6. Amplitude on the EXTAL pin after startup is determined by the ALC block (that is, the Automatic Level Control Circuit). The function of the ALC is to provide high drive current during oscillator startup, while reducing current after oscillation to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
7. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 7.

Table 15. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
00000	1.8
00001	2.8
00010	3.7
00011	4.6
00100	5.6
00101	6.5
00110	7.4
00111	8.4
01000	9.3
01001	10.2
01010	11.2
01011	12.1
01100	13.0
01101	13.9

Table continues on the next page...

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	80	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	77	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	74	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	71	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	71	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	70	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	68	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	65	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	62	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF333}$	Signal to noise and distortion ratio in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	59	—	—	
$SINAD_{SE150}$	Signal to noise and distortion ratio in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	54	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

3.10.1 LFAST interface timing diagrams

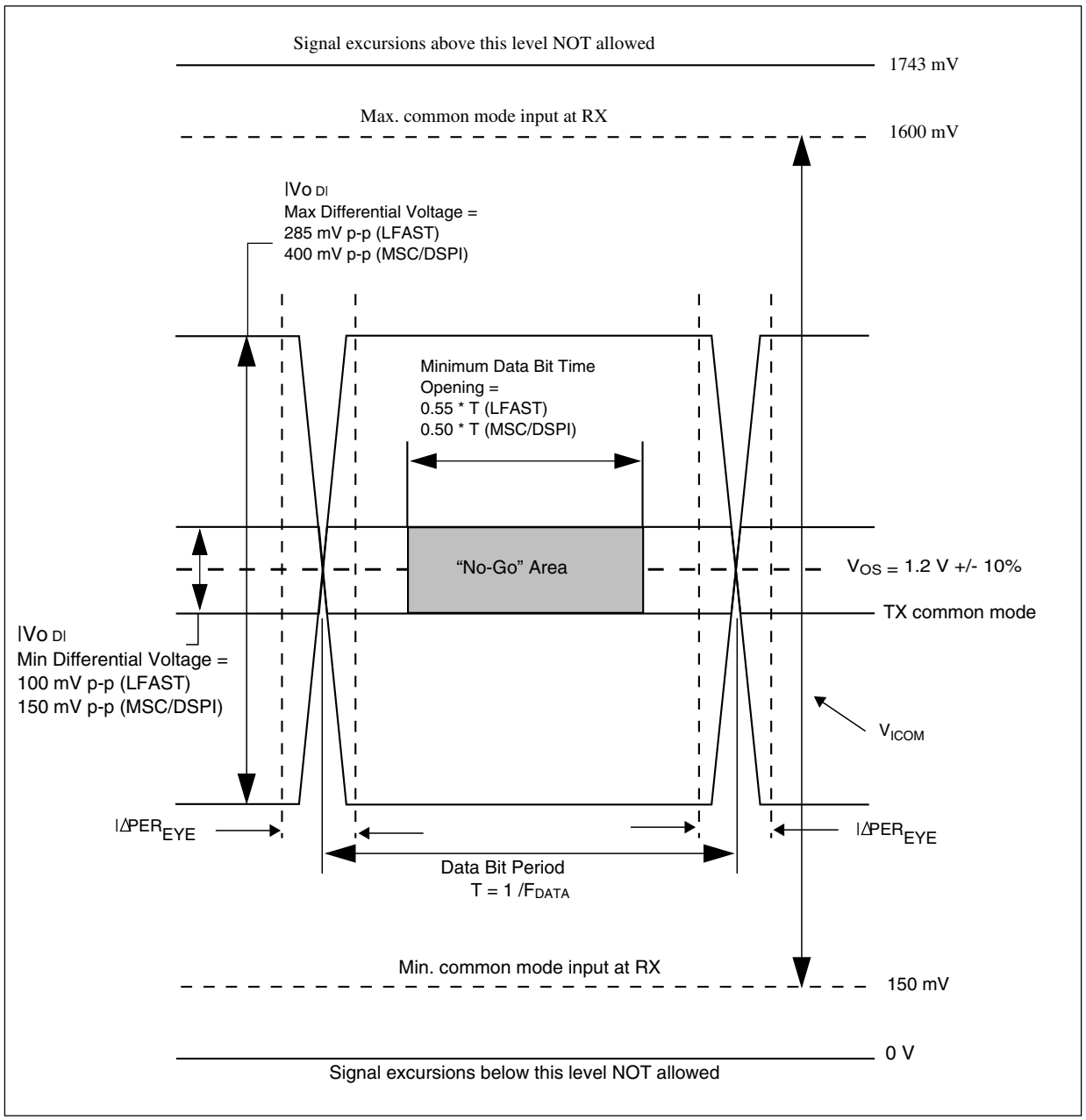


Figure 8. LFAST and MSC/DSPI LVDS timing definition

The following table shows the recommended components to be used in LDO regulation mode.

Table 25. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	NPN BJT	h_{FE} = 400	NJD2873: ON Semiconductor LDO voltage regulator controller (VRC)
CI	Capacitor	4.7 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.047–0.049 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to NPN collector)
CB	Capacitor	0.1 µF - 7 V	Ceramic V_{DDPWR}
R	Resistor	Application specific	Optional; reduces thermal loading on the NPN with high V_{DDPMC} levels

The following diagram shows the LDO configuration connection.

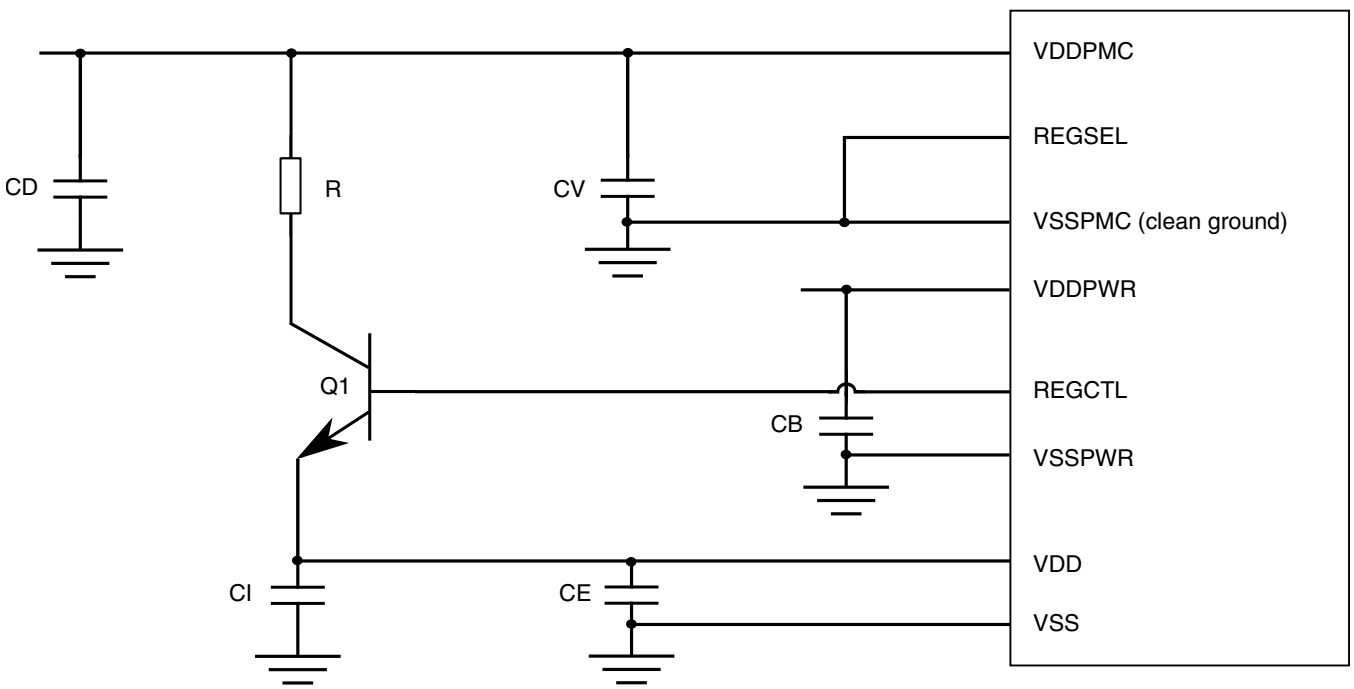


Figure 12. VRC 1.2 V LDO configuration

3.11.1.2 SMPS mode recommended external components and characteristics

The following table shows the recommended components to be used in SMPS regulation mode.

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

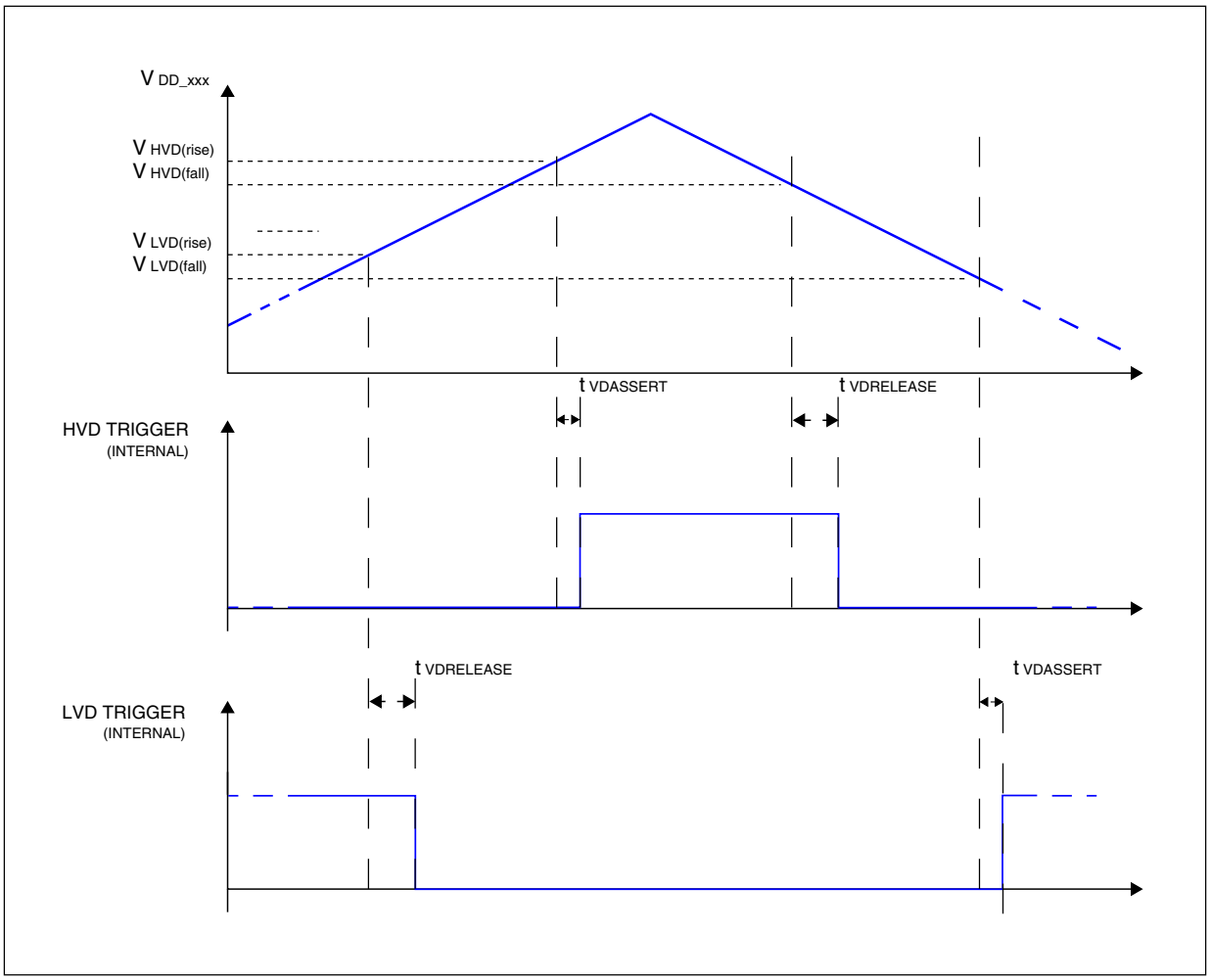


Figure 15. Voltage monitor threshold definition

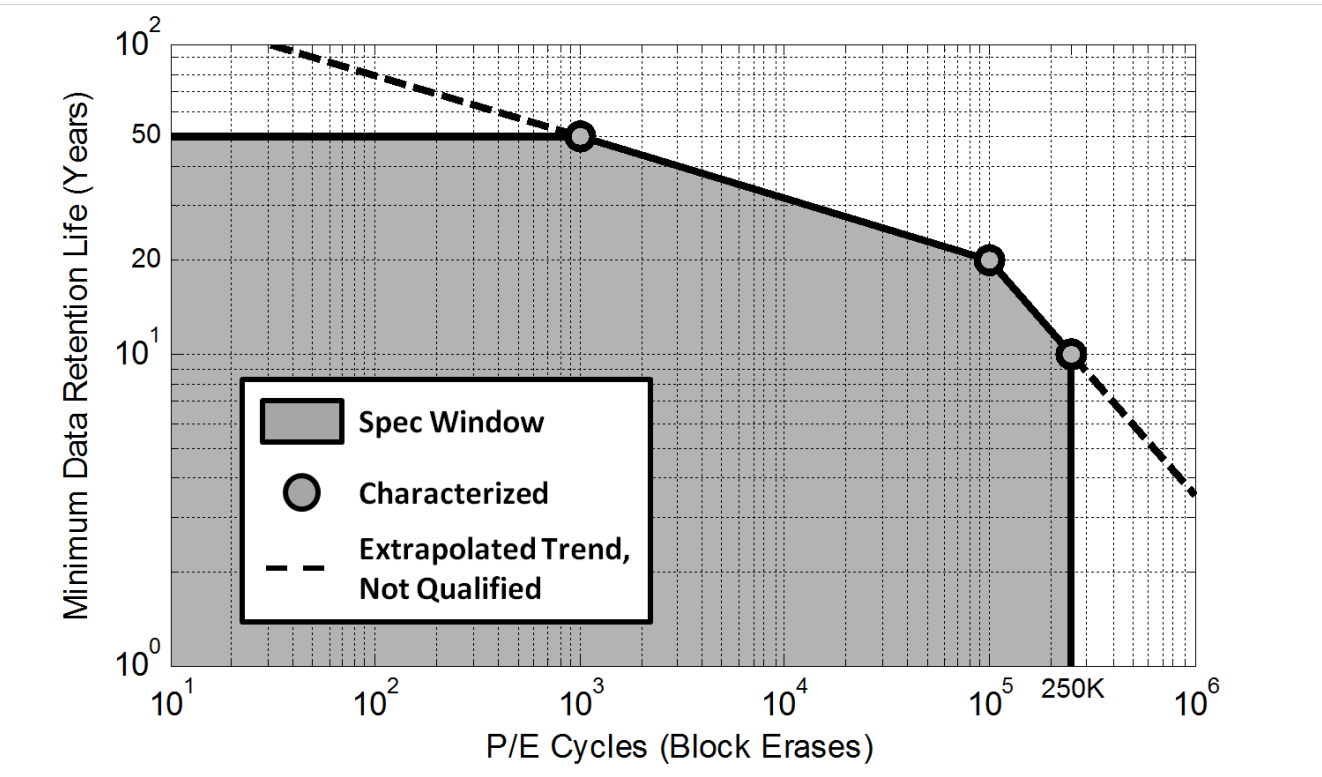
Table 29. Voltage monitor electrical characteristics[1, 2]

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR098_c[3]	LV internal supply power on reset	Rising voltage (powerup)	N/A	No	Enab.	960	1010	1060	mV
		Falling voltage (power down)				940	990	1040	
LVD_core_hot	LV internal[4] supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	1100	1140	1183	mV
		Falling voltage (untrimmed)				1080	1120	1163	
		Rising voltage (trimmed)				1142	1165	1183	
		Falling voltage (trimmed)				1122	1145	1163	
LVD_core_cold	LV external[5] supply low voltage monitoring	Rising voltage	4bit	Yes	Disab.	1165	1180	1198	mV
		Falling voltage				1136	1160	1178	
HVD_core	LV internal cold supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	1338	1365	1385	mV
		Falling voltage				1318	1345	1365	

Table continues on the next page...

3.12.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.12.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns

Table continues on the next page...

Table 37. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{RDY}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

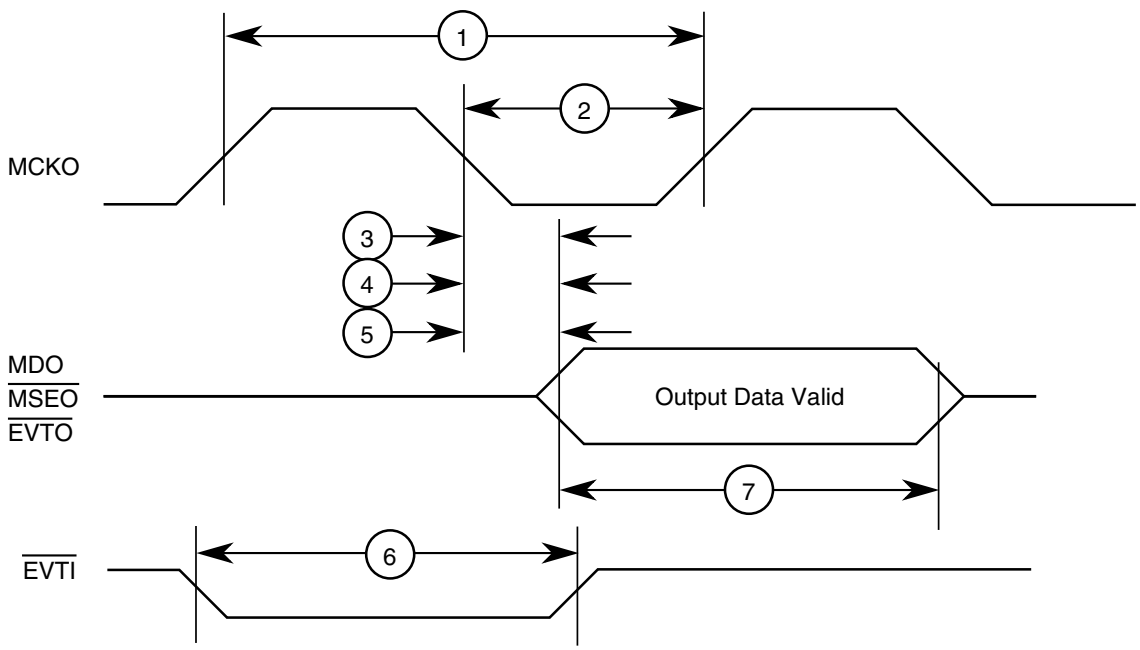


Figure 23. Nexus timings

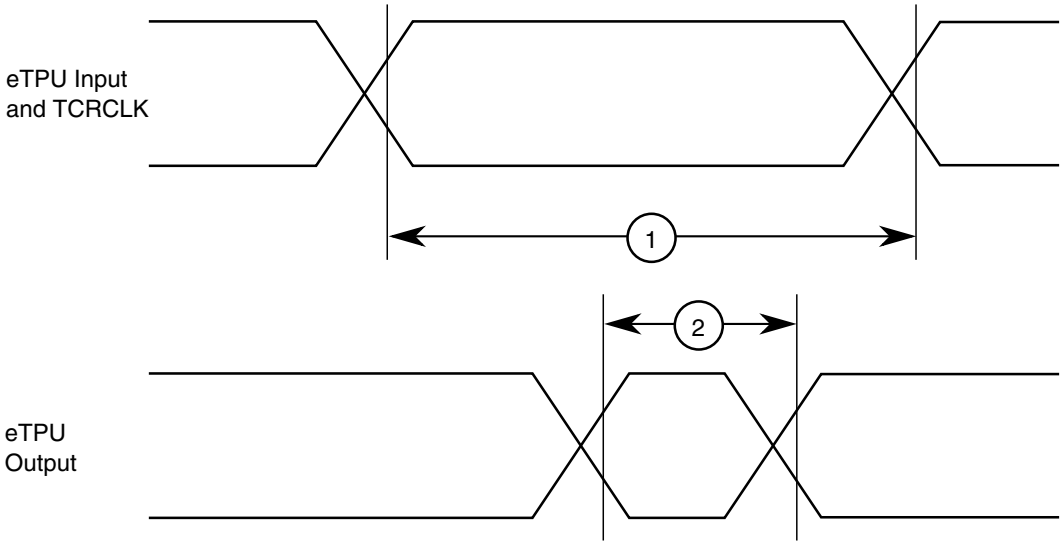


Figure 30. eTPU timing

3.13.8 eMIOS timing

Table 41. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

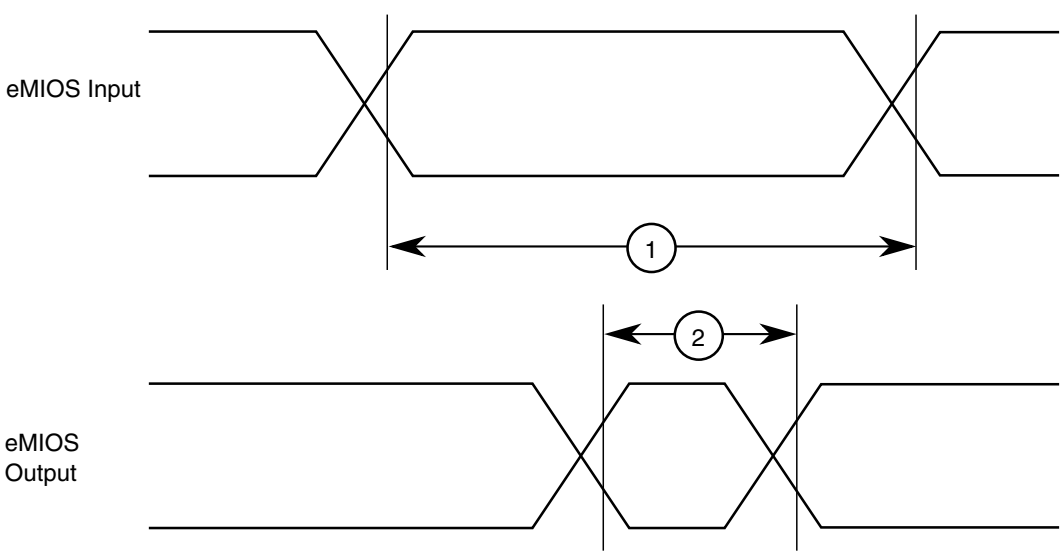


Figure 31. eMIOS timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	($M^7 \times t_{SYS}$, 6) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK}$ – 2	$1/2t_{SCK}$ + 2	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK}$ – 5	$1/2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	50 pF	31 – ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	50 pF	62 – ($P^{11} \times t_{SYS}$, 6)	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	ns
			PCR[SRC]=10b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
			PCR[SRC]=01b	0 pF	–1 + ($P^{11} \times t_{SYS}$, 6)	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							

Table continues on the next page...

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} – 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

Table continues on the next page...

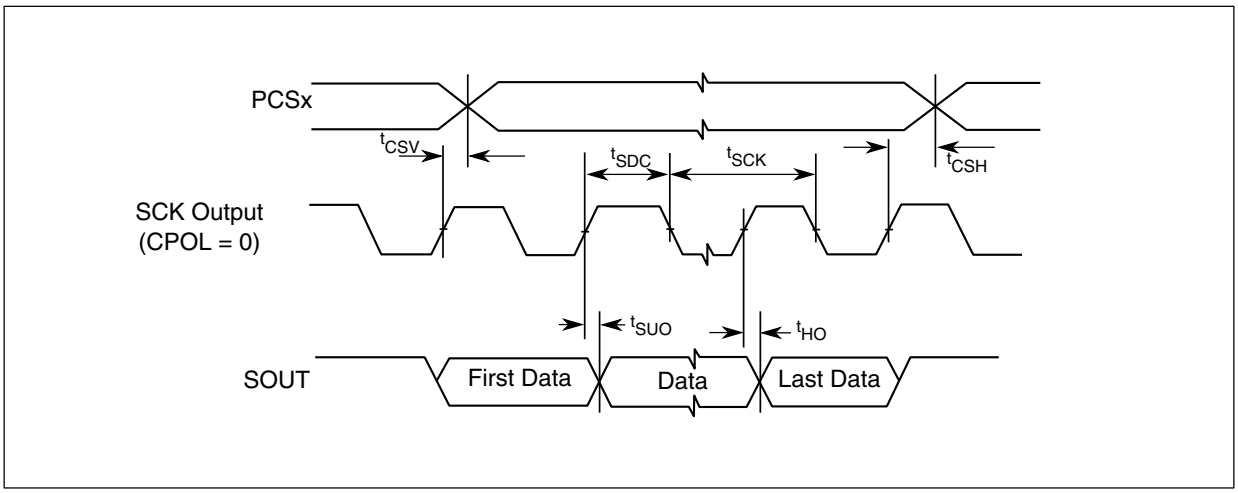


Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

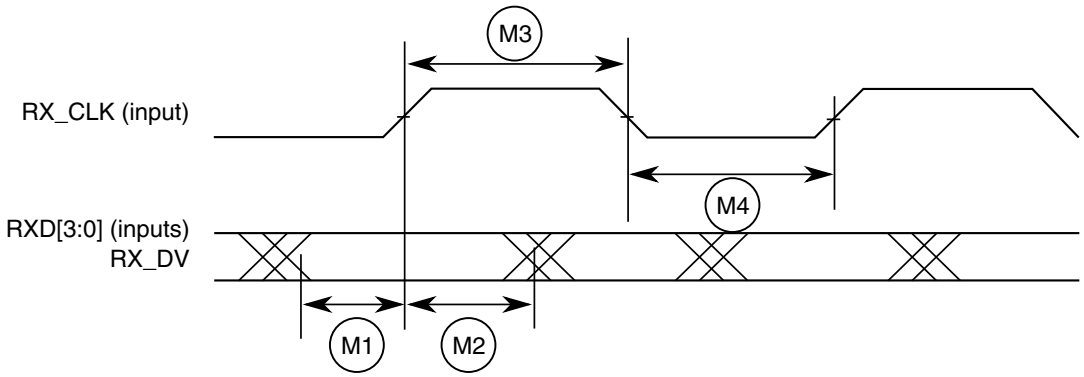


Figure 41. MII receive signal timing diagram

3.13.10.2 MII transmit signal timing (TXD[3:0], TX_EN, and TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of noncompliant MII PHYs.

Refer to the *MPC5777C Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 49. MII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN invalid	4.5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

Table 56. Orderable part numbers

Part number[1]	Package description	Speed (MHz)[2]	Operating temperature[3]	
			Min (T_L)	Max (T_H)
SPC5777CK2MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK2MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 57. Revision history

Revision	Date	Description of changes
9	06/2016	For I_{MAXSEG} in Table 1 of Absolute maximum ratings • Changed Parameter description from "Maximum DC current per power segment" to "Maximum current per I/O power segment" • Added two footnotes In Electromagnetic interference (EMI) characteristics removed references to Freescale In Table 3 of Operating conditions • In third-to-last row, changed "Injection current" to "Current" • Added I_{MAXSEG} specification In Table 6 of Input pad specifications • For I_{LKG} and I_{LKG_FAST}, added Condition: $V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}$ • For I_{LKGA}, added Condition: $V_{SSA\_SD} < V_{IN} < V_{DDA\_SD}$, $V_{SSA\_EQ} < V_{IN} < V_{DDA\_EQA/B}$

Table continues on the next page...