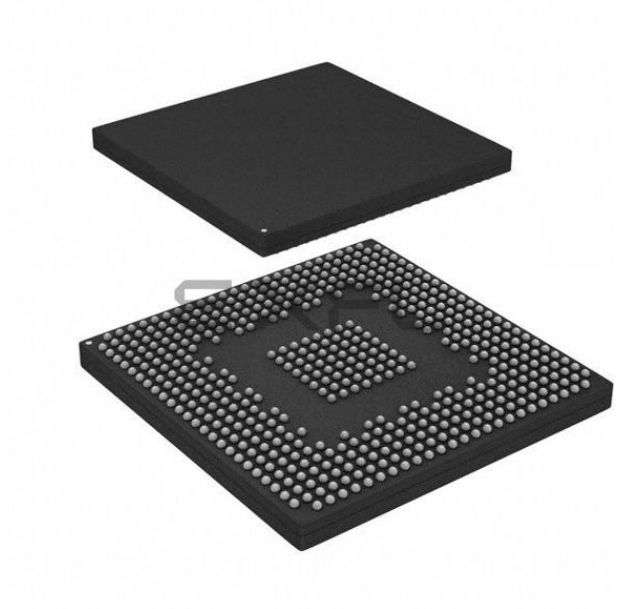

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16b Sigma-Delta, eQADC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777ck3mmo3

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads
EBI pads	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[1]	10	—	µs
—	Resolution[2]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[3]	–4	4	LSB[4]
	INL: 33 MHz eQADC clock[3]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[3]	–3	3	LSB
	DNL: 33 MHz eQADC clock[3]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[5, 6, 7, 8]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[9, 10]	—	+4	Counts
TUE	TUE value[11, 12] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[13]	-	-	Counts[15]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[14]	3[14]	
	DNL, 33 MHz ADC	–3[14]	3[14]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[13]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.
2. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
3. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
4. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
GAIN	ADC gain	Defined through SDADC_MCR[PGAN]. Only integer powers of 2 are valid gain values.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$	Absolute value of the ADC gain error[6, 7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	Conversion offset[6, 7]	Before calibration (applies to all gain settings: 1, 2, 4, 8, 16)	—	10*(1+1/gain)	20	mV
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 1	72	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 2	69	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 4	66	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 8	62	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] V_{RH_SD} = V_{DDA_SD} GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be “clipped.”
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5*V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range 3.6 V < V_{DDA_SD} < 4.0 V: SNR parameter degrades by 3 dB. SDADC is functional in the range 3.0 V < V_{RH_SD} < 4.0 V: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} – f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of (V_{RH_SD} - V_{RL_SD}) / 2.
14. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

Table 20. LVDS pad startup and receiver electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to Normal mode)[5]	—	—	0.4	2.75	µs
t_{SM2NM_TX}	Transmitter startup time (Sleep mode to Normal mode)[6]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	Receiver startup time (power down to Normal mode)[7]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to Sleep mode)[8]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[9]	—	1.6[10]	V
$\|\Delta VI\|$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	V_{DDEH} = 3.0 V to 5.5 V	80	125	150	Ω
C_{IN}	Differential input capacitance[11]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules.
3. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
4. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
5. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
6. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
7. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
8. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
9. Absolute min = 0.15 V – (285 mV/2) = 0 V
10. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
11. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in Figure 11.

Table 21. LFAST transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	240	Mbps

Table continues on the next page...

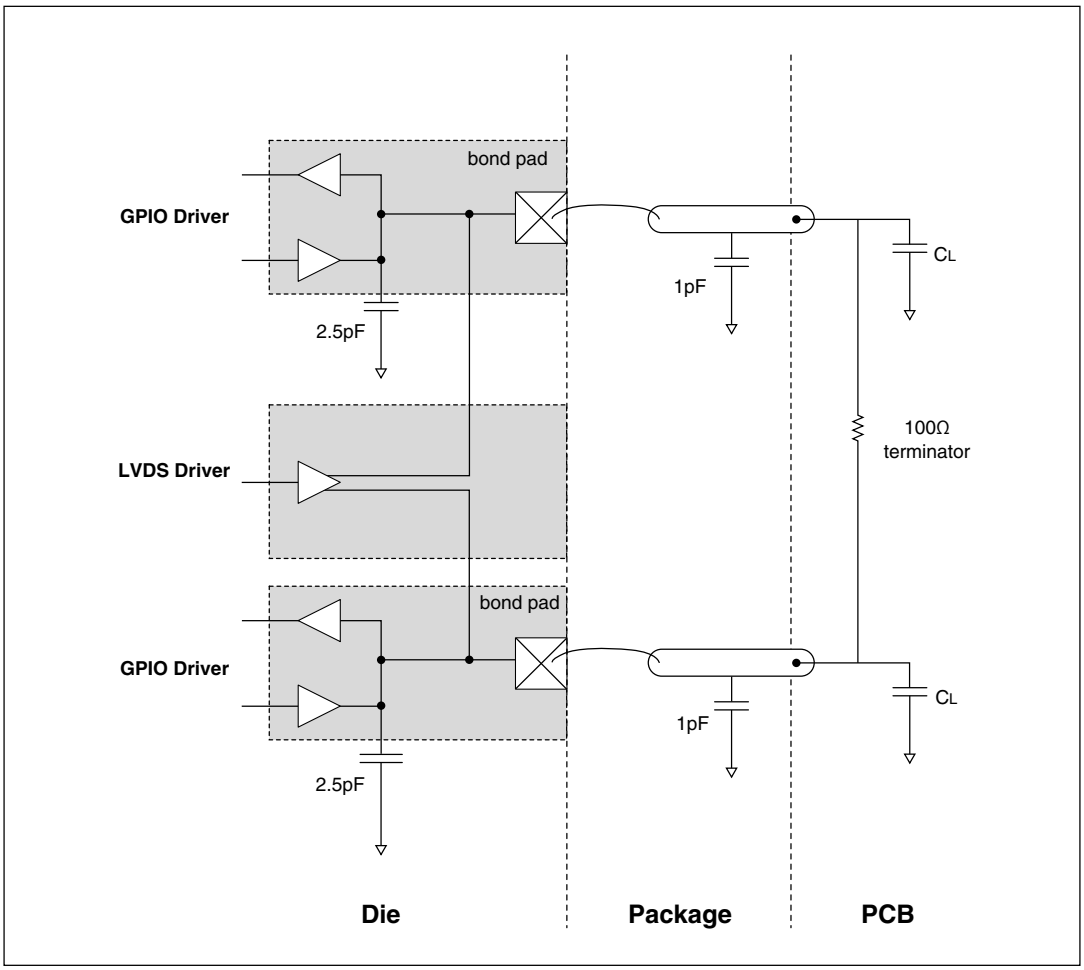

Figure 11. LVDS pad external load diagram

3.10.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 23. LFAST PLL electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
DC_{REF}	PLL reference clock duty cycle	—	45	—	55	%
PN	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
		f_{RF_REF} = 10 MHz	—	—	–64	
f_{VCO}	PLL VCO frequency	—	—	480[2]	—	MHz
t_{LOCK}	PLL phase lock[3]	—	—	—	40	µs

Table continues on the next page...

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

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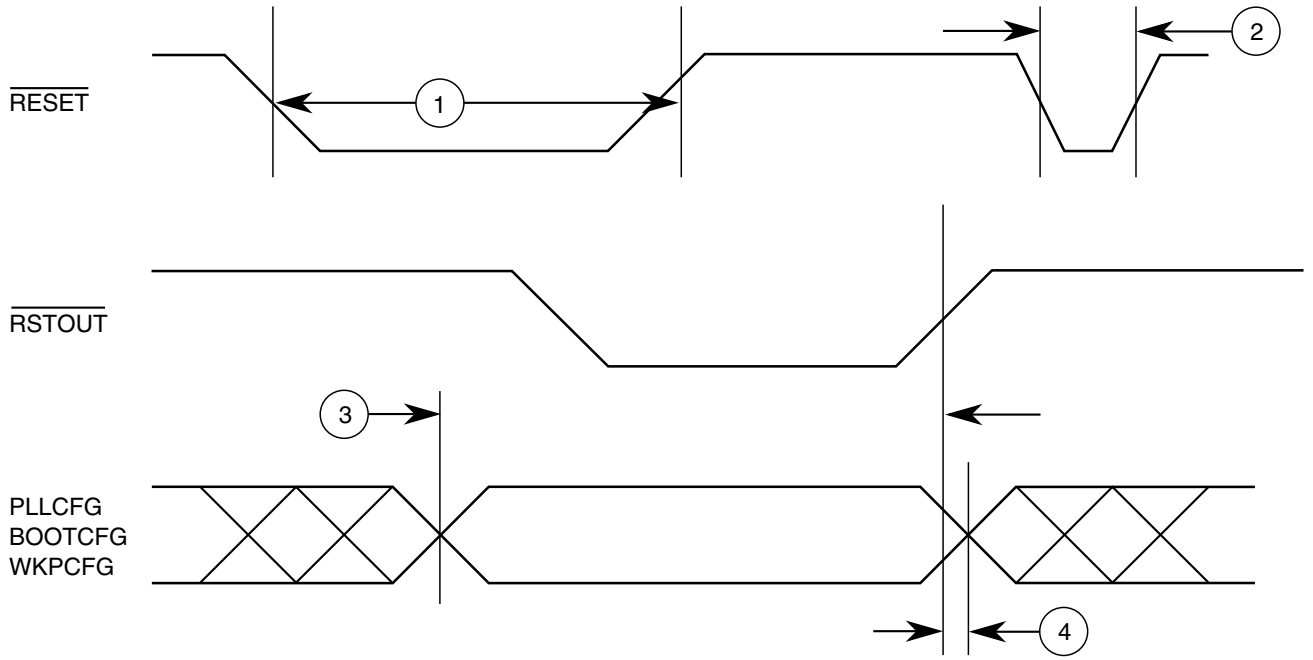

Figure 18. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

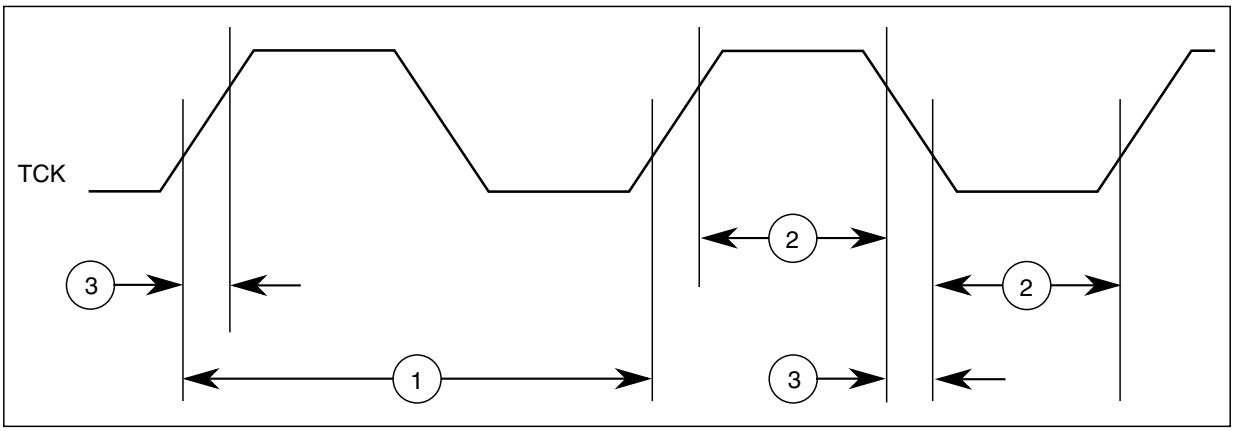

Figure 19. JTAG test clock input timing

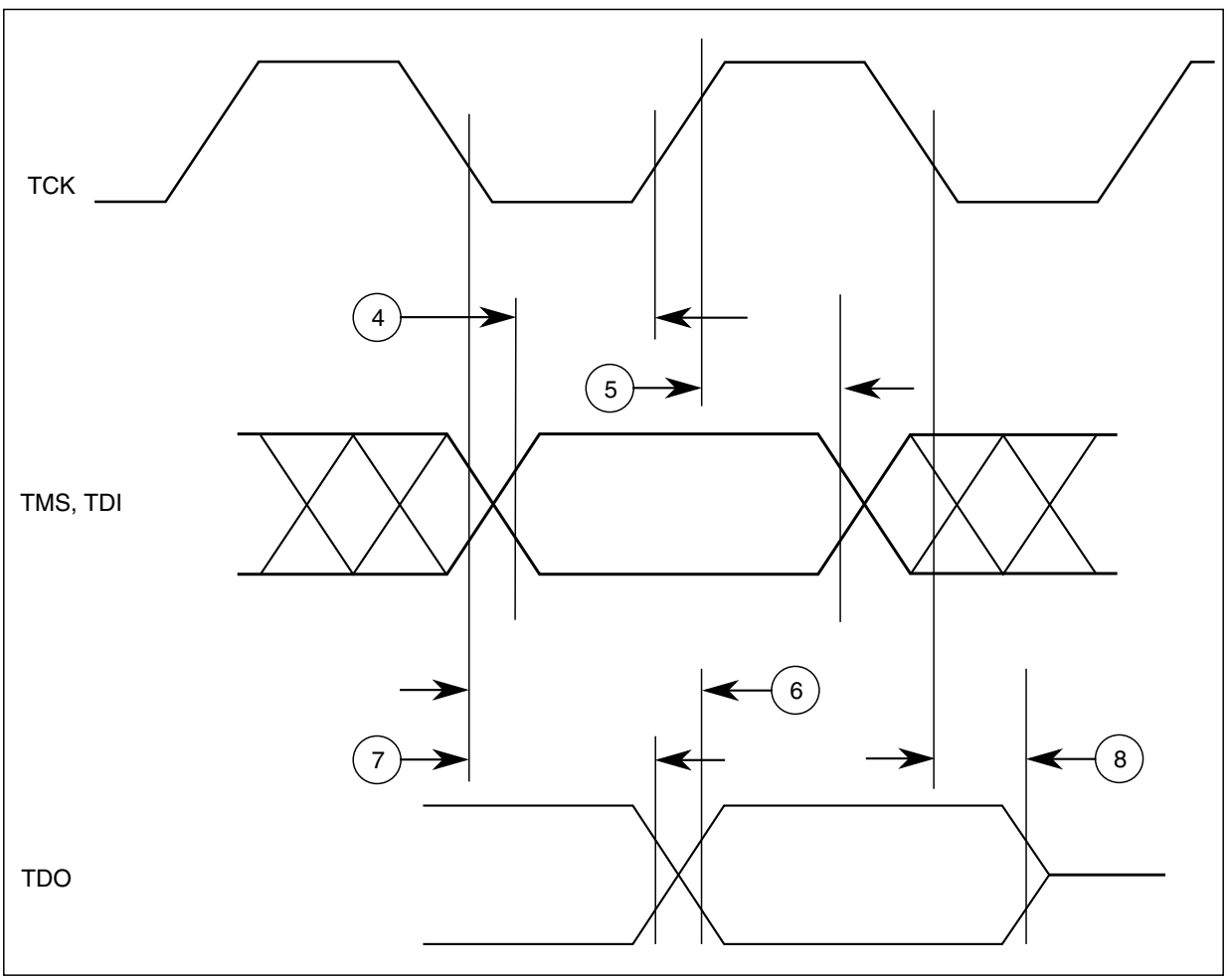

Figure 20. JTAG test access port timing

Table 38. Bus operation timing[1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1. EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SIU_PCR[DSC] = 10b for ADDR/CTRL and SIU_PCR[DSC] = 11b for CLKOUT/DATA.
2. Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM).
3. Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.
4. Refer to D_CLKOUT pad timing in Table 10.
5. ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0°C. 2.0ns spec applies to temperatures > 0°C. This spec has no dependency on the SIU_ECCR[EBTS] bit.

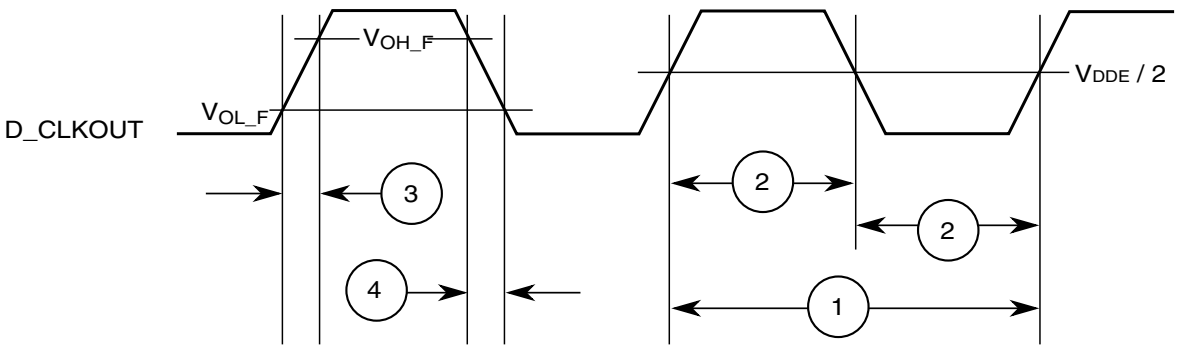

Figure 25. D_CLKOUT timing

3.13.6 External interrupt timing (IRQ/NMI pin)

Table 39. External Interrupt timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ/NMI Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ/NMI Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1. IRQ/NMI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H.
2. For further information on t_{cyc}, see Table 3.
3. Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

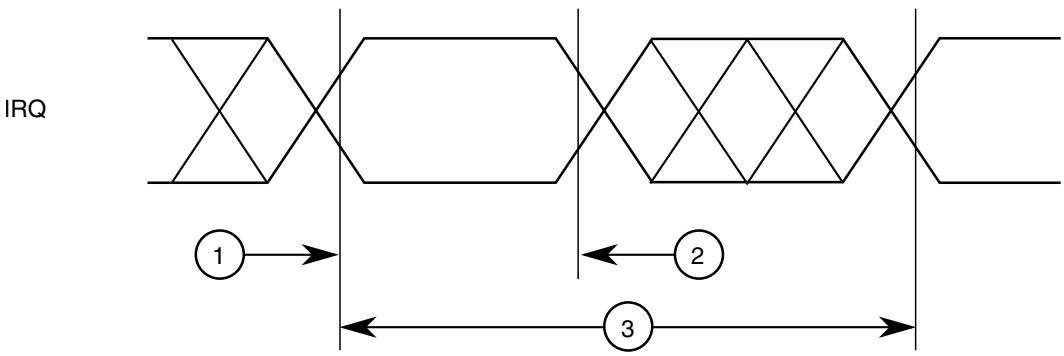

Figure 29. External interrupt timing

3.13.7 eTPU timing

Table 40. eTPU timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{CYC_ETPU}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{CYC_ETPU}[2]

1. eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. For further information on $_{tCYC\_ETPU}$, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

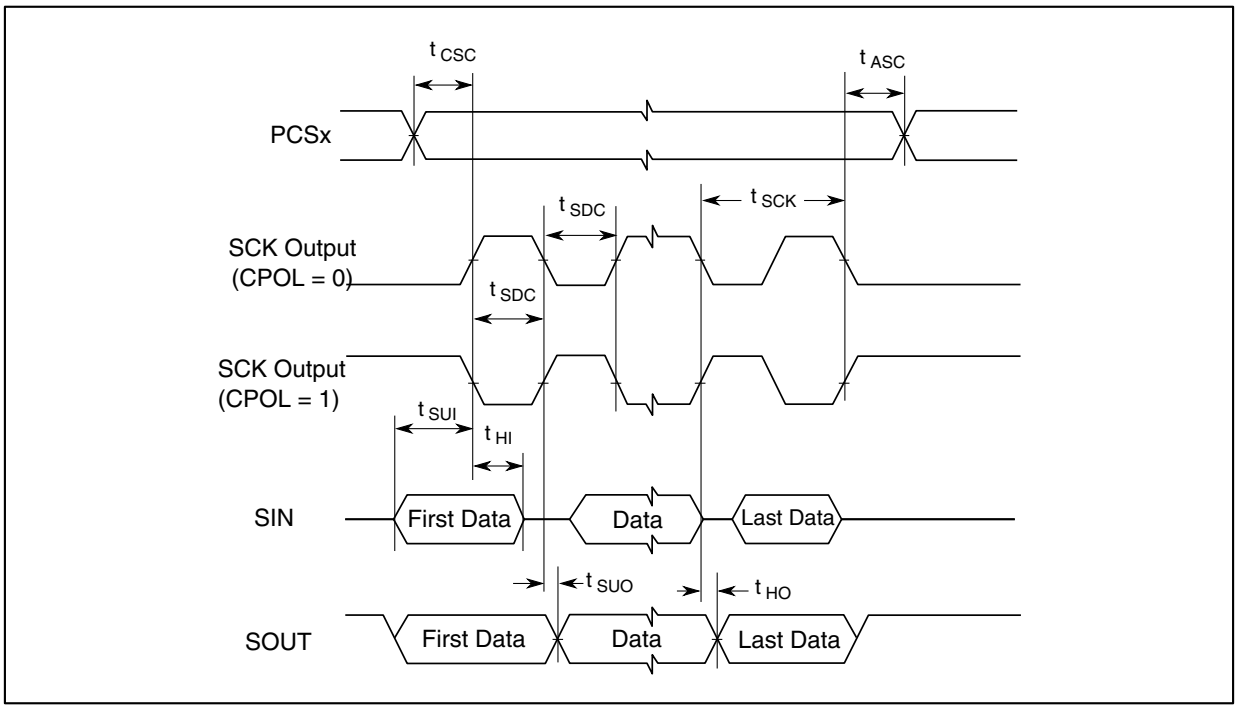

Figure 38. DSPI LVDS master mode – modified timing, CPHA = 0

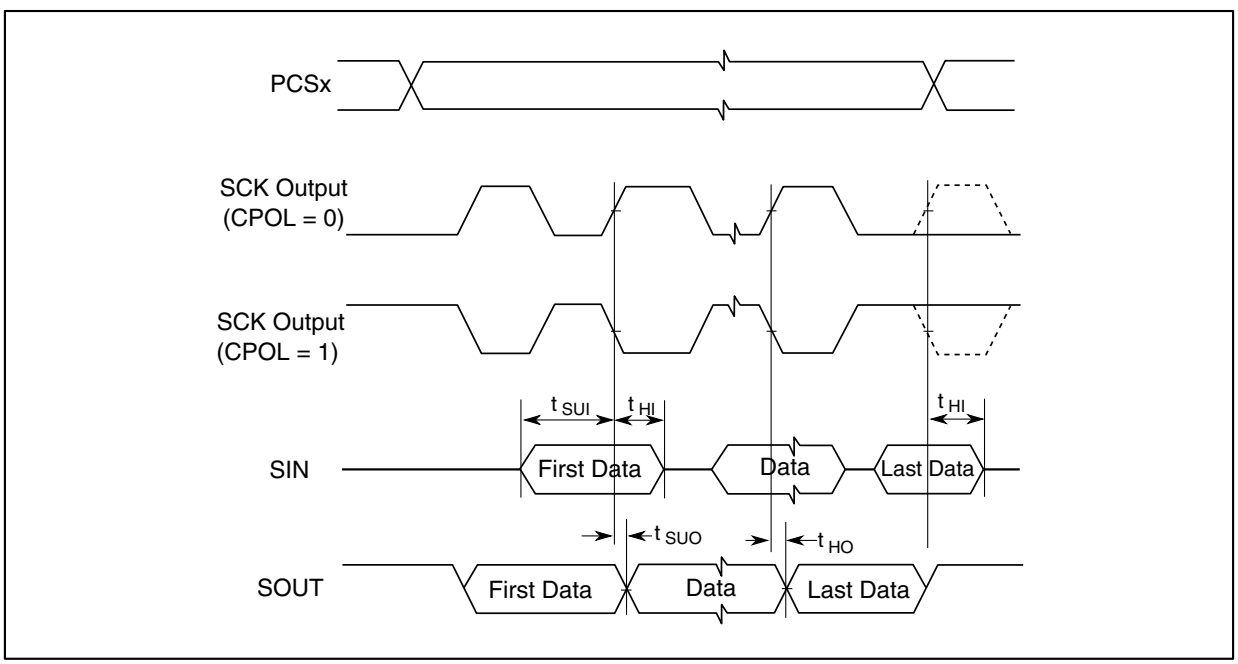

Figure 39. DSPI LVDS master mode – modified timing, CPHA = 1

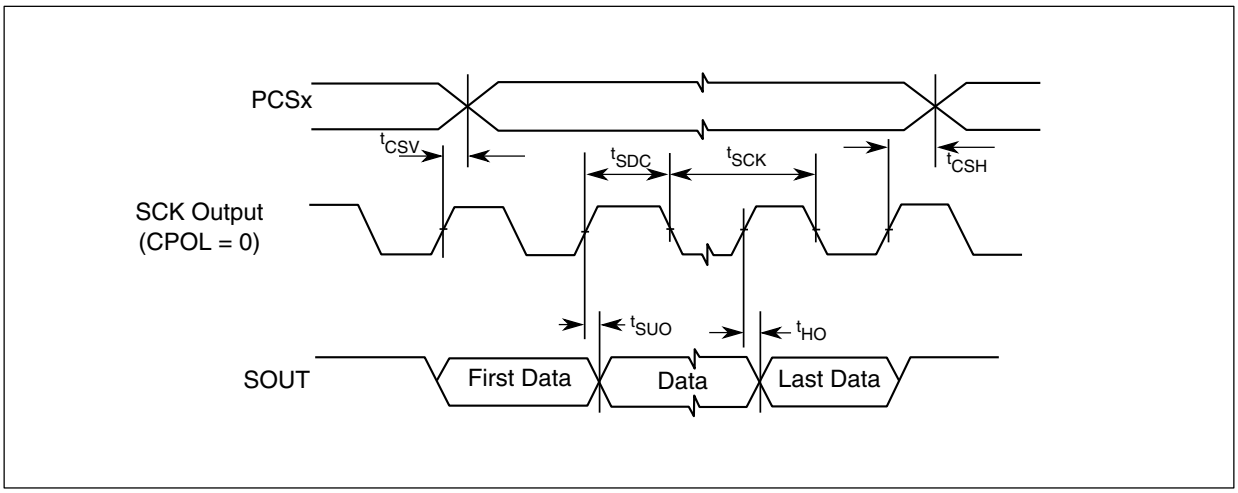

Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 55. Thermal characteristics, 516-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.5	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	20.0	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.5	°C/W
Junction to Board [4]	$R_{\Theta JB}$	8.8	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.1 General notes for thermal characteristics

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately

Table 57. Revision history (continued)

Revision	Date	Description of changes

9 (continued)	06/2016	In I/O pad current specifications
		• Removed sentence: "Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table. The sum of all pad usage ratio within a segment should remain below 100%."
		• Added sentence: "To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1."
		• Added sentence: "To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3."
		
		In Table 18 of Sigma-Delta ADC (SDADC)
		• Removed Z_{IN} specification
		• Added Z_{DIFF}, Z_{CM}, and ΔV_{INTCM} specifications
		• For R_{BIAS}
		  • Changed Parameter description from "Bias resistance" to "Bare bias resistance"
		  • Changed Min from 100 kΩ to 110 kΩ
		  • Changed Typ from 125 kΩ to 144 kΩ
		  • Changed Max from 160 kΩ to 180 kΩ
		
		In Table 24 of LDO mode recommended power transistors
		• For I_{CMaxDC}: Changed Parameter description from "Minimum peak collector current" to "Maximum DC collector current"
		
		In Table 26 of SMPS mode recommended external components and characteristics
		• For part R (Resistor): Changed Nominal value range from 50–100 kΩ to 2.0-4.7 kΩ
		
		In Table 29 of Device voltage monitoring
		• For LVD_core_cold, falling voltage: Changed Min from 1145 mV to 1136 mV
		
		In Power sequencing requirements added new final requirement: "When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device."
		
		In Table 37 of Nexus timing
		• For existing specification 8, TCK Cycle Time (t_{TCYC}):
		  • Changed Min from $4 \times t_{CYC}$ to $2 \times t_{CYC}$
		  • Changed associated footnote from "Lower frequency is required to be fully compliant to standard" to "This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification."
		• Added another row (containing two sub-rows and associated footnotes) for specification 8, TCK Cycle Time (t_{TCYC}):
		  • Absolute minimum TCK cycle time (TDO sampled on posedge of TCK)
		  • Absolute minimum TCK cycle time (TDO sampled on negedge of TCK)
		• For specification 12, TCK Low to TDO Data Valid (t_{NTDOV}): Changed Max from 14 ns to 18 ns
		
		In Package information
		• Added sentence and table explaining how to download latest package drawings
		• Removed subsections: "416-ball package" and "516-ball package"
		
		In Table 55 of Thermal characteristics corrected numbering of footnotes and display of footnote references
		
		In Ordering information removed reference to Freescale