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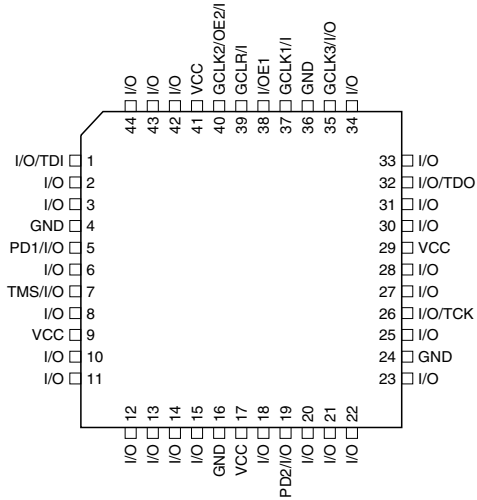**Understanding Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.
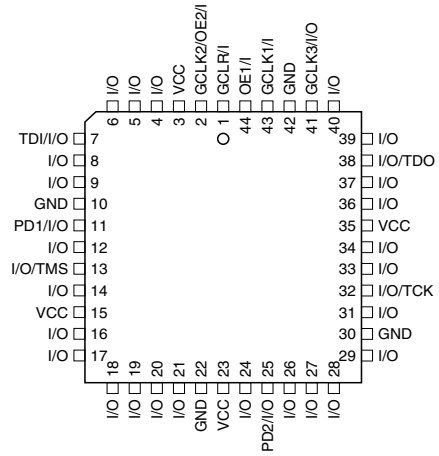
Applications of Embedded - CPLDs

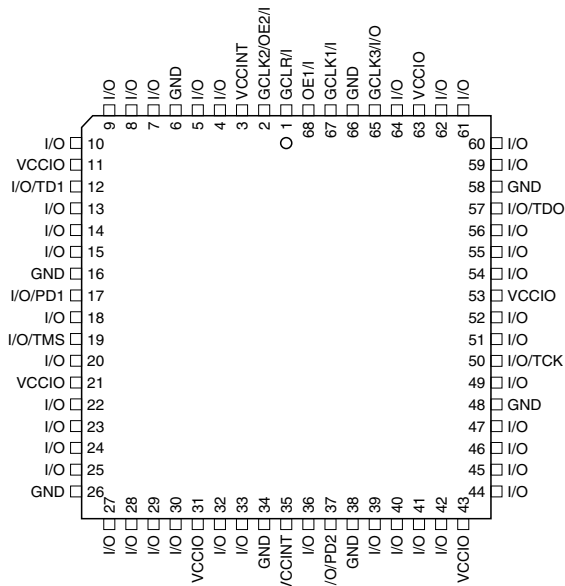| Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atf1504as-10jc84

44-lead TQFP
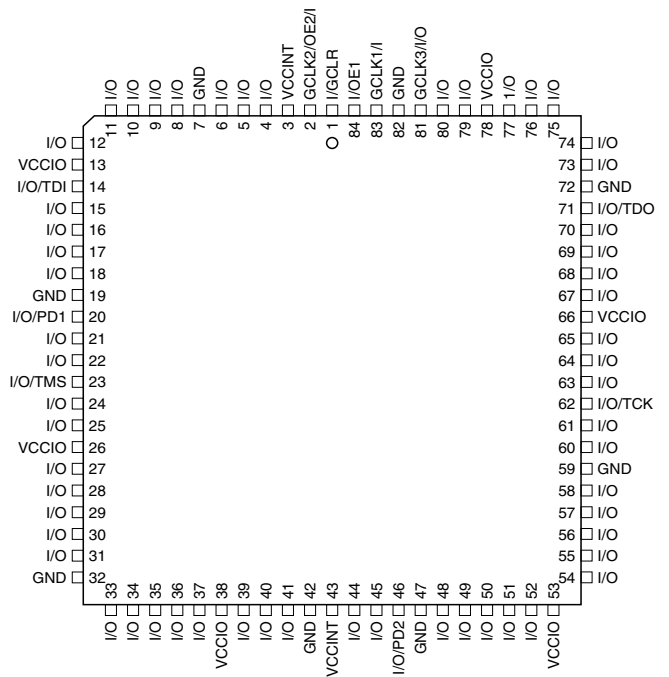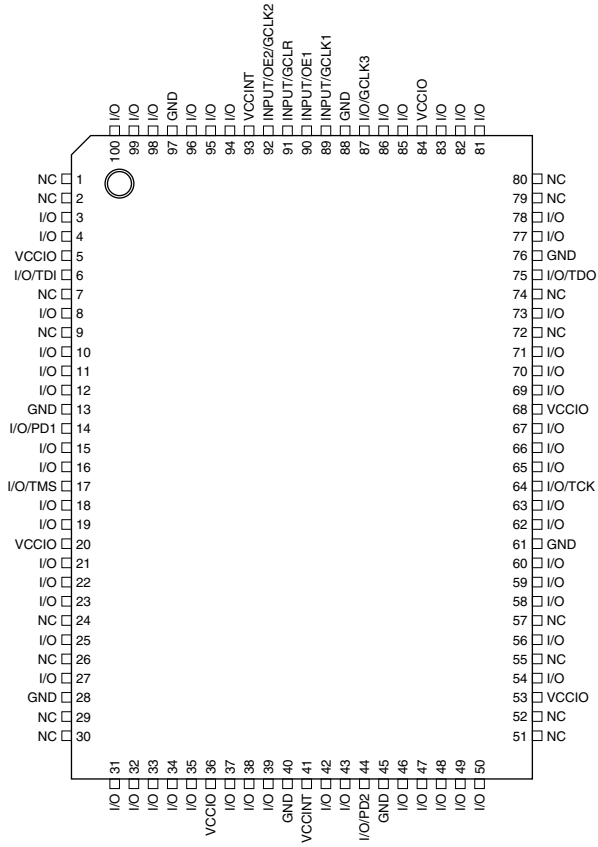**Top View**

Top pins (44-43-42-41-40-39-38-37-36-35-34): I/O, I/O, I/O, VCC, GCLK2/OE2/I, GCLR/I, I/OE1, GCLK1/I, GND, GCLK3/I/O, I/O

Left pins (1-11): I/O/TDI 1, I/O 2, I/O 3, GND 4, PD1/I/O 5, I/O 6, TMS/I/O 7, I/O 8, VCC 9, I/O 10, I/O 11

Right pins (33-23): 33 I/O, 32 I/O/TDO, 31 I/O, 30 I/O, 29 VCC, 28 I/O, 27 I/O, 26 I/O/TCK, 25 I/O, 24 GND, 23 I/O

Bottom pins (12-22): I/O 12, I/O 13, I/O 14, I/O 15, GND 16, VCC 17, I/O 18, PD2/I/O 19, I/O 20, I/O 21, I/O 22

44-lead PLCC
Top View

Top pins (6-5-4-3-2-1-44-43-42-41-40): I/O, I/O, I/O, VCC, GCLK2/OE2/I, GCLR/I, I/OE1, GCLK1/I, GND, GCLK3/I/O, I/O

Left pins (7-17): TDI/I/O 7, I/O 8, I/O 9, GND 10, PD1/I/O 11, I/O 12, I/O/TMS 13, I/O 14, VCC 15, I/O 16, I/O 17

Right pins (39-29): 39 I/O, 38 I/O/TDO, 37 I/O, 36 I/O, 35 VCC, 34 I/O, 33 I/O, 32 I/O/TCK, 31 I/O, 30 GND, 29 I/O

Bottom pins (18-28): I/O 18, I/O 19, I/O 20, I/O 21, GND 22, VCC 23, PD2/I/O 25, I/O 26, I/O 27, I/O 28

68-lead PLCC
Top View

Top pins (9-8-7-6-5-4-3-2-1-68-67-66-65-64-63-62-61): I/O, I/O, I/O, GND, I/O, I/O, VCCINT, GCLK2/OE2/I, GCLR/I, I/OE1, GCLK1/I, GND, GCLK3/I/O, VCCIO, I/O, I/O

Left pins (10-26): I/O 10, VCCIO 11, I/O/TD1 12, I/O 13, I/O 14, I/O 15, GND 16, I/O/PD1 17, I/O 18, I/O/TMS 19, I/O 20, VCCIO 21, I/O 22, I/O 23, I/O 24, I/O 25, GND 26

Right pins (60-44): 60 I/O, 59 I/O, 58 GND, 57 I/O/TDO, 56 I/O, 55 I/O, 54 I/O, 53 VCCIO, 52 I/O, 51 I/O, 50 I/O/TCK, 49 I/O, 48 GND, 47 I/O, 46 I/O, 45 I/O, 44 I/O

Bottom pins (27-43): I/O 27, I/O 28, I/O 29, I/O 30, VCCIO 31, I/O 32, I/O 33, VCCINT 34, GND 35, I/O 36, I/O/PD2 37, GND 38, I/O 39, I/O 40, I/O 41, I/O 42, VCCIO 43

84-lead PLCC
Top View

Top pins (11-10-9-8-7-6-5-4-3-2-1-84-83-82-81-80-79-78-77-76-75): I/O, I/O, I/O, I/O, GND, I/O, I/O, VCCINT, GCLK2/OE2/I, I/GCLR, I/OE1, GCLK1/I, GND, GCLK3/I/O, I/O, I/O, VCCIO, I/O, I/O, I/O

Left pins (12-32): I/O 12, VCCIO 13, I/O/TDI 14, I/O 15, I/O 16, I/O 17, I/O 18, GND 19, I/O/PD1 20, I/O 21, I/O 22, I/O/TMS 23, I/O 24, I/O 25, VCCIO 26, I/O 27, I/O 28, I/O 29, I/O 30, I/O 31, GND 32

Right pins (74-54): 74 I/O, 73 I/O, 72 GND, 71 I/O/TDO, 70 I/O, 69 I/O, 68 I/O, 67 I/O, 66 VCCIO, 65 I/O, 64 I/O, 63 I/O, 62 I/O/TCK, 61 I/O, 60 I/O, 59 GND, 58 I/O, 57 I/O, 56 I/O, 55 I/O, 54 I/O

Bottom pins (33-53): I/O 33, I/O 34, I/O 35, I/O 36, VCCIO 37, I/O 38, I/O 39, I/O 40, I/O 41, GND 42, VCCINT 43, I/O 44, I/O 45, I/O/PD2 46, GND 47, I/O 48, I/O 49, I/O 50, I/O 51, I/O 52, VCCIO 53

100-lead PQFP
Top View

Top pins (100–81): I/O, I/O, I/O, GND, I/O, I/O, I/O, VCCINT, INPUT/OE2/GCLK2, INPUT/GCLR, INPUT/OE1, INPUT/GCLK1, GND, I/O/GCLK3, I/O, I/O, VCCIO, I/O, I/O, I/O

Left pins (1–30):
1 NC
2 NC
3 I/O
4 I/O
5 VCCIO
6 I/O/TDI
7 NC
8 I/O
9 NC
10 I/O
11 I/O
12 I/O
13 GND
14 I/O/PD1
15 I/O
16 I/O
17 I/O/TMS
18 I/O
19 I/O
20 VCCIO
21 I/O
22 I/O
23 I/O
24 NC
25 I/O
26 NC
27 I/O
28 GND
29 NC
30 NC

Right pins (80–51):
80 NC
79 NC
78 I/O
77 I/O
76 GND
75 I/O/TDO
74 NC
73 I/O
72 NC
71 I/O
70 I/O
69 I/O
68 VCCIO
67 I/O
66 I/O
65 I/O
64 I/O/TCK
63 I/O
62 I/O
61 GND
60 I/O
59 I/O
58 I/O
57 NC
56 I/O
55 NC
54 I/O
53 VCCIO
52 NC
51 NC

Bottom pins (31–50): I/O, I/O, I/O, I/O, VCCIO, I/O, I/O, I/O, VCCINT, GND, I/O, I/O, I/O/PD2, GND, I/O, I/O, I/O, I/O, I/O, I/O

100-lead TQFP
Top View

Top pins (100–76): I/O, I/O, I/O, I/O, GND, I/O, I/O, VCCINT, INPUT/OE2/GCLK2, INPUT/GCLR, INPUT/OE1, INPUT/GCLK1, GND, I/O/GCLK3, I/O, I/O, VCCIO, I/O, I/O, NC, NC, I/O

Left pins (1–25):
1 NC
2 NC
3 VCCIO
4 I/O/TDI
5 NC
6 I/O
7 NC
8 I/O
9 I/O
10 I/O
11 GND
12 I/O/PD1
13 I/O
14 I/O
15 I/O/TMS
16 I/O
17 I/O
18 VCCIO
19 I/O
20 I/O
21 I/O
22 NC
23 I/O
24 NC
25 I/O

Right pins (75–51):
75 I/O
74 GND
73 I/O/TDO
72 NC
71 I/O
70 NC
69 I/O
68 I/O
67 I/O
66 VCCIO
65 I/O
64 I/O
63 I/O
62 I/O/TCK
61 I/O
60 I/O
59 GND
58 I/O
57 I/O
56 I/O
55 NC
54 I/O
53 NC
52 I/O
51 VCCIO

Bottom pins (26–50): GND, NC, NC, I/O, I/O, I/O, I/O, I/O, VCCIO, I/O, I/O, I/O, VCCINT, I/O, I/O, I/O/PD2, GND, I/O, I/O, I/O, I/O, I/O, NC, NC

Block Diagram

Logic Block A

Macrocells
1 to 16

6 to 12

I/O Pins

16

Regional
Foldbacks

16

40

Switch
Matrix

12

GLOBAL
BUS
(INPUTS AND FEEDBACKS BUS)

Logic Block D

I/O Pins

Logic Block B

I/O Pins

GOE[0:5]
GCK[0:2]
GCLEAR

Output
Enable
Switch
Matrix

GOE[0:5]

6

Logic Block C

I/O Pins

GCLEAR
GCK[0:2]
GOE[0:5]

I/O (MC64)/GCLK3

Global
Clock
Mux

GCK[0:2]

3

INPUT/GCLK1

OE1/INPUT

INPUT/OE2/GCLK2

Global
Clear
Mux

GCLEAR

1

INPUT/GCLR

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1504AS macrocell has five product terms. Each product term receives as its possible inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1504AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a little small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip-flop

The ATF1504AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either one of the Global CLK Signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1504AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its possible inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504AS offers the option of programming all input and I/O pins so that pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram
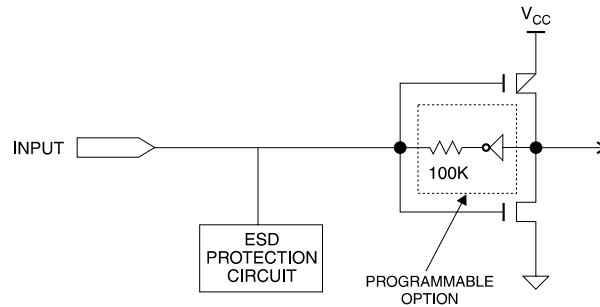
Speed/Power Management

The ATF1504AS has several built-in speed and power management features. The ATF1504AS contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

I/O Diagram
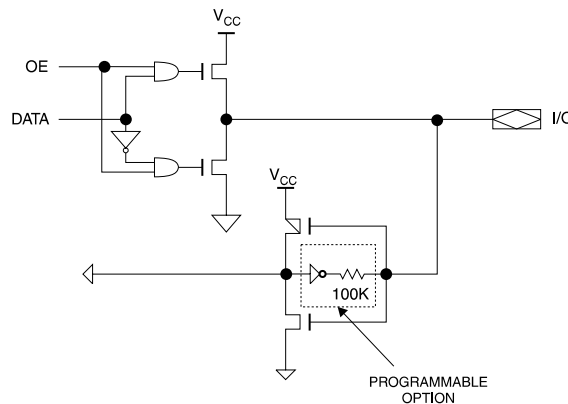
To further reduce power, each ATF1504AS macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504AS also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power-down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced Power Bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

The ATF1504AS macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned-down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1504AS designs are supported by several industry-standard third-party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

Power-up Reset

The ATF1504AS is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF1504AS has two options for the hysteresis about the reset level, V_{RST}, Small and Large. During the fitting process users may configure the device with the Power-up Reset hysteresis set to Large or Small. Atmel POF2JED users may select the Large option by including the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504AS fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CCINT} or V_{CCIO} (5V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	
I_{OZ}	Tri-state Output Off-state Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max $V_{IN} = 0, V_{CC}$	Std Mode	Com.		105		mA
				Ind.		130		mA
			"L" Mode	Com.		10		µA
				Ind.		10		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max $V_{IN} = 0, V_{CC}$	"PD" Mode			1	10	mA
I_{CC3} [2]	Current in Reduced-power Mode	V_{CC} = Max $V_{IN} = 0,$ VCC	Std Power	Com		85		ma
				Ind		105		
V_{CCIO}	Supply Voltage	5.0V Device Output		Com.	4.75		5.25	V
				Ind.	4.5		5.5	V
V_{CCIO}	Supply Voltage	3.3V Device Output			3.0		3.6	V
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OL} = 12 mA		Com.			0.45	V
				Ind.				
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OL} = 0.1 mA		Com.			.2	V
				Ind.			.2	V
V_{OH}	Output High Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OH} = -4.0 mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. When macrocell reduced-power feature is enabled.

Pin Capacitance

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Absolute Maximum Ratings*

Temperature Under Bias .... -40°C to +85°C

Storage Temperature .... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground .... -2.0V to +7.0V[1]

Voltage on Input Pins
with Respect to Ground
During Programming .... -2.0V to +14.0V[1]

Programming Voltage with
Respect to Ground .... -2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

AC Characteristics

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		ns
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	166.7		125		100		83.3		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		2		1.5		4		5		6	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		5.5		8		10		10	ns

Note: See ordering information for valid part numbers.

Timing Model
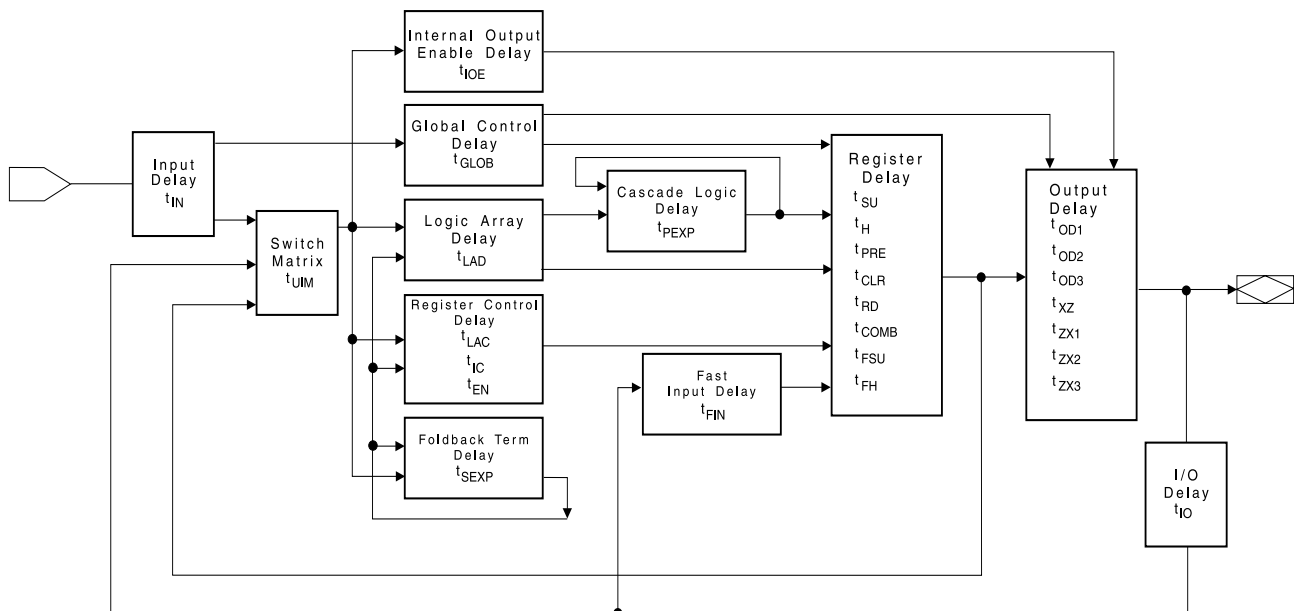
AC Characteristics (Continued)

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		4.0		5.0		7		9		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		4.5		5.5		7		9		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		9		9		10		11		12	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		4		5		6		7		8	ns
t_{SU}	Register Setup Time	3		3		4		5		6		ns
t_H	Register Hold Time	2		3		4		5		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t_{RD}	Register Delay		1		2		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		6		7		8	ns
t_{EN}	Register Enable Time		3		5		6		7		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		5		6	ns
t_{CLR}	Register Clear Time		2		3		4		5		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t_{RPA}	Reduced-power Adder[2]		10		11		13		14		15	ns

Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

Input Test Waveforms and Measurement Levels
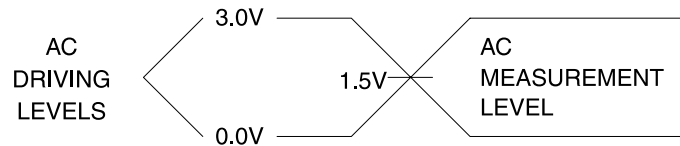
t_R, t_F = 1.5 ns typical

Output AC Test Loads

```
                        5.0V

        R1 = 464Ω  ⌇
                          OUTPUT
                            PIN
        R2 = 250Ω  ⌇    ⊥ CL = 35 pF
                   ▽    ▽
```
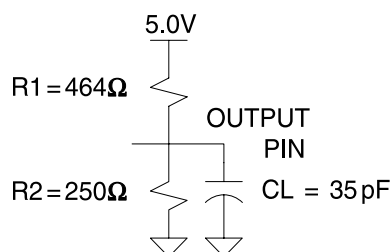
Note: *Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

Power-down Mode

The ATF1504AS includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down mode feature is enabled in the logic design file or as a fitted or translated s/w option. Designs using the power-down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power Down AC Characteristics[1][2]

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	7		10		15		20		25		ns
t_{GVDH}	Valid OE[2] before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock[2] before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		30		35	ns
t_{DHGX}	OE[2] Don't Care after PD High		12		15		25		30		35	ns
t_{DHCX}	Clock[2] Don't Care after PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	μs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	μs

Notes: 1. For slow slew outputs, add t_{SSO}.
         2. Pin or product term.
         3. Includes t_{RPA} due to reduced power bit enabled.

JTAG-BST/ISP Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary scan testing. The ATF1504AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504AS's ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504AS programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504AS has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504AS is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1504AS contains up to 68 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)
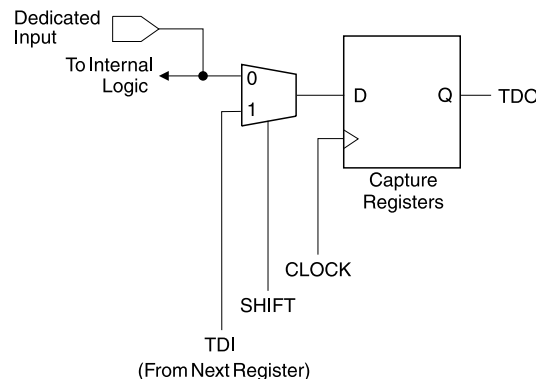
Note: The ATF1504AS has pull-up option on TMS and TDI pins. This feature is selected as a design option.
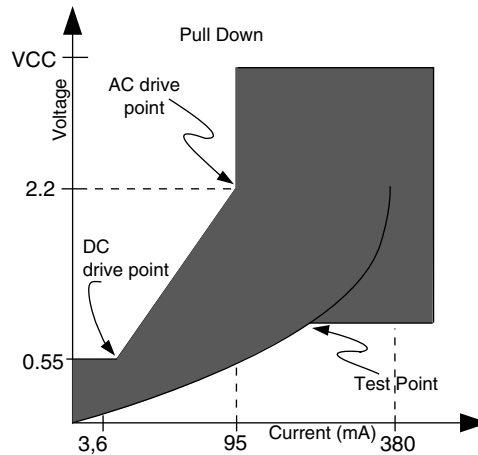
PCI Compliance

The ATF1504AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS allows this without contributing to system noise while delivering low output-to-output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance. The PCI electrical characteristics appear on the next page.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode
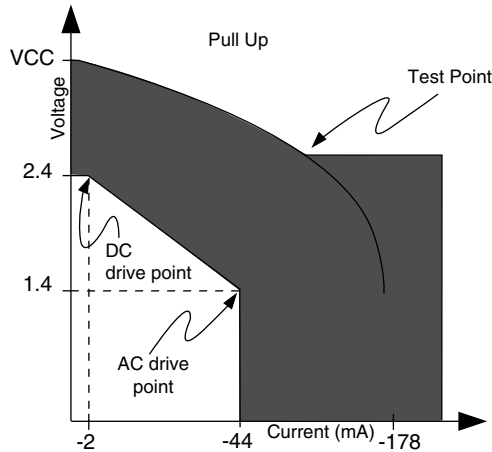
PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode

SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T$_A$ = 25°C, F = 0)

STANDARD

REDUCED POWER MODE

I$_{CC}$ (mA) / V$_{CC}$ (V)
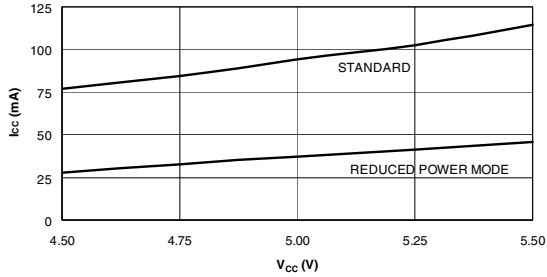
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
(T$_A$ = 25°C, F = 0)

STANDARD POWER

REDUCED POWER MODE

I$_{CC}$ (μA) / V$_{CC}$ (V)
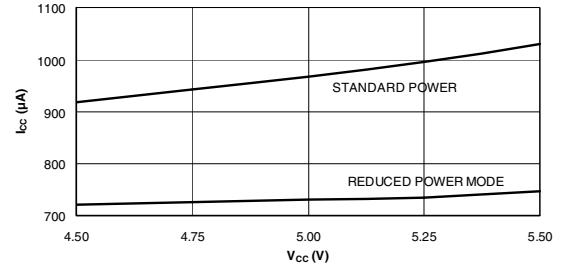
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW-POWER ("L") VERSION
(T$_A$ = 25°C, F = 0)

I$_{CC}$ (μA) / V$_{CC}$ (V)
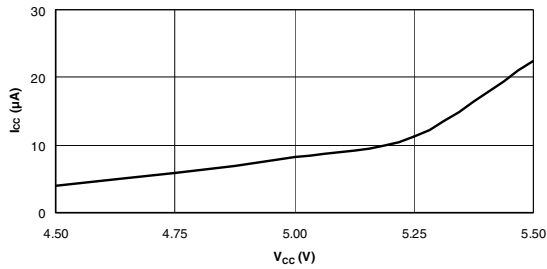
SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION
LOW POWER (T$_A$ = 25°C)

STANDARD POWER

REDUCED POWER MODE

I$_{CC}$ (mA) / FREQUENCY (MHz)
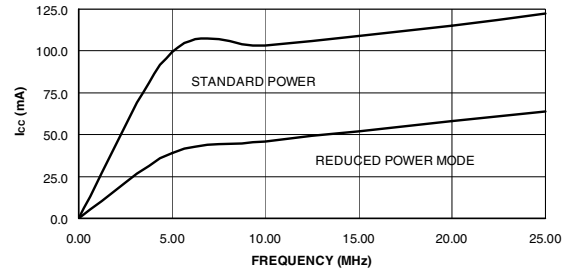
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER (T$_A$ = 25°C)

STANDARD POWER

REDUCED POWER MODE

I$_{CC}$ (mA) / FREQUENCY (MHz)
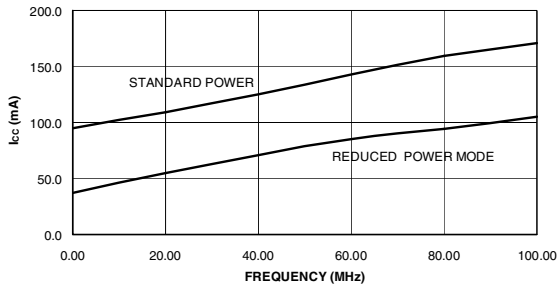
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE
(V$_{CC}$ = 5V, T$_A$ = 25°C)

IOH (mA) / OUTPUT VOLTAGE (V)
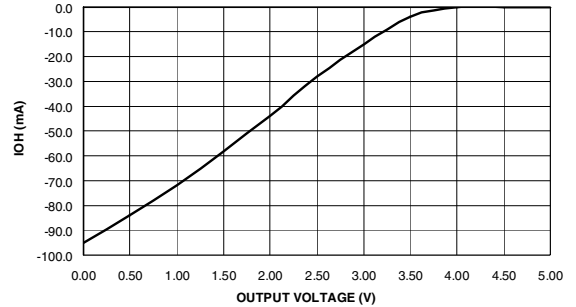
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE
(VOH = 2.4V, T$_A$ = 25°C)

IOH (mA) / SUPPLY VOLTAGE (V)
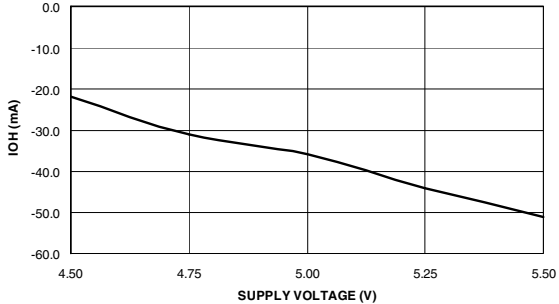
INPUT CLAMP CURRENT VS. INPUT VOLTAGE
(V$_{CC}$ = 5V, T$_A$ = 25°C)
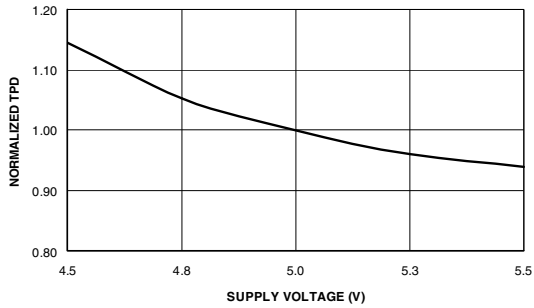

INPUT CURRENT (mA) / INPUT VOLTAGE (V)
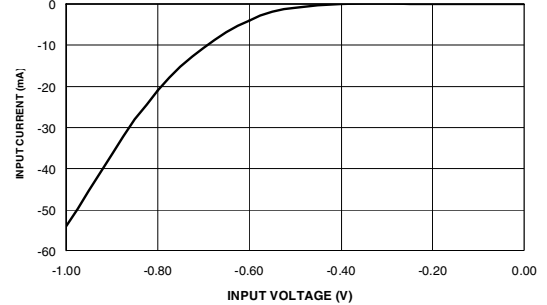
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE
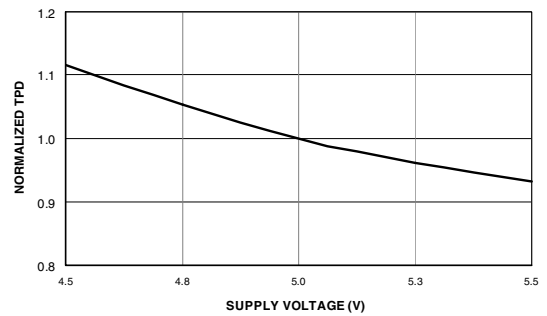**(VOL = 0.5V, T$_A$ = 25°C)**
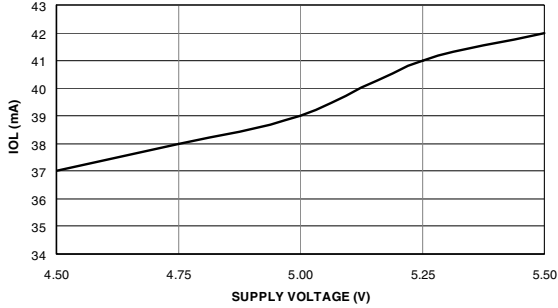
NORMALIZED TPD
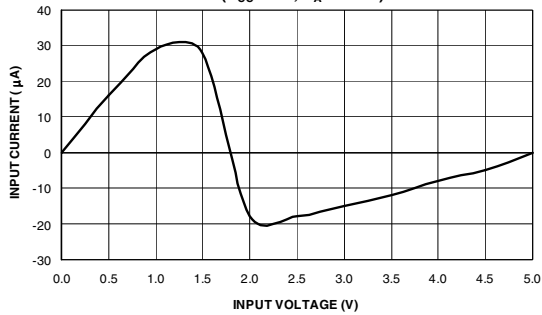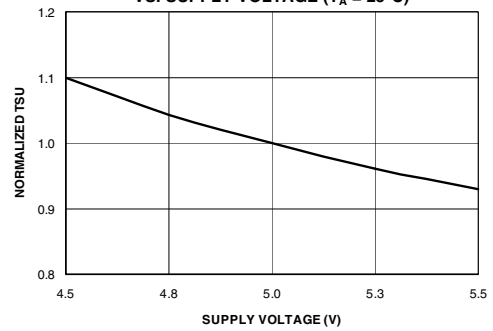**VS. TEMPERATURE (V$_{CC}$ = 5.0V)**
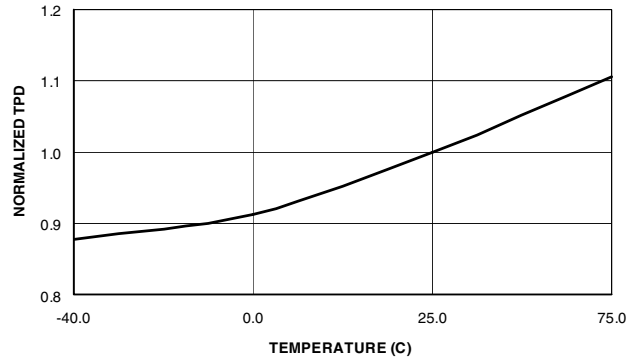
NORMALIZED TPD
VS. SUPPLY VOLTAGE (T$_A$ = 25°C)
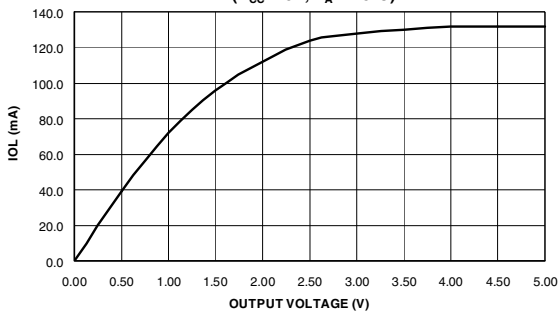
NORMALIZED TCO
VS. SUPPLY VOLTAGE (T$_A$ = 25°C)

INPUT CURRENT VS. INPUT VOLTAGE
(V$_{CC}$ = 5V, T$_A$ = 25°C)

NORMALIZED TSU
VS. SUPPLY VOLTAGE (T$_A$ = 25°C)

OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
(V$_{CC}$ = 5V, T$_A$ = 25°C)

NORMALIZED TCO
VS.TEMPERATURE (V$_{CC}$ = 5.0V)

NORMALIZED TSU
VS. TEMPERATURE (V$_{CC}$ = 5.0V)
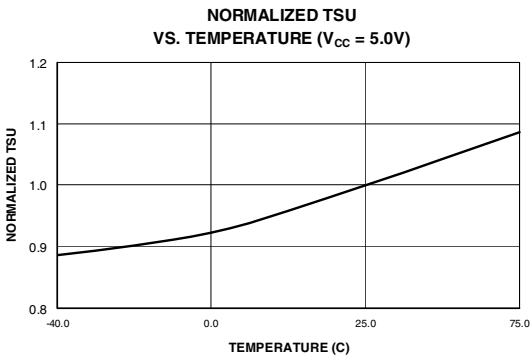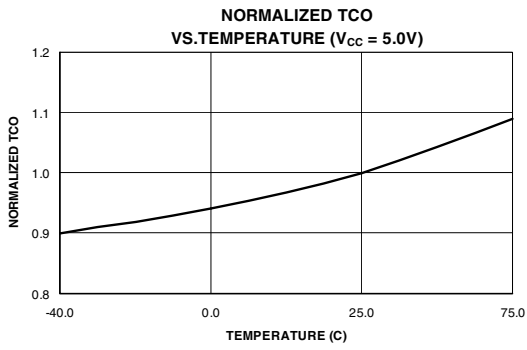
ATF1504AS Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1504AS-7 AC44	44A	Commercial (0°C to 70°C)
			ATF1504AS-7 JC44	44J	
			ATF1504AS-7 JC68	68J	
			ATF1504AS-7 JC84	84J	
			ATF1504AS-7 QC100	100Q1	
			ATF1504AS-7 AC100	100A	
10	5	125	ATF1504AS-10 AC44	44A	Commercial (0°C to 70°C)
			ATF1504AS-10 JC44	44J	
			ATF1504AS-10 JC68	68J	
			ATF1504AS-10 JC84	84J	
			ATF1504AS-10 QC100	100Q1	
			ATF1504AS-10 AC100	100A	
10	5	125	ATF1504AS-10 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504AS-10 JI44	44J	
			ATF1504AS-10 JI68	68J	
			ATF1504AS-10 JI84	84J	
			ATF1504AS-10 QI100	100Q1	
			ATF1504AS-10 AI100	100A	
15	8	100	ATF1504AS-15 AC44	44A	Commercial (0°C to 70°C)
			ATF1504AS-15 JC44	44J	
			ATF1504AS-15 JC68	68J	
			ATF1504AS-15 JC84	84J	
			ATF1504AS-15 QC100	100Q1	
			ATF1500AS-15 AC100	100A	
15	8	100	ATF1504AS-15 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504AS-15 JI44	44J	
			ATF1504AS-15 JI68	68J	
			ATF1504AS-15 JI84	84J	
			ATF1504AS-15 QI100	100Q1	
			ATF1504AS-15 AI100	100A	

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7 ns "C" = 10 ns "I") and de-rate power by 30%.
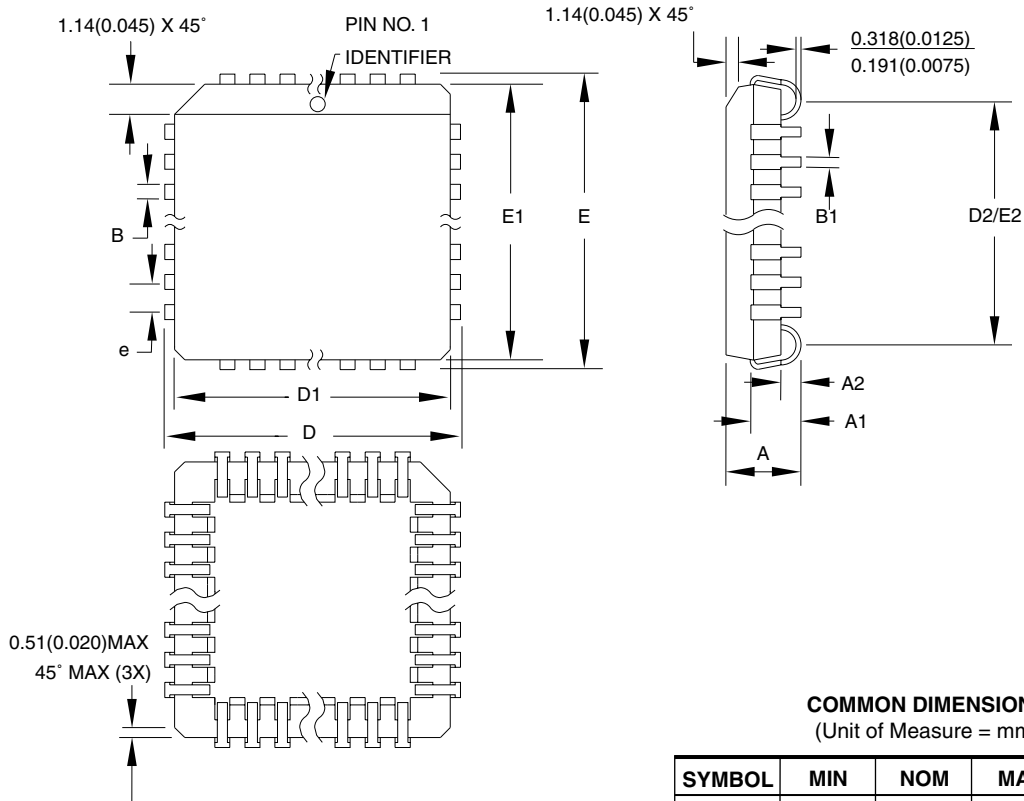
ATF1504ASL Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1504ASL-20 AC44	44A	Commercial
			ATF1504ASL-20 JC44	44J	(0°C to 70°C)
			ATF1504ASL-20 JC68	68J	
			ATF1504ASL-20 JC84	84J	
			ATF1504ASL-20 QC100	100Q1	
			ATF1504ASL-20 AC100	100A	
25	15	70	ATF1504ASL-25 AI44	44A	Industrial
			ATF1504ASL-25 JI84	44J	(-40°C to +85°C)
			ATF1504ASL-25 JI68	68J	
			ATF1504ASL-25 JI84	84J	
			ATF1504ASL-25 QI100	100Q1	
			ATF1504ASL-25 AI100	100A	

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7 ns "C" = 10 ns "I") and de-rate power by 30%.

44J – PLCC

Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

10/04/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

1.14(0.045) X 45˚

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45˚

0.318(0.0125)
0.191(0.0075)

E1 E

B

e

D1

D

B1

D2/E2

A2

A1

A

0.51(0.020)MAX
45˚ MAX (3X)

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes: 1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

0950N–PLD–07/02