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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

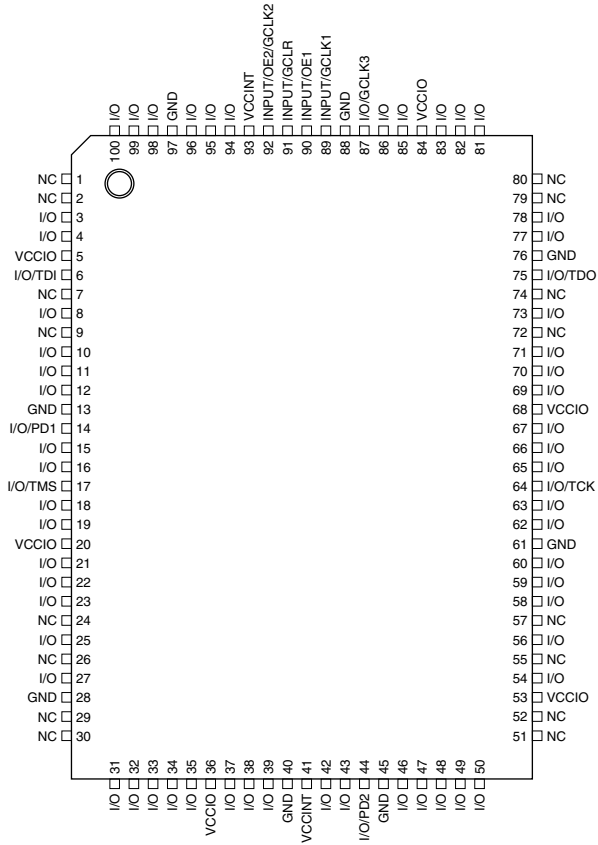
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

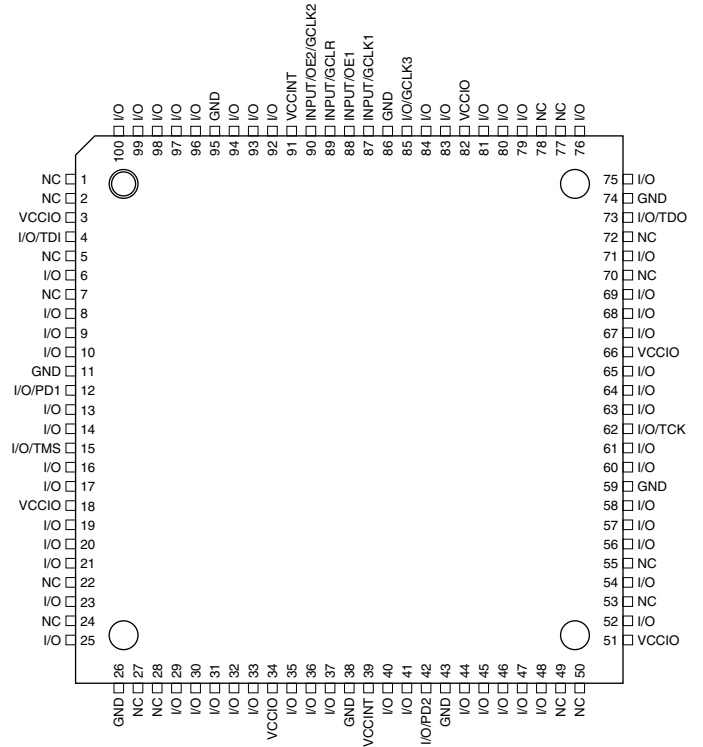
#### Details

Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-15ai44">https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-15ai44</a>

**100-lead PQFP  
Top View**



**100-lead TQFP  
Top View**



## Description

The ATF1504AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504AS's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504AS has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504AS allows fast, efficient generation of complex logic functions. The ATF1504AS contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

## **Product Terms and Select Mux**

Each ATF1504AS macrocell has five product terms. Each product term receives as its possible inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

## **OR/XOR/CASCADE Logic**

The ATF1504AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a little small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

## **Flip-flop**

The ATF1504AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either one of the Global CLK Signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

## **Output Select and Enable**

The ATF1504AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

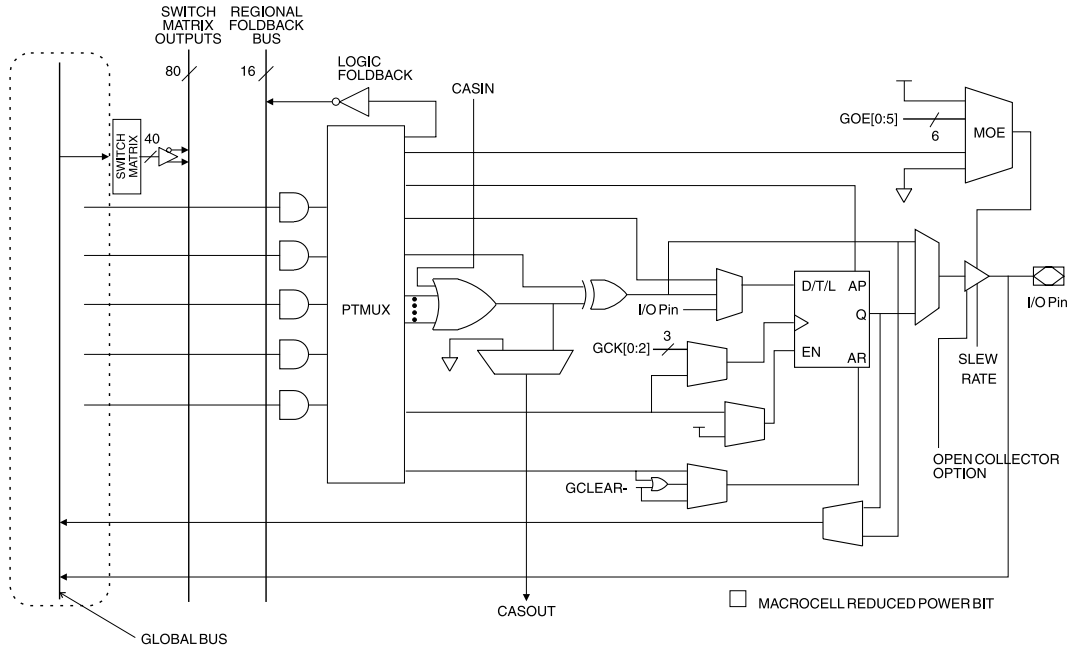
## **Global Bus/Switch Matrix**

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its possible inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

## Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The sixteen foldback terms in each region allow generation of high fan-in sum terms (up to sixteen product terms) with a nominal additional delay.

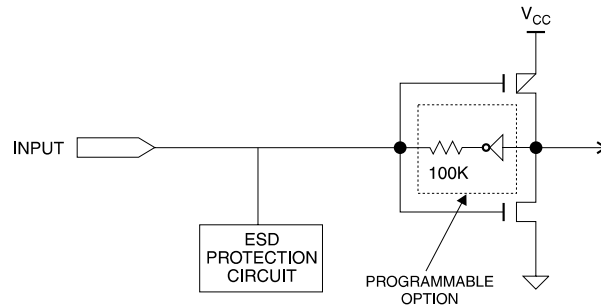
**Figure 1. ATF1504AS Macrocell**



## Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504AS offers the option of programming all input and I/O pins so that pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

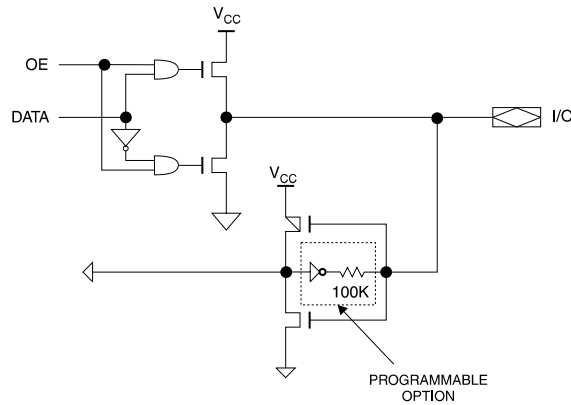
### Input Diagram



## Speed/Power Management

The ATF1504AS has several built-in speed and power management features. The ATF1504AS contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

### I/O Diagram



To further reduce power, each ATF1504AS macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504AS also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power-down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

## Programming

ATF1504AS devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504AS devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

## ISP Programming Protection

The ATF1504AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504AS is being programmed via ISP.

All ATF1504AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

## Absolute Maximum Ratings\*

Temperature Under Bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note:** 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## AC Characteristics

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD1}$	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
$t_{PD2}$	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		25	ns
$t_{SU}$	Global Clock Setup Time	6		7		11		16		20		ns
$t_H$	Global Clock Hold Time	0		0		0		0		0		ns
$t_{FSU}$	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
$t_{FH}$	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		ns
$t_{COP}$	Global Clock to Output Delay		4.5		5		8		10		13	ns
$t_{CH}$	Global Clock High Time	3		4		5		6		7		ns
$t_{CL}$	Global Clock Low Time	3		4		5		6		7		ns
$t_{ASU}$	Array Clock Setup Time	3		3		4		4		5		ns
$t_{AH}$	Array Clock Hold Time	2		3		4		5		6		ns
$t_{ACOP}$	Array Clock Output Delay		7.5		10		15		20		25	ns
$t_{ACH}$	Array Clock High Time	3		4		6		8		10		ns
$t_{ACL}$	Array Clock Low Time	3		4		6		8		10		ns
$t_{CNT}$	Minimum Clock Global Period		8		10		13		17		22	ns
$f_{CNT}$	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
$t_{ACNT}$	Minimum Array Clock Period		8		10		13		17		22	ns
$f_{ACNT}$	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

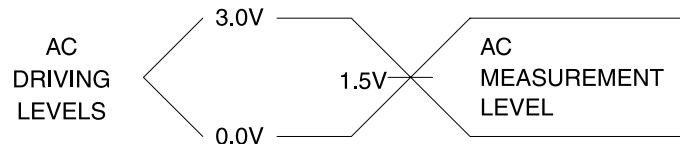


## AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{ZX1}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$ ; $C_L = 35$ pF)		4.0		5.0		7		9		10	ns
$t_{ZX2}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$ ; $C_L = 35$ pF)		4.5		5.5		7		9		10	ns
$t_{ZX3}$	Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO} = 5.0V/3.3V$ ; $C_L = 35$ pF)		9		9		10		11		12	ns
$t_{XZ}$	Output Buffer Disable Delay ( $C_L = 5$ pF)		4		5		6		7		8	ns
$t_{SU}$	Register Setup Time	3		3		4		5		6		ns
$t_H$	Register Hold Time	2		3		4		5		6		ns
$t_{FSU}$	Register Setup Time of Fast Input	3		3		2		2		3		ns
$t_{FH}$	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
$t_{RD}$	Register Delay		1		2		1		2		2	ns
$t_{COMB}$	Combinatorial Delay		1		2		1		2		2	ns
$t_{IC}$	Array Clock Delay		3		5		6		7		8	ns
$t_{EN}$	Register Enable Time		3		5		6		7		8	ns
$t_{GLOB}$	Global Control Delay		1		1		1		1		1	ns
$t_{PRE}$	Register Preset Time		2		3		4		5		6	ns
$t_{CLR}$	Register Clear Time		2		3		4		5		6	ns
$t_{UIM}$	Switch Matrix Delay		1		1		2		2		2	ns
$t_{RPA}$	Reduced-power Adder <sup>(2)</sup>		10		11		13		14		15	ns

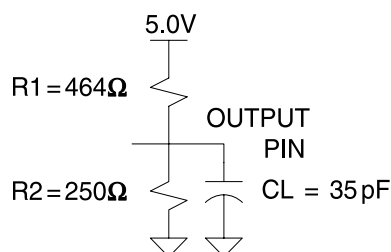
- Notes: 1. See ordering information for valid part numbers.  
2. The  $t_{RPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{TIC}$ ,  $t_{ACL}$ , and  $t_{SEXP}$  parameters for macrocells running in the reduced-power mode.

## Input Test Waveforms and Measurement Levels



$t_R$ ,  $t_F = 1.5$  ns typical

## Output AC Test Loads



Note: \*Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

## Power-down Mode

The ATF1504AS includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down mode feature is enabled in the logic design file or as a fitted or translated s/w option. Designs using the power-down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

## Power Down AC Characteristics<sup>(1)(2)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IVDH}$	Valid I, I/O before PD High	7		10		15		20		25		ns
$t_{GV DH}$	Valid OE <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{CVDH}$	Valid Clock <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{DHIX}$	I, I/O Don't Care after PD High		12		15		25		30		35	ns
$t_{DHGX}$	OE <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DHCX}$	Clock <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DLIV}$	PD Low to Valid I, I/O		1		1		1		1		1	μs
$t_{DLGV}$	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
$t_{DLCV}$	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
$t_{DLOV}$	PD Low to Valid Output		1		1		1		1		1	μs

- Notes:
1. For slow slew outputs, add  $t_{SSO}$ .
  2. Pin or product term.
  3. Includes  $t_{RPA}$  due to reduced power bit enabled.

## JTAG-BST/ISP Overview

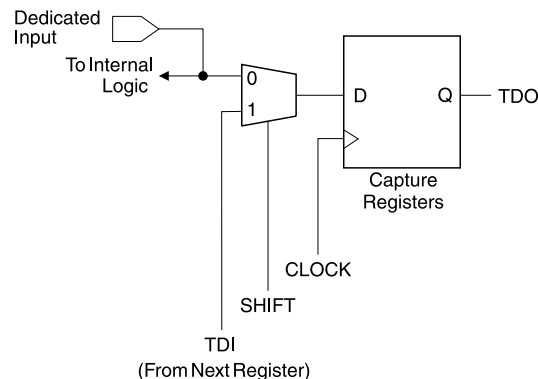
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary scan testing. The ATF1504AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504AS's ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504AS programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504AS has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504AS is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

## JTAG Boundary-scan Cell (BSC) Testing

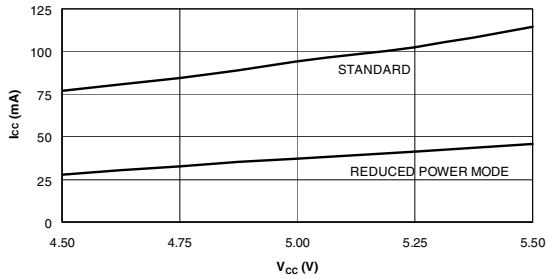
The ATF1504AS contains up to 68 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

## BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)

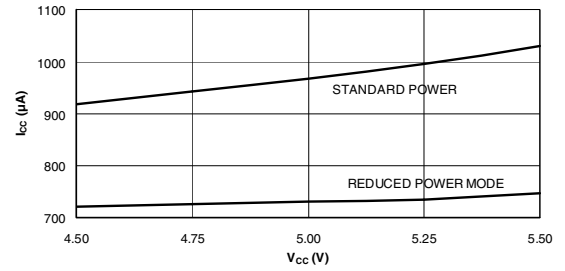


Note: The ATF1504AS has pull-up option on TMS and TDI pins. This feature is selected as a design option.

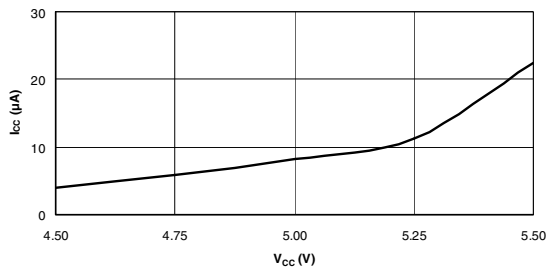
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



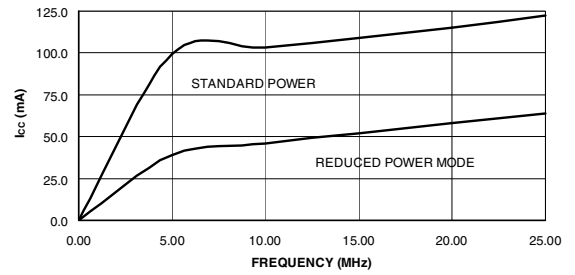
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**PIN-CONTROLLED POWER-DOWN MODE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



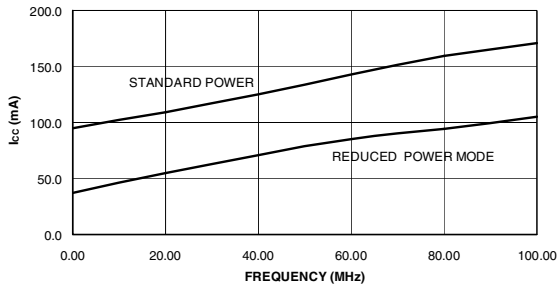
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**LOW-POWER ("L") VERSION**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



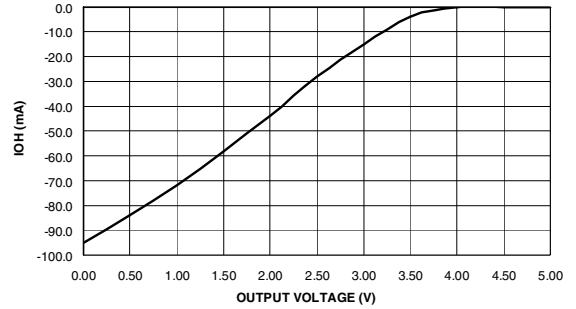
**SUPPLY CURRENT VS. FREQUENCY**  
**LOW-POWER ("L") VERSION**  
**LOW POWER ( $T_A = 25^\circ\text{C}$ )**



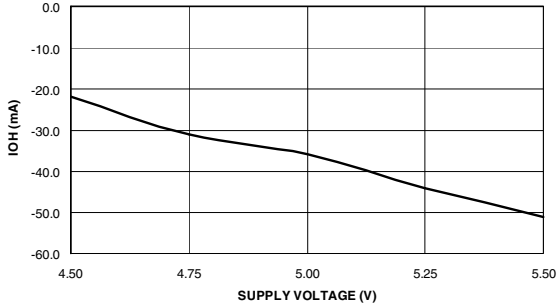
**SUPPLY CURRENT VS. FREQUENCY**  
**STANDARD POWER ( $T_A = 25^\circ\text{C}$ )**



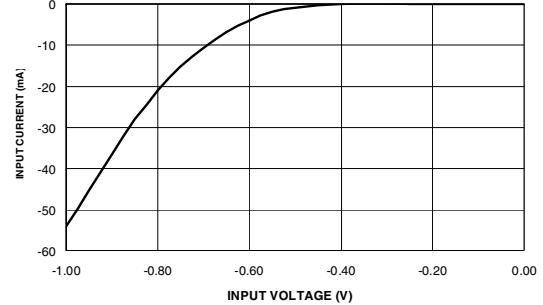
**OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE**  
( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



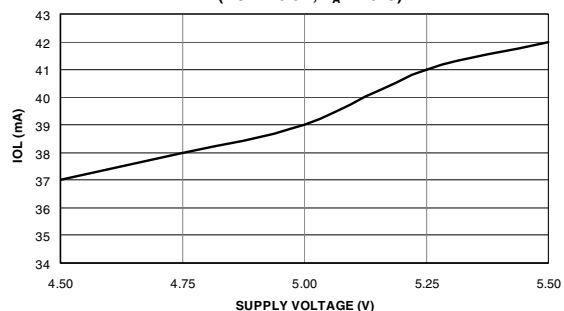
**OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE**  
( $V_{OH} = 2.4\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



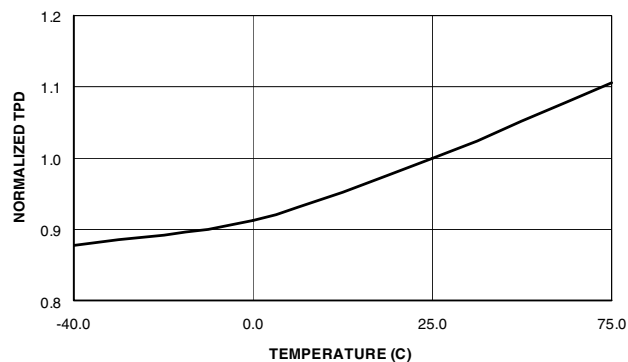
**INPUT CLAMP CURRENT VS. INPUT VOLTAGE**  
( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



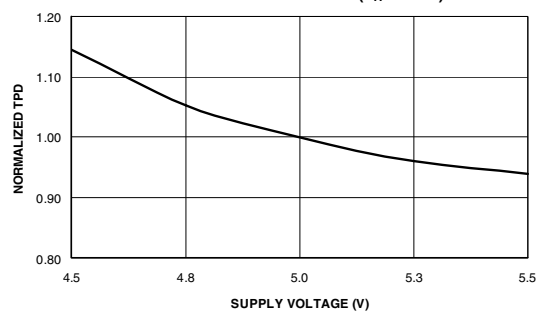
**OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE**  
(VOL = 0.5V,  $T_A = 25^\circ\text{C}$ )



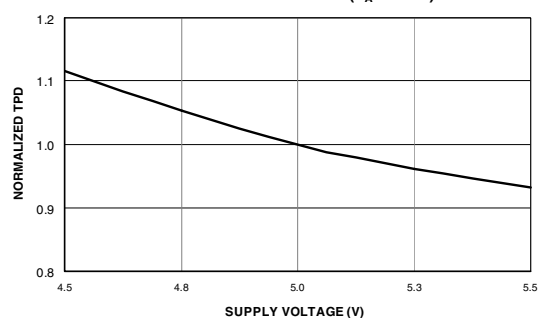
**NORMALIZED TPD**  
**VS. TEMPERATURE ( $V_{CC} = 5.0\text{V}$ )**



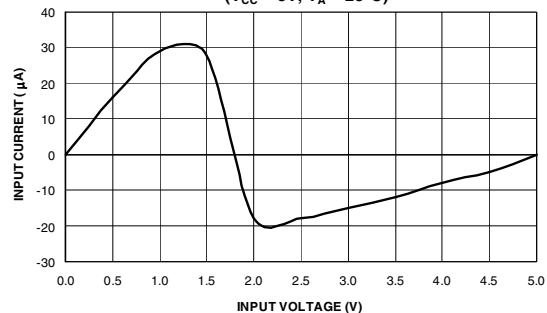
**NORMALIZED TPD**  
**VS. SUPPLY VOLTAGE ( $T_A = 25^\circ\text{C}$ )**



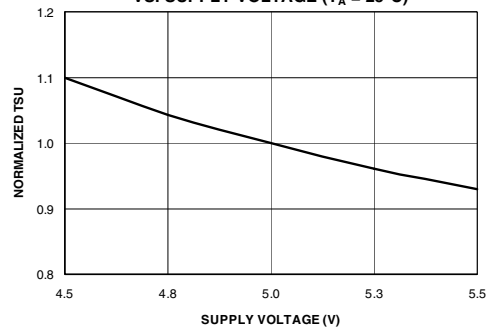
**NORMALIZED TCO**  
**VS. SUPPLY VOLTAGE ( $T_A = 25^\circ\text{C}$ )**



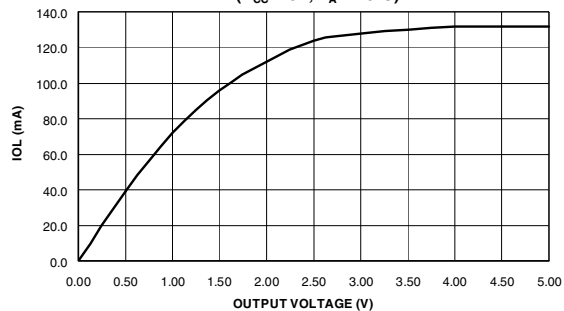
**INPUT CURRENT VS. INPUT VOLTAGE**  
( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )

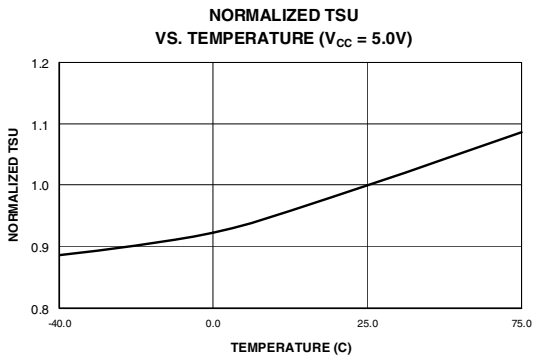
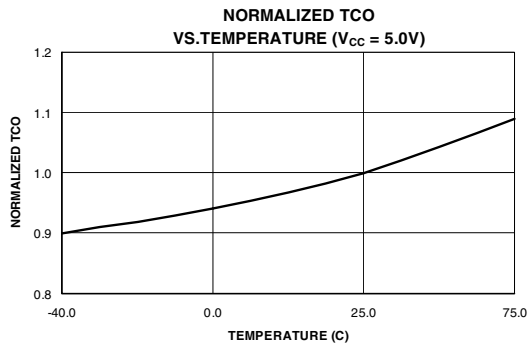


**NORMALIZED TSU**  
**VS. SUPPLY VOLTAGE ( $T_A = 25^\circ\text{C}$ )**



**OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE**  
( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )





## ATF1504AS Ordering Information

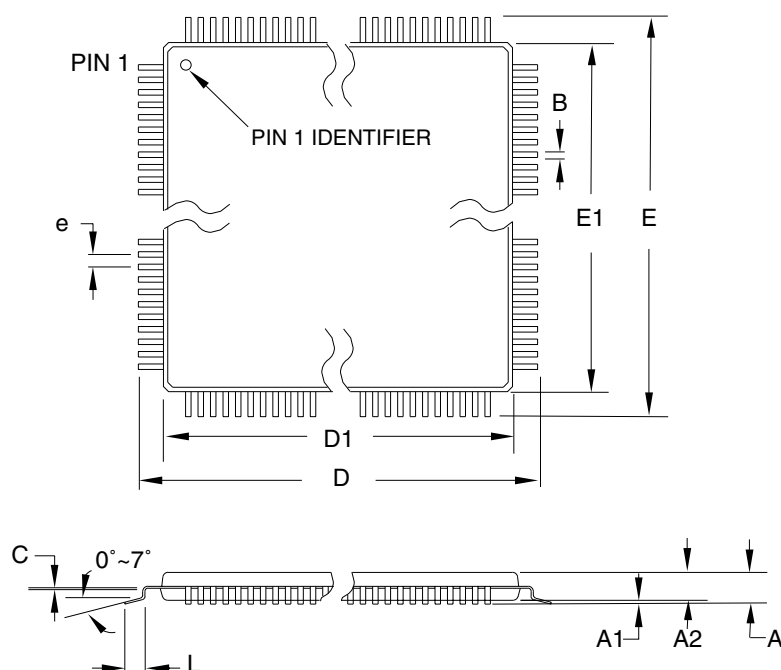
$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1504AS-7 AC44 ATF1504AS-7 JC44 ATF1504AS-7 JC68 ATF1504AS-7 JC84 ATF1504AS-7 QC100 ATF1504AS-7 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AC44 ATF1504AS-10 JC44 ATF1504AS-10 JC68 ATF1504AS-10 JC84 ATF1504AS-10 QC100 ATF1504AS-10 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AI44 ATF1504AS-10 JI44 ATF1504AS-10 JI68 ATF1504AS-10 JI84 ATF1504AS-10 QI100 ATF1504AS-10 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)
15	8	100	ATF1504AS-15 AC44 ATF1504AS-15 JC44 ATF1504AS-15 JC68 ATF1504AS-15 JC84 ATF1504AS-15 QC100 ATF1500AS-15 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
15	8	100	ATF1504AS-15 AI44 ATF1504AS-15 JI44 ATF1504AS-15 JI68 ATF1504AS-15 JI84 ATF1504AS-15 QI100 ATF1504AS-15 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

# Packaging Information

## 44A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	—	0.45	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,  
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

### DRAWING NO.

44A

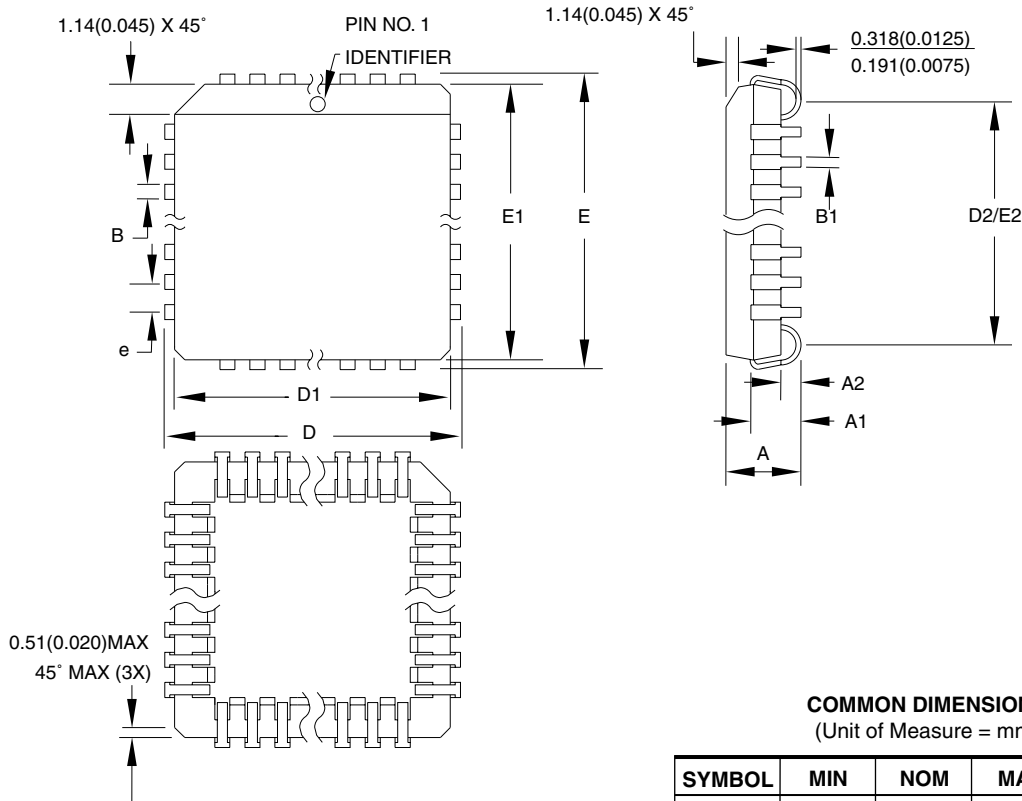
### REV.

B





## 44J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	17.399	—	17.653	
D1	16.510	—	16.662	Note 2
E	17.399	—	17.653	
E1	16.510	—	16.662	Note 2
D2/E2	14.986	—	16.002	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

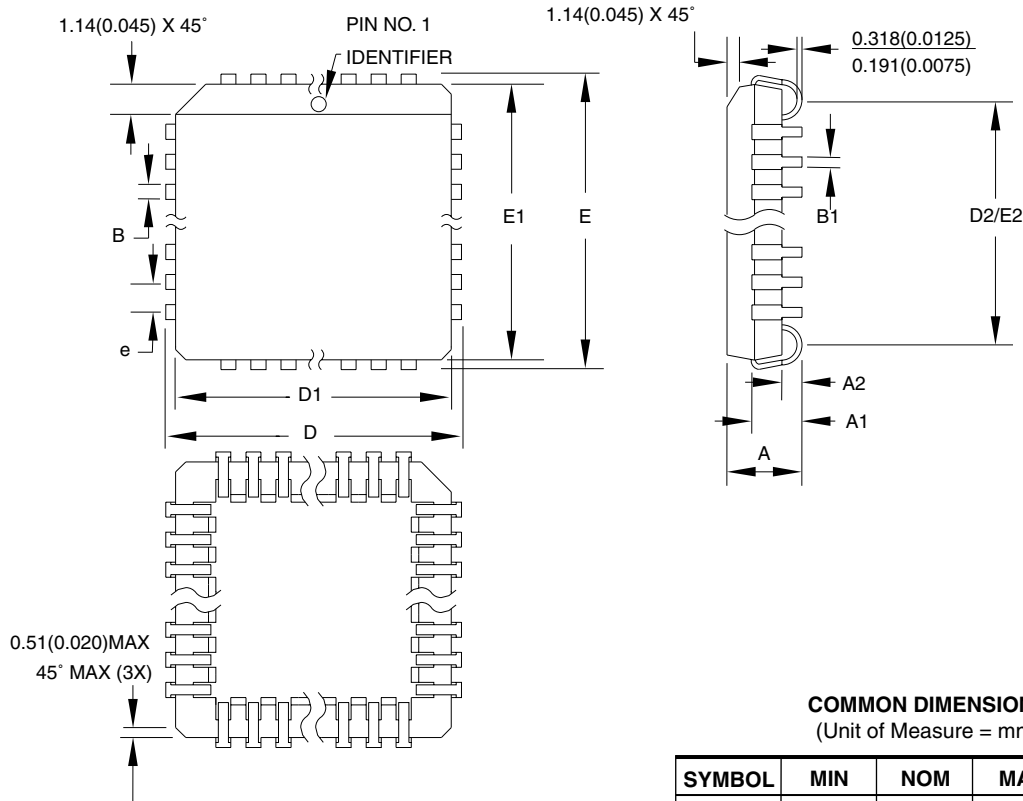
### DRAWING NO.

44J

### REV.

B

## 68J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	25.019	—	25.273	
D1	24.130	—	24.333	Note 2
E	25.019	—	25.273	
E1	24.130	—	24.333	Note 2
D2/E2	22.606	—	23.622	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AE.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**68J**, 68-lead, Plastic J-leaded Chip Carrier (PLCC)

**DRAWING NO.**

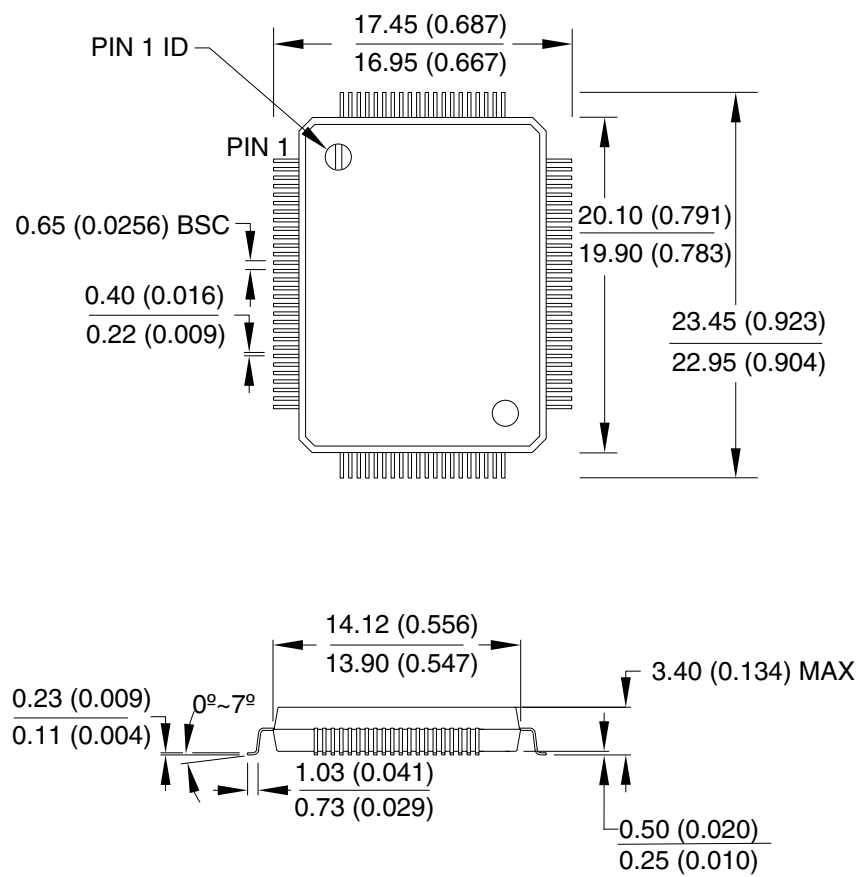
68J

**REV.**


B

100Q1 – PQFP

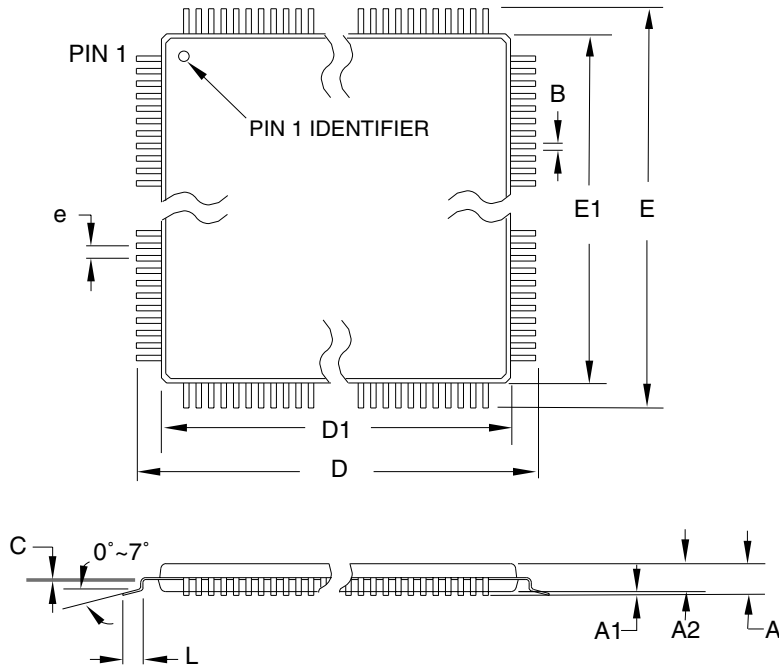
Dimensions in Millimeters and (Inches)\*  
 \*Controlling dimensions: millimeters  
 JEDEC STANDARD MS-022, GC-1



04/11/2001

 2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>100Q1</b> , 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	<b>DRAWING NO.</b> 100Q1	<b>REV.</b> A
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# 100A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.08 mm maximum.

10/5/2001



2325 Orchard Parkway  
San Jose, CA 95131

## TITLE

**100A**, 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness,  
0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

## DRAWING NO.

100A

## REV.

C



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