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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

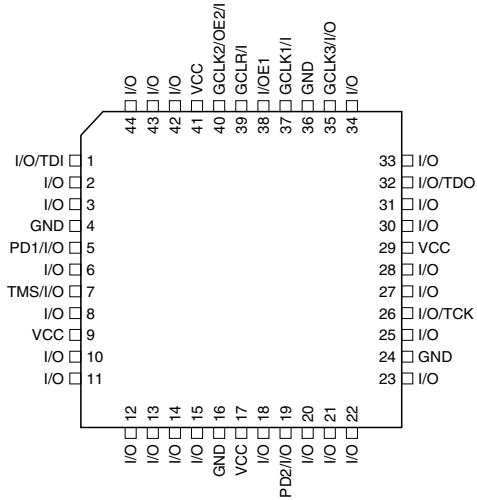
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

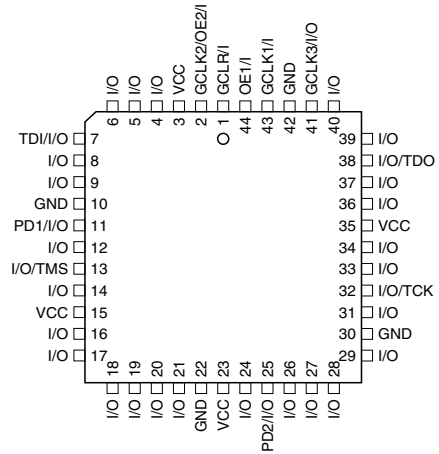
Details

Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	48
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-15jc68

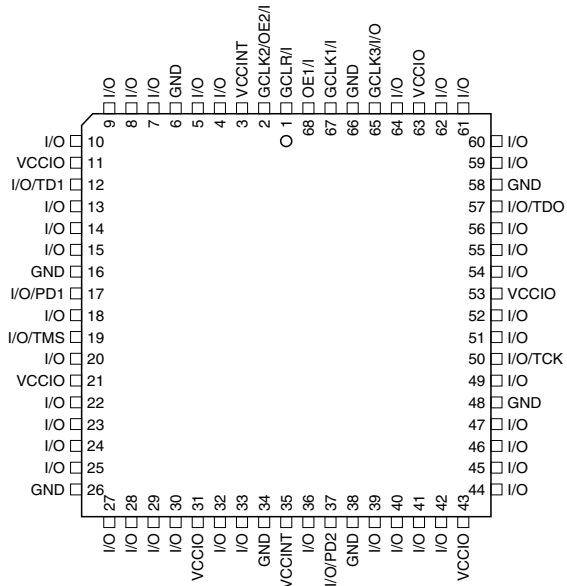
44-lead TQFP
Top View



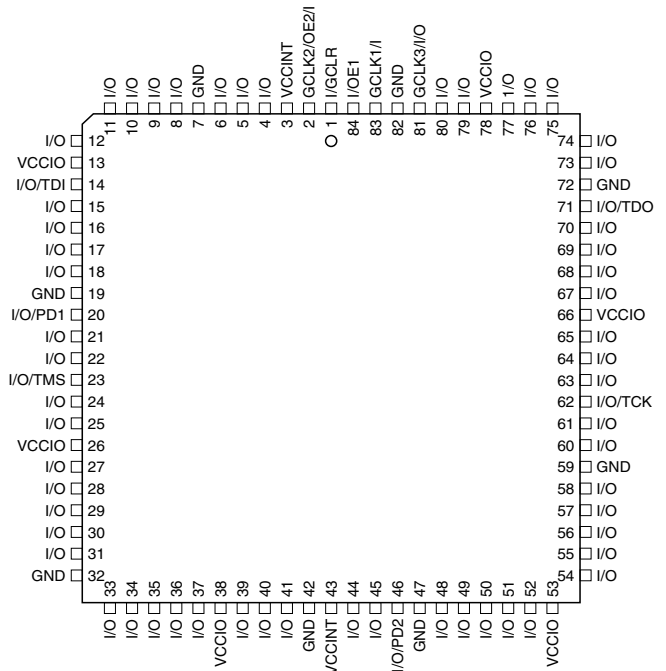
44-lead PLCC
Top View



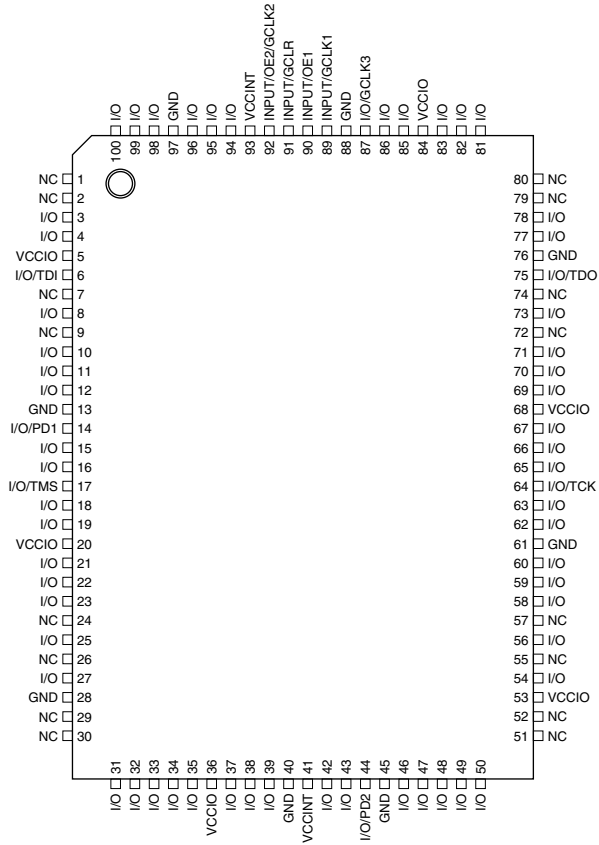
68-lead PLCC
Top View



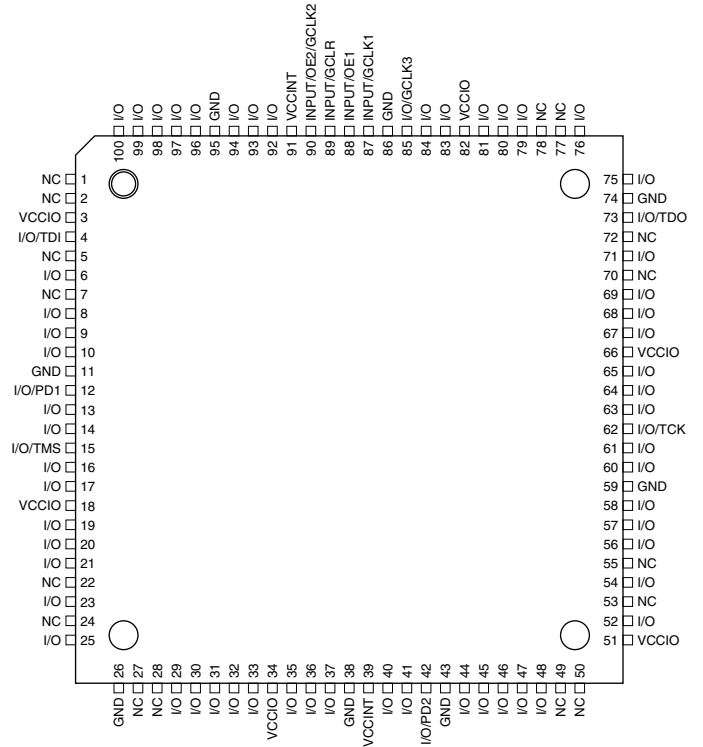
84-lead PLCC
Top View



**100-lead PQFP
Top View**



**100-lead TQFP
Top View**



Product Terms and Select Mux

Each ATF1504AS macrocell has five product terms. Each product term receives as its possible inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1504AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a little small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip-flop

The ATF1504AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either one of the Global CLK Signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1504AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

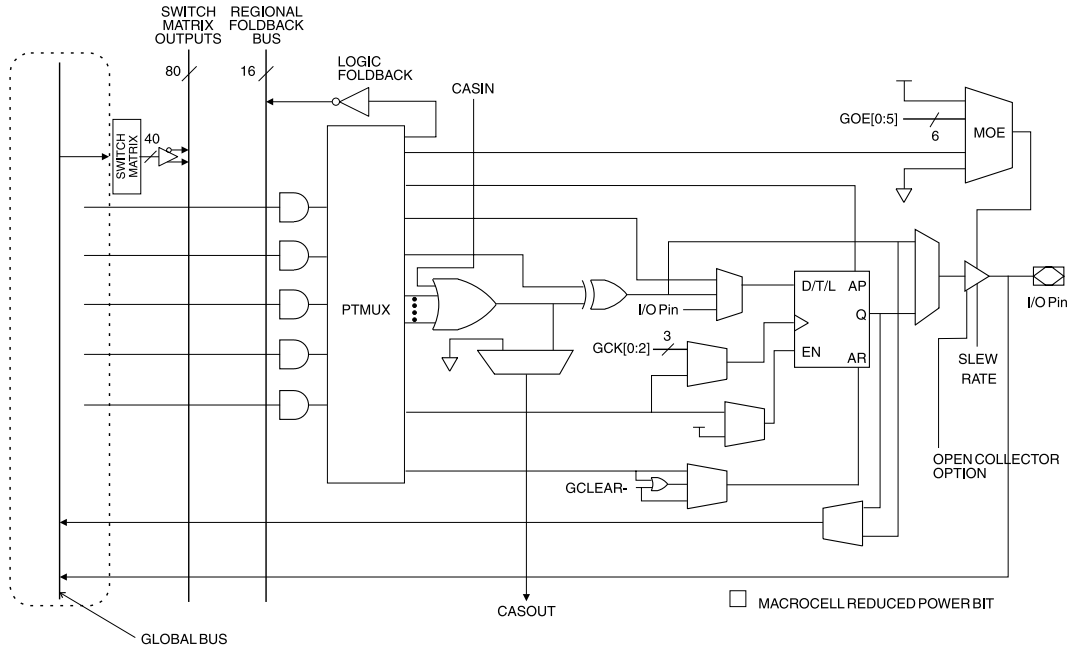
Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its possible inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The sixteen foldback terms in each region allow generation of high fan-in sum terms (up to sixteen product terms) with a nominal additional delay.

Figure 1. ATF1504AS Macrocell



All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced Power Bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{ACH} and t_{SEXP} .

The ATF1504AS macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned-down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1504AS designs are supported by several industry-standard third-party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

Power-up Reset

The ATF1504AS is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D .

The ATF1504AS has two options for the hysteresis about the reset level, V_{RST} , Small and Large. During the fitting process users may configure the device with the Power-up Reset hysteresis set to Large or Small. Atmel POF2JED users may select the Large option by including the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504AS fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.



Programming

ATF1504AS devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504AS devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1504AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504AS is being programmed via ISP.

All ATF1504AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20 ns.

AC Characteristics

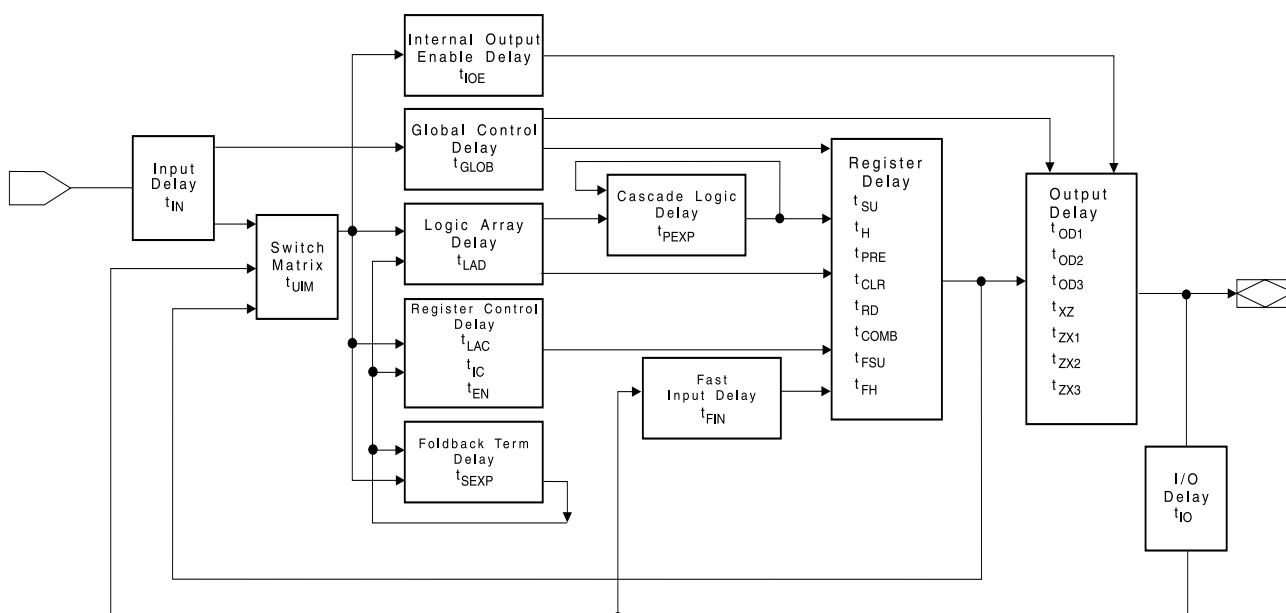
Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		ns
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	166.7		125		100		83.3		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{\text{CCIO}} = 5\text{V}$; $C_L = 35\text{ pF}$)		2		1.5		4		5		6	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{\text{CCIO}} = 3.3\text{V}$; $C_L = 35\text{ pF}$)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; $V_{\text{CCIO}} = 5\text{V}$ or 3.3V ; $C_L = 35\text{ pF}$)		5		5.5		8		10		10	ns

Note: See ordering information for valid part numbers.

Timing Model

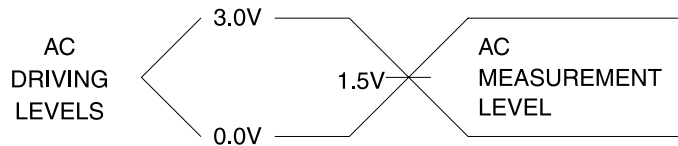


AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$; $C_L = 35$ pF)		4.0		5.0		7		9		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$; $C_L = 35$ pF)		4.5		5.5		7		9		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO} = 5.0V/3.3V$; $C_L = 35$ pF)		9		9		10		11		12	ns
t_{XZ}	Output Buffer Disable Delay ($C_L = 5$ pF)		4		5		6		7		8	ns
t_{SU}	Register Setup Time	3		3		4		5		6		ns
t_H	Register Hold Time	2		3		4		5		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t_{RD}	Register Delay		1		2		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		6		7		8	ns
t_{EN}	Register Enable Time		3		5		6		7		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		5		6	ns
t_{CLR}	Register Clear Time		2		3		4		5		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t_{RPA}	Reduced-power Adder ⁽²⁾		10		11		13		14		15	ns

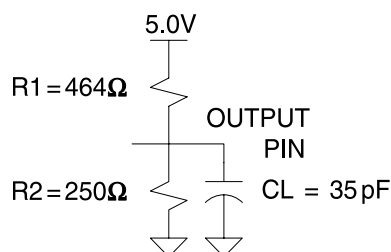
- Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{TIC} , t_{ACL} , and t_{SEXP} parameters for macrocells running in the reduced-power mode.

Input Test Waveforms and Measurement Levels



t_R , $t_F = 1.5$ ns typical

Output AC Test Loads



Note: *Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

Power-down Mode

The ATF1504AS includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down mode feature is enabled in the logic design file or as a fitted or translated s/w option. Designs using the power-down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power Down AC Characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	7		10		15		20		25		ns
$t_{GV DH}$	Valid OE ⁽²⁾ before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock ⁽²⁾ before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		30		35	ns
t_{DHGX}	OE ⁽²⁾ Don't Care after PD High		12		15		25		30		35	ns
t_{DHCX}	Clock ⁽²⁾ Don't Care after PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	μs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	μs

- Notes:
1. For slow slew outputs, add t_{SSO} .
 2. Pin or product term.
 3. Includes t_{RPA} due to reduced power bit enabled.

JTAG-BST/ISP Overview

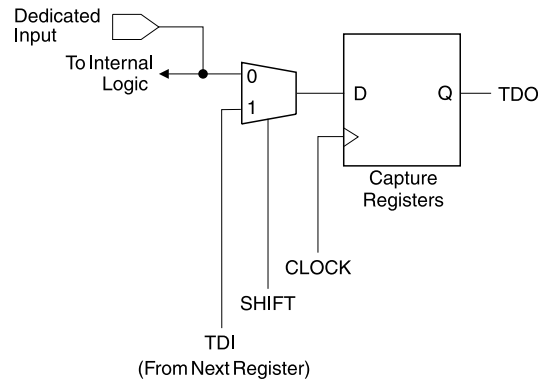
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary scan testing. The ATF1504AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504AS's ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504AS programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504AS has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504AS is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1504AS contains up to 68 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

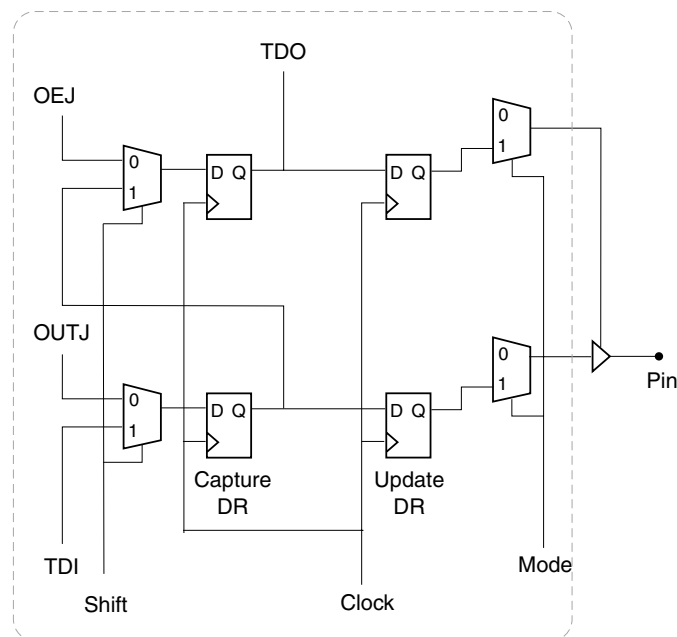
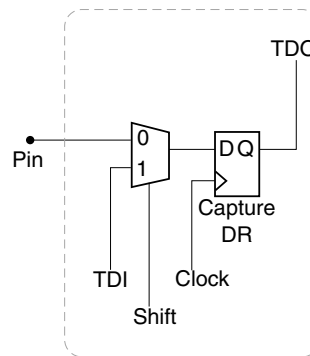
BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: The ATF1504AS has pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell

Pin BSC

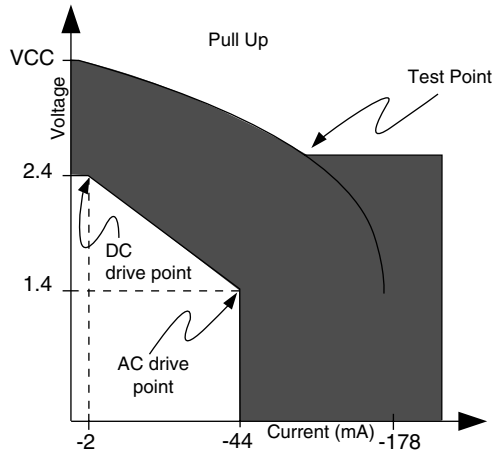


Macrocell BSC

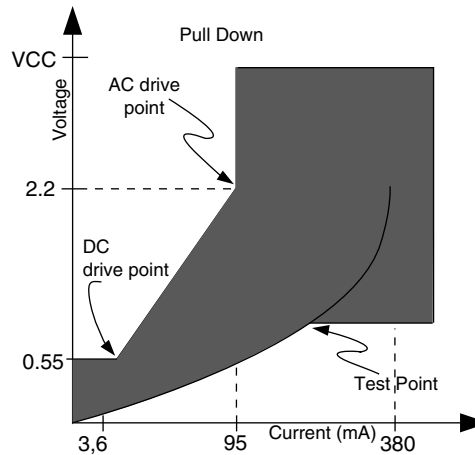
PCI Compliance

The ATF1504AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS allows this without contributing to system noise while delivering low output-to-output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance. The PCI electrical characteristics appear on the next page.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current	$V_{IN} = 2.7V$		70	μA
I_{IL}	Input Low Leakage Current	$V_{IN} = 0.5V$		-70	μA
V_{OH}	Output High Voltage	$I_{OUT} = -2\text{ mA}$	2.4		V
V_{OL}	Output Low Voltage	$I_{OUT} = 3\text{ mA}, 6\text{ mA}$		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: Leakage current is with pin-keeper off.

PCI AC Characteristics

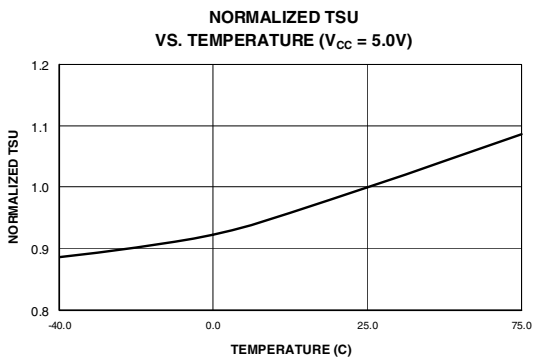
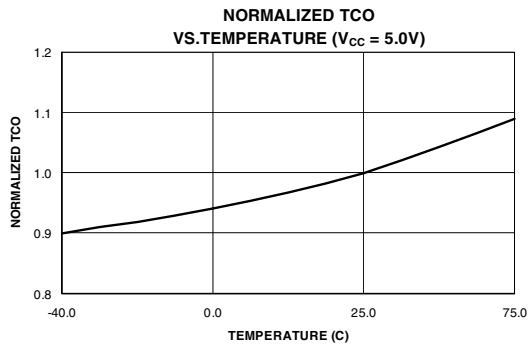
Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching Current High (Test High)	$0 < V_{OUT} \leq 1.4$	-44		mA
		$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
		$V_{OUT} = 3.1V$		-142	μA
$I_{OL(AC)}$	Switching Current Low (Test Point)	$V_{OUT} > 2.2V$	95		mA
		$2.2 > V_{OUT} > 0$	$V_{OUT}/0.023$		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
		$V_{OUT} = 0.71$		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V load	0.5	3	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V load	0.5	3	V/ns

- Notes:
- Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
 - Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

ATF1504AS Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead J-lead	68-lead J-lead	84-lead J-lead	100-lead PQFP	100-lead TQFP
INPUT/OE2/GCLK2	40	2	2	2	92	90
INPUT/GCLR	39	1	1	1	91	89
INPUT/OE1	38	44	68	84	90	88
INPUT/GCLK1	37	43	67	83	89	87
I/O /GCLK3	35	41	65	81	87	85
I/O/PD (1,2)	5, 19	11, 25	17, 37	20, 46	14, 44	12, 42
I/O/TDI (JTAG)	1	7	12	14	6	4
I/O/TMS (JTAG)	7	13	19	23	17	15
I/O/TCK (JTAG)	26	32	50	62	64	62
I/O/TDO (JTAG)	32	38	57	71	75	73
GND	4, 16, 24, 36	10, 22, 30, 42	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86, 95
V _{CCINT}	9, 17, 29, 41	3, 15, 23, 35	3, 35	3, 43	41, 93	39, 91
V _{CCIO}	—	—	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	3, 18, 34, 51, 66, 82
N/C	—	—	—	—	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	52	68	68	68
# User I/O Pins	32	32	48	64	64	64

OE (1, 2) Global OE Pins
 GCLR Global Clear Pin
 GCLK (1, 2, 3) Global Clock Pins
 PD (1, 2) Power down pins
 TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming
 GND Ground Pins
 V_{CCINT} VCC pins for the device (+5V - Internal)
 V_{CCIO} VCC pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)



ATF1504AS Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1504AS-7 AC44 ATF1504AS-7 JC44 ATF1504AS-7 JC68 ATF1504AS-7 JC84 ATF1504AS-7 QC100 ATF1504AS-7 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AC44 ATF1504AS-10 JC44 ATF1504AS-10 JC68 ATF1504AS-10 JC84 ATF1504AS-10 QC100 ATF1504AS-10 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AI44 ATF1504AS-10 JI44 ATF1504AS-10 JI68 ATF1504AS-10 JI84 ATF1504AS-10 QI100 ATF1504AS-10 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)
15	8	100	ATF1504AS-15 AC44 ATF1504AS-15 JC44 ATF1504AS-15 JC68 ATF1504AS-15 JC84 ATF1504AS-15 QC100 ATF1500AS-15 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
15	8	100	ATF1504AS-15 AI44 ATF1504AS-15 JI44 ATF1504AS-15 JI68 ATF1504AS-15 JI84 ATF1504AS-15 QI100 ATF1504AS-15 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

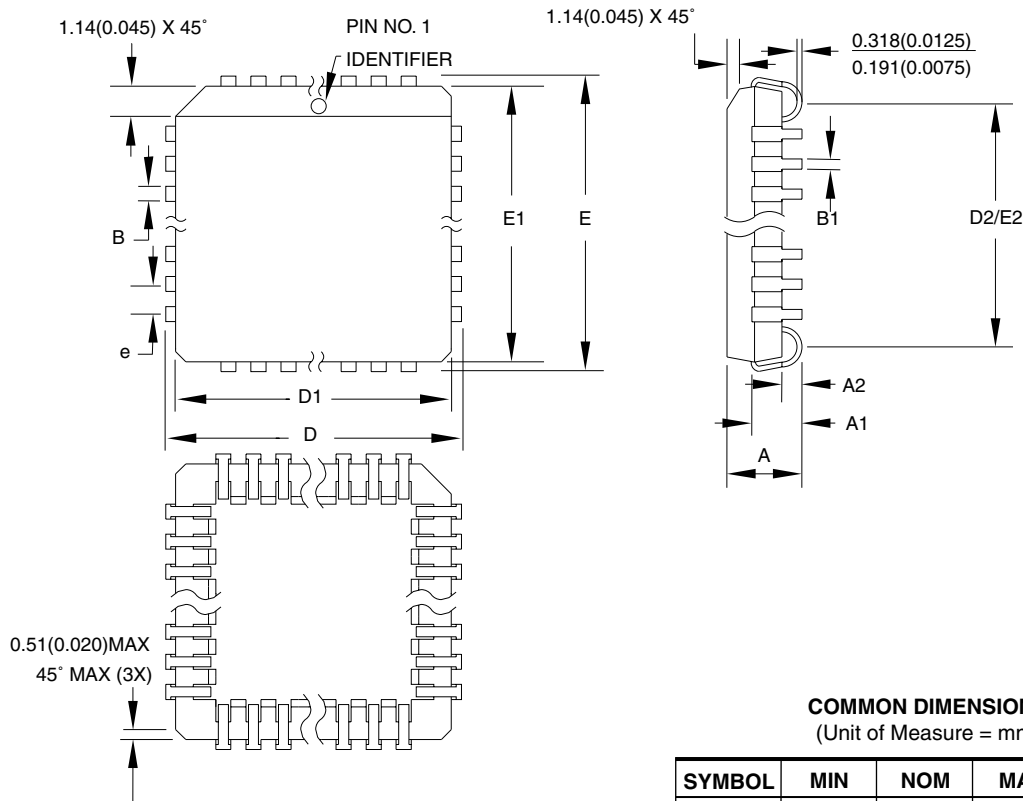
ATF1504ASL Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1504ASL-20 AC44 ATF1504ASL-20 JC44 ATF1504ASL-20 JC68 ATF1504ASL-20 JC84 ATF1504ASL-20 QC100 ATF1504ASL-20 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
25	15	70	ATF1504ASL-25 AI44 ATF1504ASL-25 JI84 ATF1504ASL-25 JI68 ATF1504ASL-25 JI84 ATF1504ASL-25 QI100 ATF1504ASL-25 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

68J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	25.019	—	25.273	
D1	24.130	—	24.333	Note 2
E	25.019	—	25.273	
E1	24.130	—	24.333	Note 2
D2/E2	22.606	—	23.622	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

68J, 68-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

68J

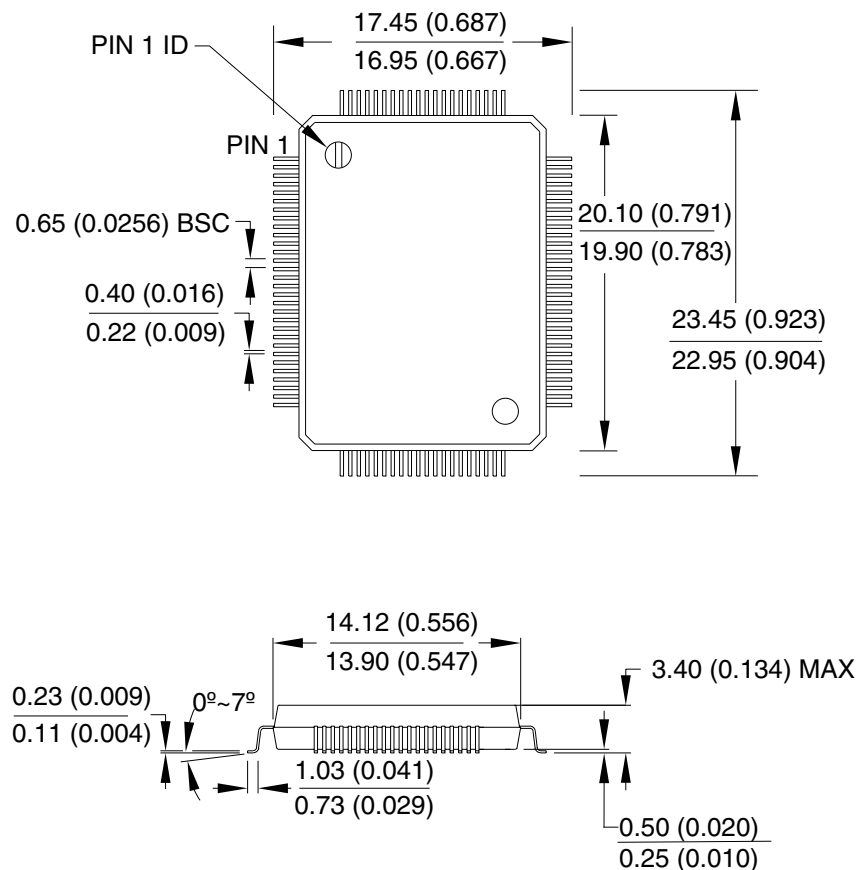
REV.

B



100Q1 – PQFP

Dimensions in Millimeters and (Inches)*
 *Controlling dimensions: millimeters
 JEDEC STANDARD MS-022, GC-1



04/11/2001



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

100Q1, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch,
 Plastic Quad Flat Package (PQFP)

DRAWING NO.

100Q1

REV.

A

