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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

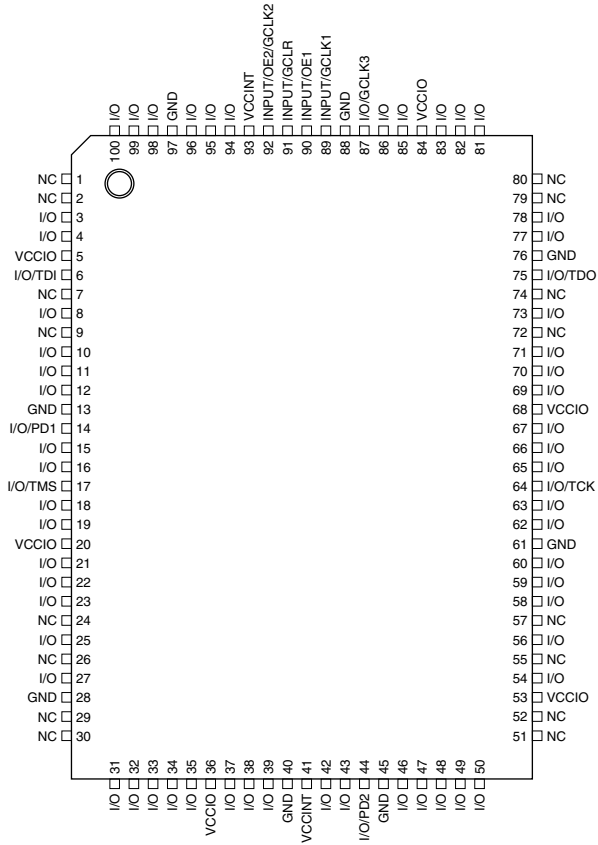
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

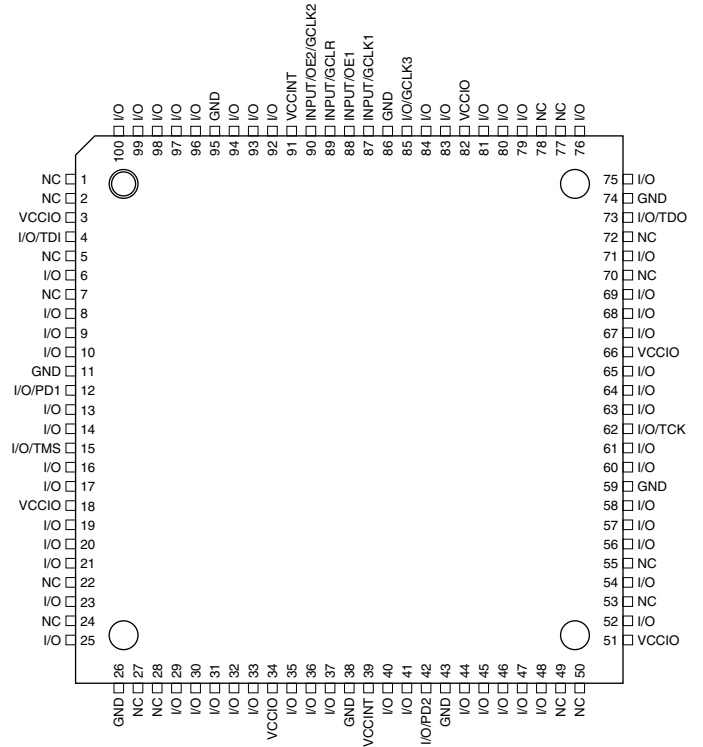
Details

Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-7ax44

**100-lead PQFP
Top View**



**100-lead TQFP
Top View**



Description

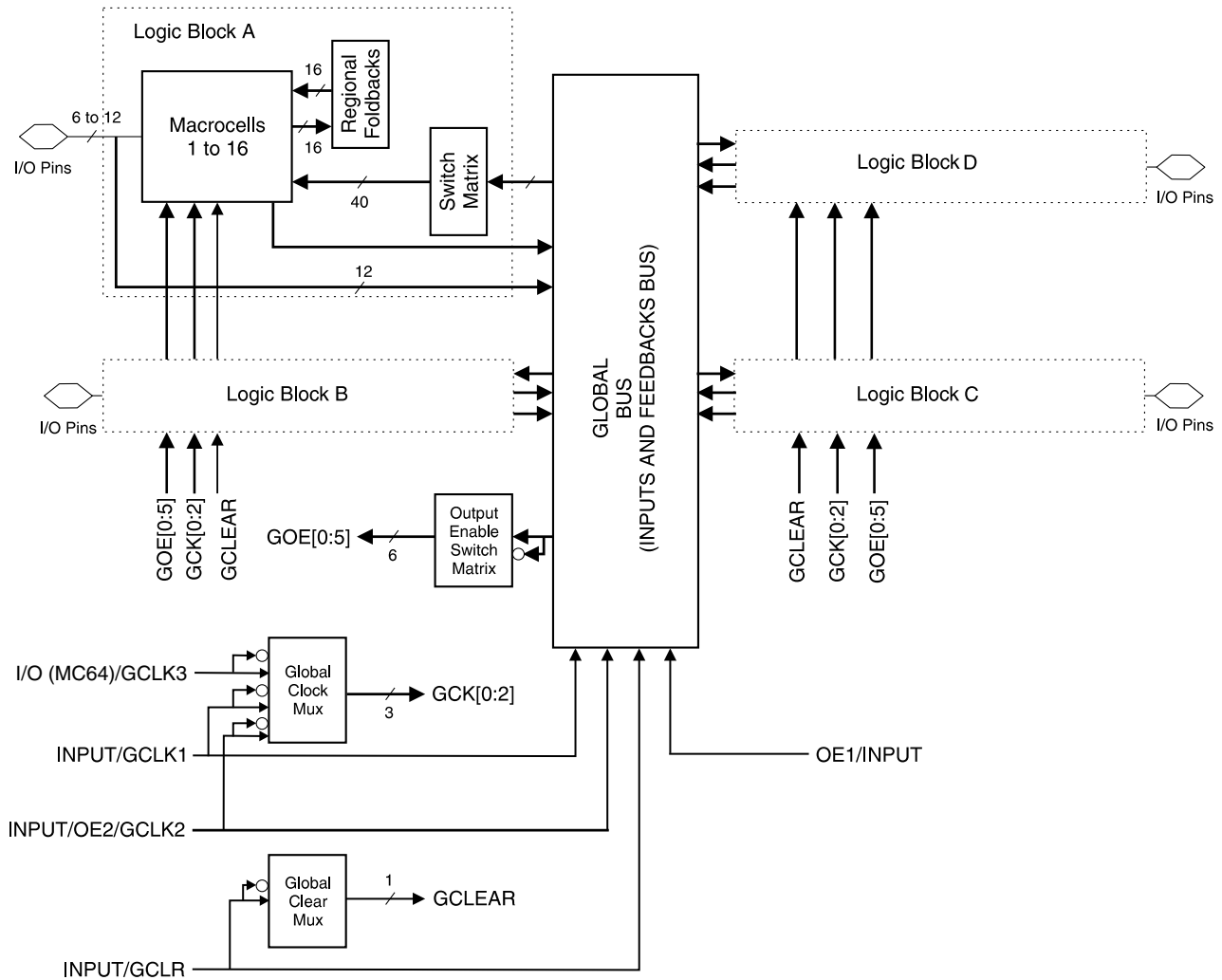
The ATF1504AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504AS's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504AS has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504AS allows fast, efficient generation of complex logic functions. The ATF1504AS contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Block Diagram



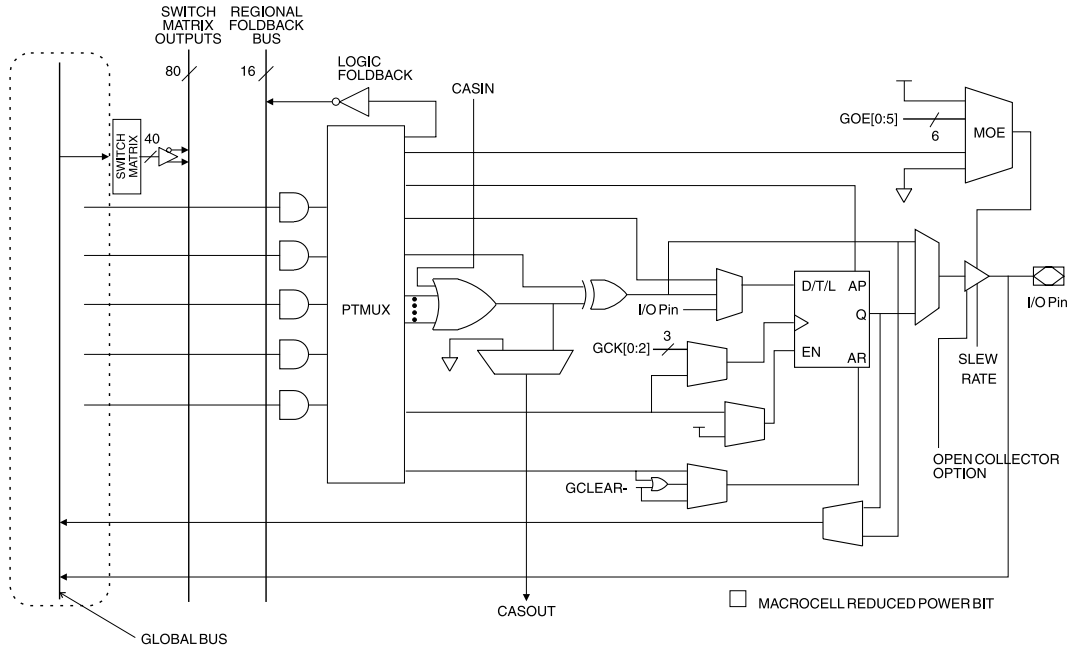
Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The sixteen foldback terms in each region allow generation of high fan-in sum terms (up to sixteen product terms) with a nominal additional delay.

Figure 1. ATF1504AS Macrocell



All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced Power Bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{ACH} and t_{SEXP} .

The ATF1504AS macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned-down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1504AS designs are supported by several industry-standard third-party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

Power-up Reset

The ATF1504AS is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D .

The ATF1504AS has two options for the hysteresis about the reset level, V_{RST} , Small and Large. During the fitting process users may configure the device with the Power-up Reset hysteresis set to Large or Small. Atmel POF2JED users may select the Large option by including the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504AS fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

Programming

ATF1504AS devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504AS devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1504AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504AS is being programmed via ISP.

All ATF1504AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20 ns.

AC Characteristics

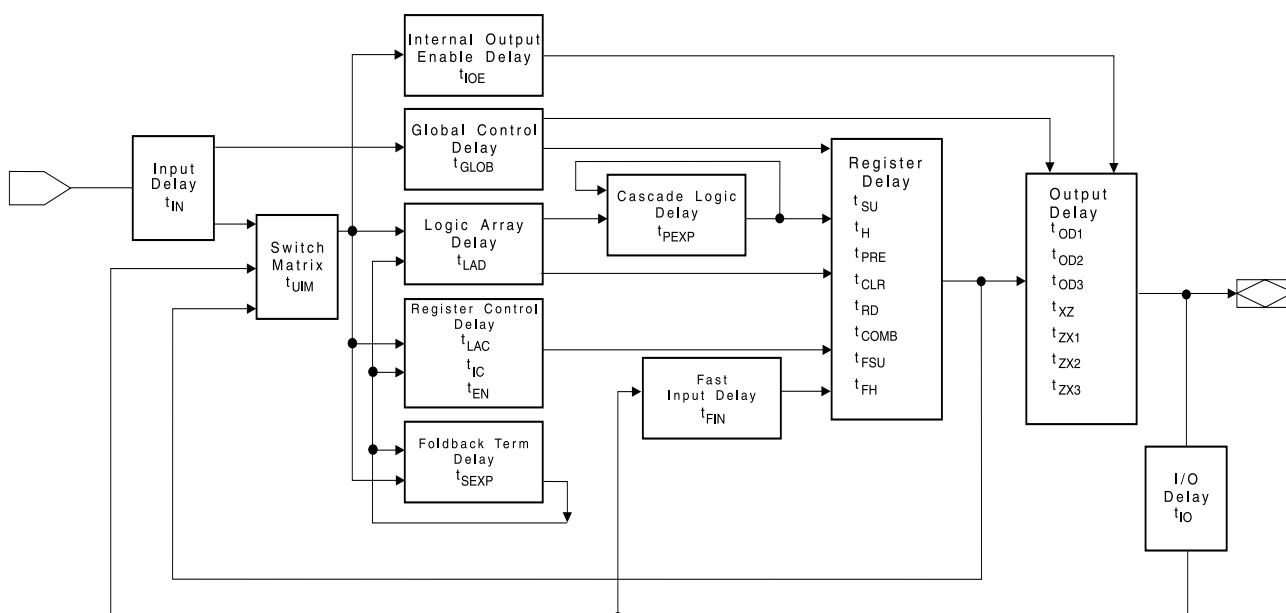
Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		ns
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	166.7		125		100		83.3		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{\text{CCIO}} = 5\text{V}$; $C_{\text{L}} = 35\text{ pF}$)		2		1.5		4		5		6	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{\text{CCIO}} = 3.3\text{V}$; $C_{\text{L}} = 35\text{ pF}$)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; $V_{\text{CCIO}} = 5\text{V}$ or 3.3V ; $C_{\text{L}} = 35\text{ pF}$)		5		5.5		8		10		10	ns

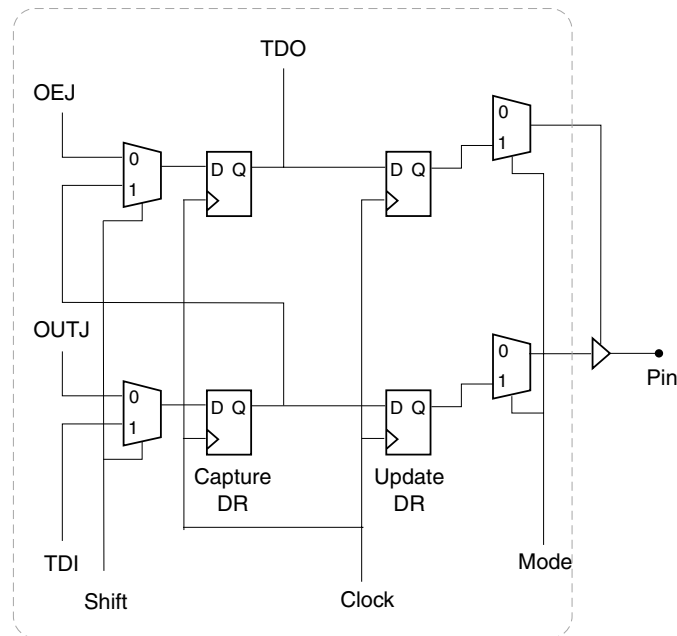
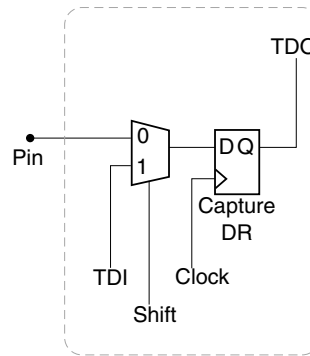
Note: See ordering information for valid part numbers.

Timing Model



BSC Configuration for Macrocell

Pin BSC

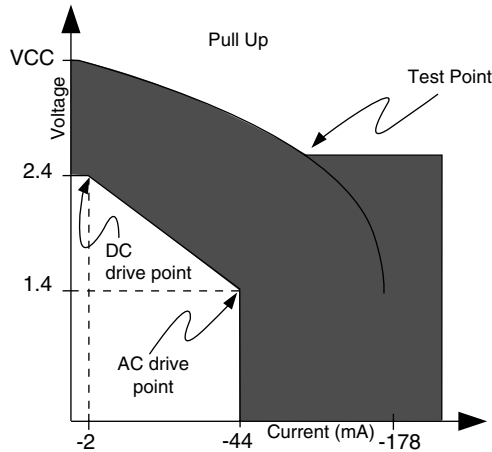


Macrocell BSC

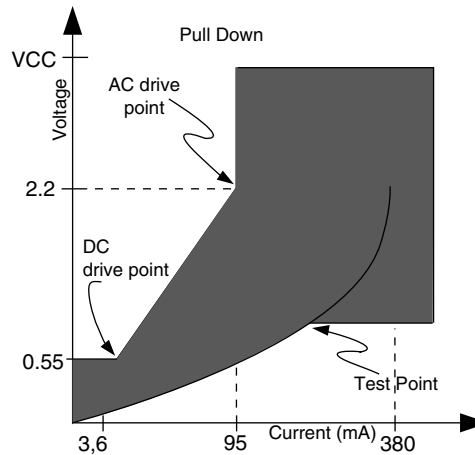
PCI Compliance

The ATF1504AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS allows this without contributing to system noise while delivering low output-to-output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance. The PCI electrical characteristics appear on the next page.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



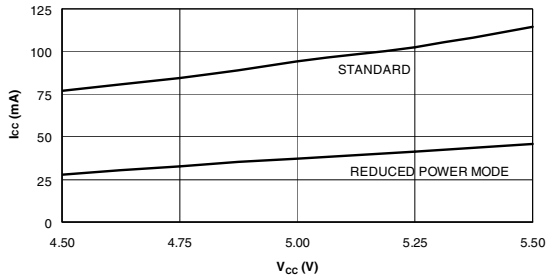
PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



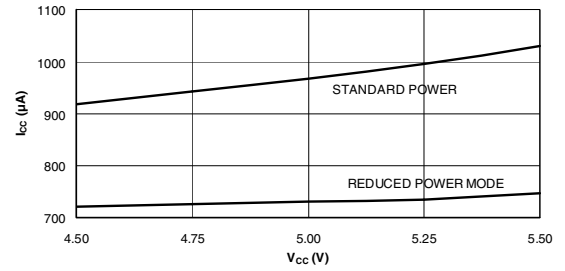
ATF1504AS I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP
1	A	12	6	18	22	16	14	33	C	24	18	36	44	42	40
2	A	—	—	—	21	15	13	34	C	—	—	—	45	43	41
3	A/ PD1	11	5	17	20	14	12	35	C/ PD2	25	19	37	46	44	42
4	A	9	3	15	18	12	10	36	C	26	20	39	48	46	44
5	A	8	2	14	17	11	9	37	C	27	21	40	49	47	45
6	A	—	—	13	16	10	8	38	C	—	—	41	50	48	46
7	A	—	—	—	15	8	6	39	C	—	—	—	51	49	47
8/ TDI	A	7	1	12	14	6	4	40	C	28	22	42	52	50	48
9	A	—	—	10	12	4	100	41	C	29	23	44	54	54	52
10	A	—	—	—	11	3	99	42	C	—	—	—	55	56	54
11	A	6	44	9	10	100	98	43	C	—	—	45	56	58	56
12	A	—	—	8	9	99	97	44	C	—	—	46	57	59	57
13	A	—	—	7	8	98	96	45	C	—	—	47	58	60	58
14	A	5	43	5	6	96	94	46	C	31	25	49	60	62	60
15	A	—	—	—	5	95	93	47	C	—	—	—	61	63	61
16	A	4	42	4	4	94	92	48/ TCK	C	32	26	50	62	64	62
17	B	21	15	33	41	39	37	49	D	33	27	51	63	65	63
18	B	—	—	—	40	38	36	50	D	—	—	—	64	66	64
19	B	20	14	32	39	37	35	51	D	34	28	52	65	67	65
20	B	19	13	30	37	35	33	52	D	36	30	54	67	69	67
21	B	18	12	29	36	34	32	53	D	37	31	55	68	70	68
22	B	—	—	28	35	33	31	54	D	—	—	56	69	71	69
23	B	—	—	—	34	32	30	55	D	—	—	—	70	73	71
24	B	17	11	27	33	31	29	56/ TDO	D	38	32	57	71	75	73
25	B	16	10	25	31	27	25	57	D	39	33	59	73	77	75
26	B	—	—	—	30	25	23	58	D	—	—	—	74	78	76
27	B	—	—	24	29	23	21	59	D	—	—	60	75	81	79
28	B	—	—	23	28	22	20	60	D	—	—	61	76	82	80
29	B	—	—	22	27	21	19	61	D	—	—	62	77	83	81
30	B	14	8	20	25	19	17	62	D	40	34	64	79	85	83
31	B	—	—	—	24	18	16	63	D	—	—	—	80	86	84
32/ TMS	B	13	7	19	23	17	15	64	D/ GCLK3	41	35	65	81	87	85

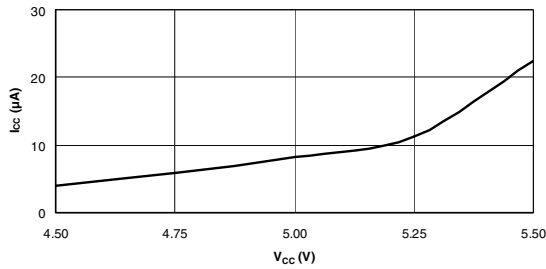
SUPPLY CURRENT VS. SUPPLY VOLTAGE
($T_A = 25^\circ\text{C}$, $F = 0$)



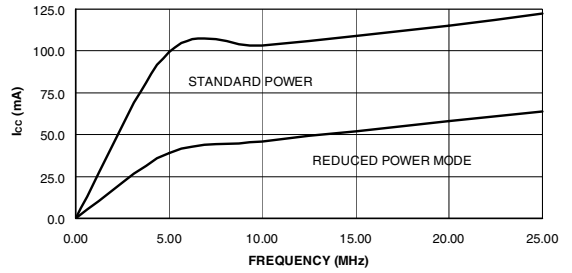
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
($T_A = 25^\circ\text{C}$, $F = 0$)



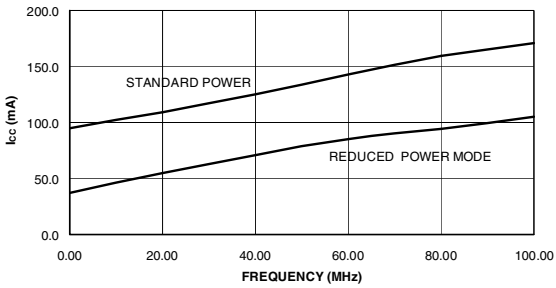
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW-POWER ("L") VERSION
($T_A = 25^\circ\text{C}$, $F = 0$)



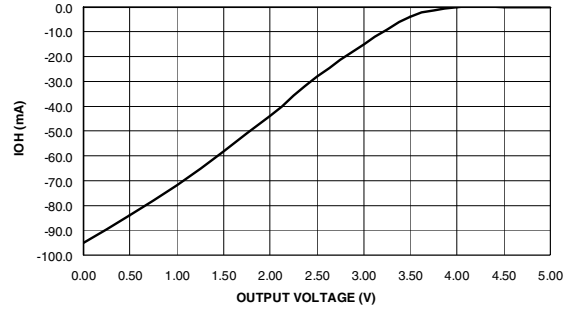
SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION
LOW POWER ($T_A = 25^\circ\text{C}$)



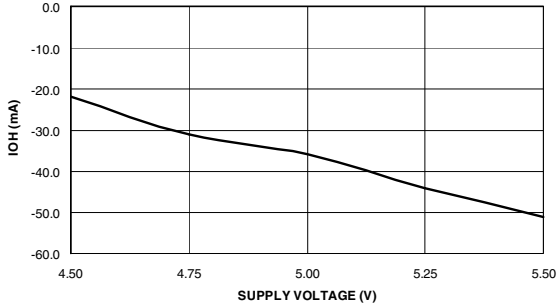
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER ($T_A = 25^\circ\text{C}$)



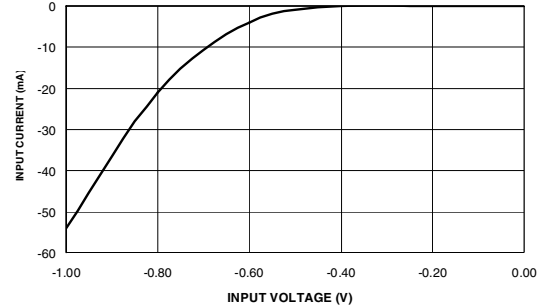
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE
($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)



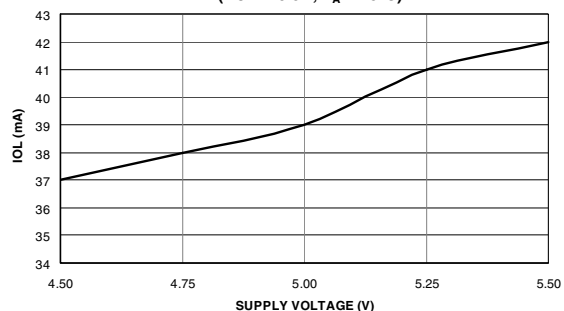
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE
($V_{OH} = 2.4\text{V}$, $T_A = 25^\circ\text{C}$)



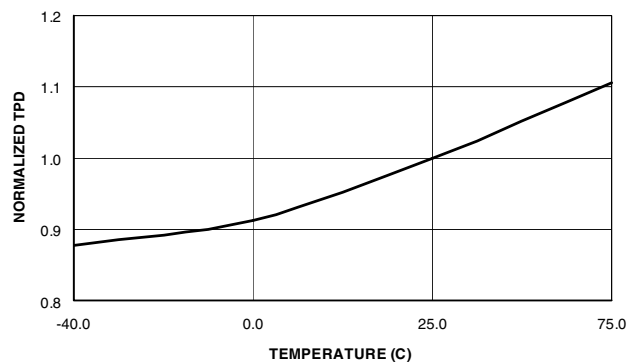
INPUT CLAMP CURRENT VS. INPUT VOLTAGE
($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)



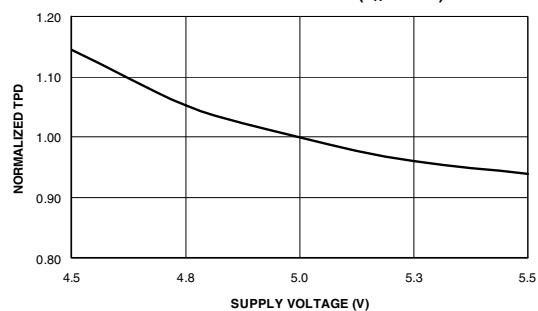
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE
($V_{OL} = 0.5V$, $T_A = 25^\circ C$)



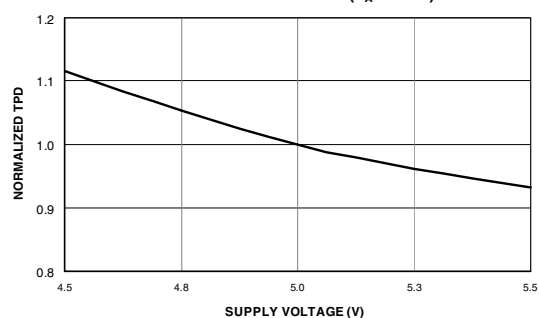
NORMALIZED TPD
VS. TEMPERATURE ($V_{CC} = 5.0V$)



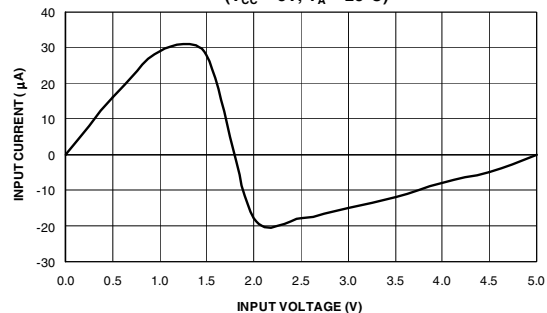
NORMALIZED TPD
VS. SUPPLY VOLTAGE ($T_A = 25^\circ C$)



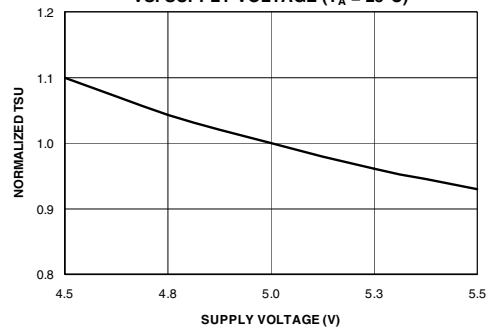
NORMALIZED TCO
VS. SUPPLY VOLTAGE ($T_A = 25^\circ C$)



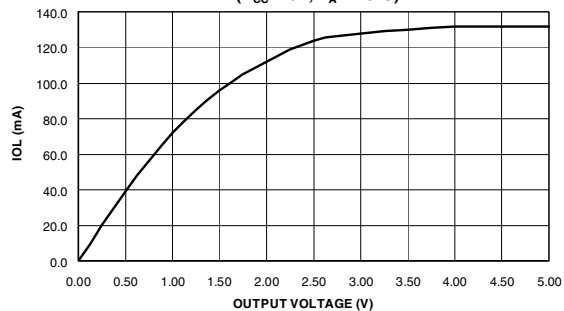
INPUT CURRENT VS. INPUT VOLTAGE
($V_{CC} = 5V$, $T_A = 25^\circ C$)

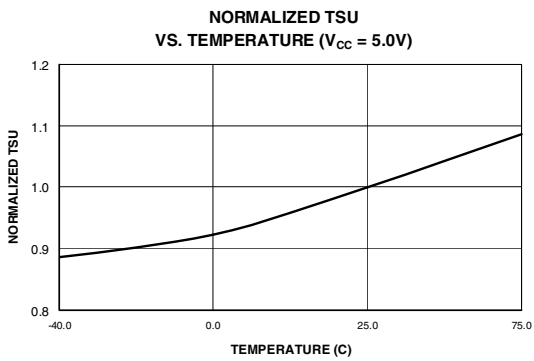
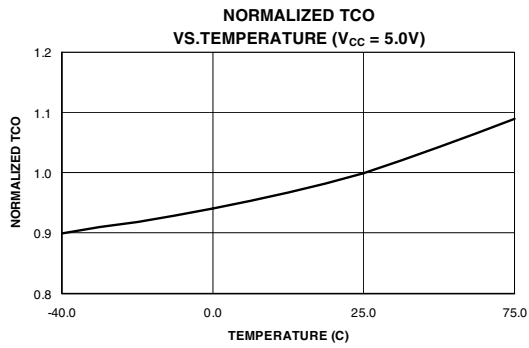


NORMALIZED TSU
VS. SUPPLY VOLTAGE ($T_A = 25^\circ C$)



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
($V_{CC} = 5V$, $T_A = 25^\circ C$)





ATF1504ASL Ordering Information

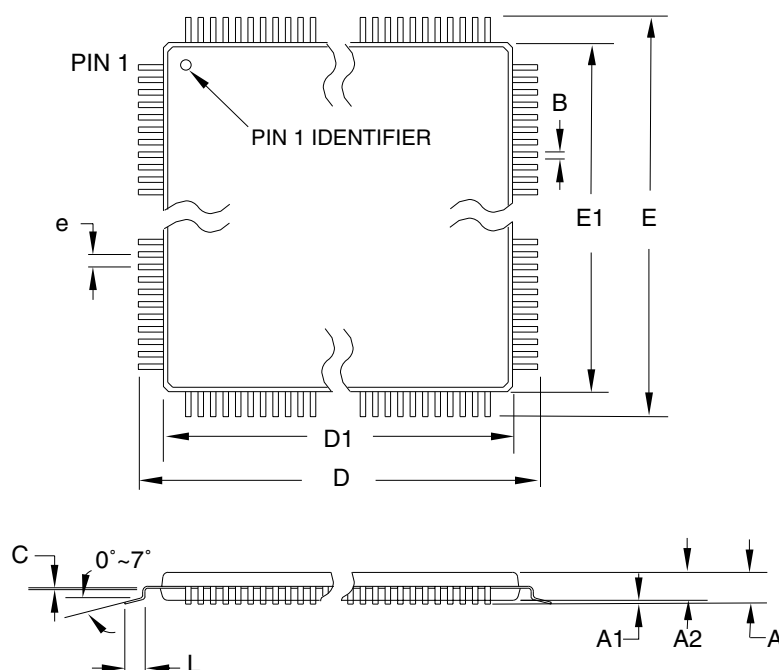
t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1504ASL-20 AC44 ATF1504ASL-20 JC44 ATF1504ASL-20 JC68 ATF1504ASL-20 JC84 ATF1504ASL-20 QC100 ATF1504ASL-20 AC100	44A 44J 68J 84J 100Q1 100A	Commercial (0°C to 70°C)
25	15	70	ATF1504ASL-25 AI44 ATF1504ASL-25 JI84 ATF1504ASL-25 JI68 ATF1504ASL-25 JI84 ATF1504ASL-25 QI100 ATF1504ASL-25 AI100	44A 44J 68J 84J 100Q1 100A	Industrial (-40°C to +85°C)

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

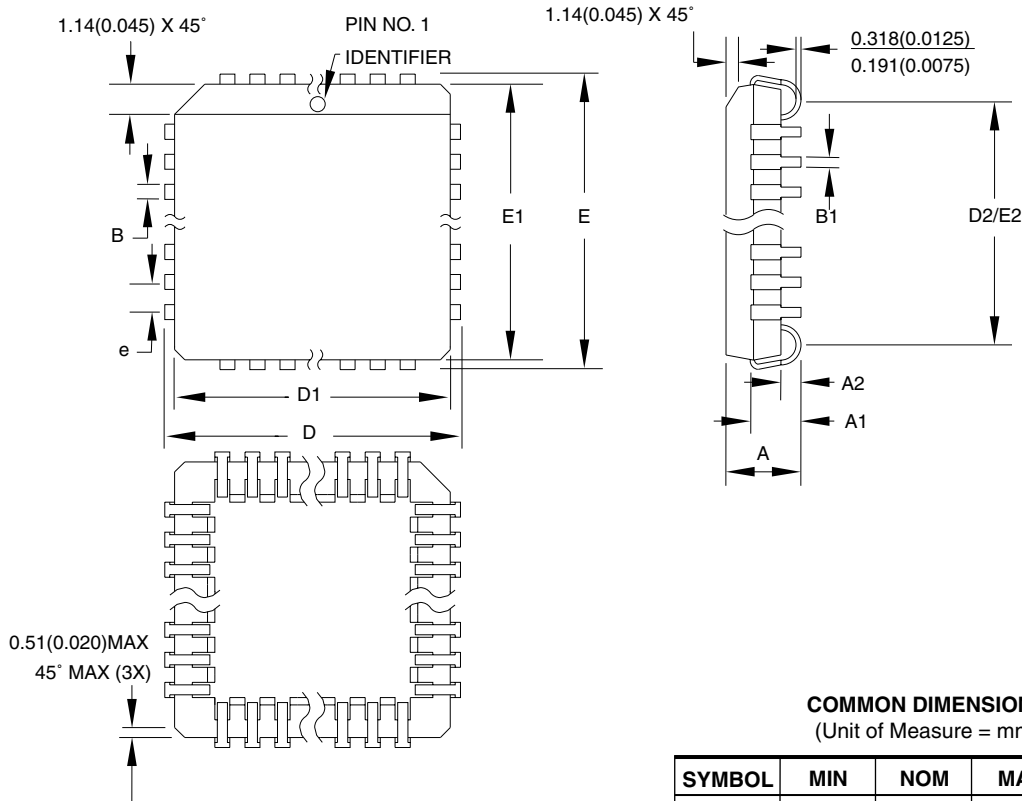
44A

REV.

B



44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	17.399	—	17.653	
D1	16.510	—	16.662	Note 2
E	17.399	—	17.653	
E1	16.510	—	16.662	Note 2
D2/E2	14.986	—	16.002	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

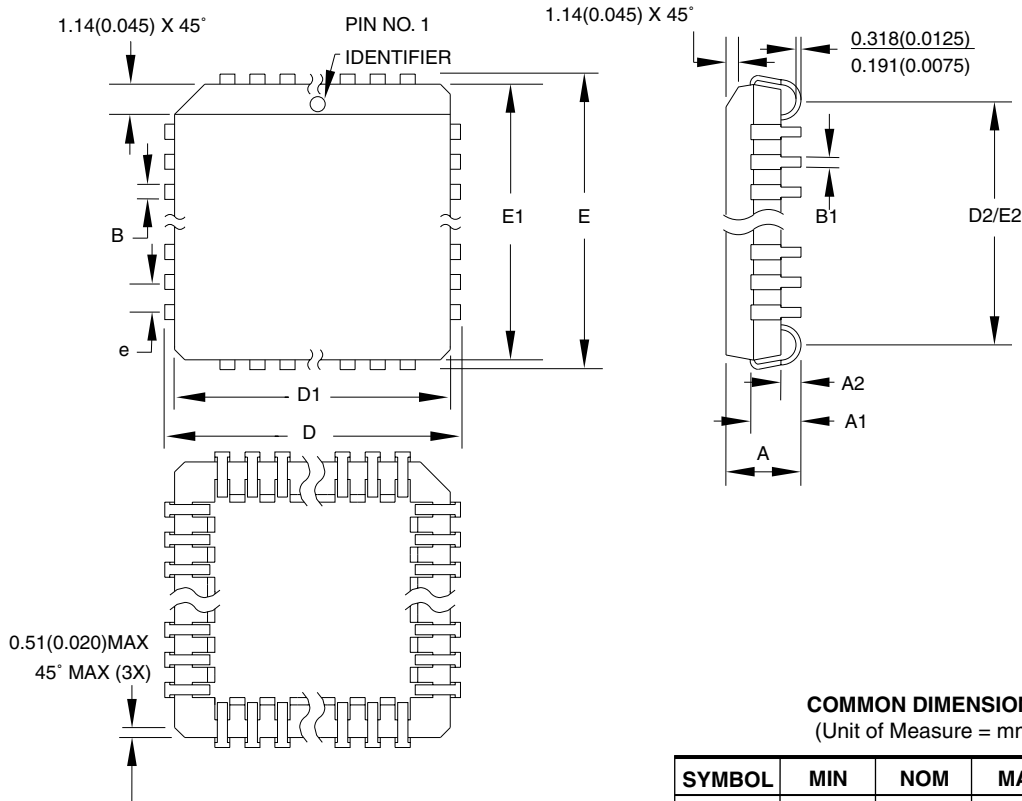
DRAWING NO.

44J

REV.

B

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	30.099	—	30.353	
D1	29.210	—	29.413	Note 2
E	30.099	—	30.353	
E1	29.210	—	29.413	Note 2
D2/E2	27.686	—	28.702	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

84J, 84-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

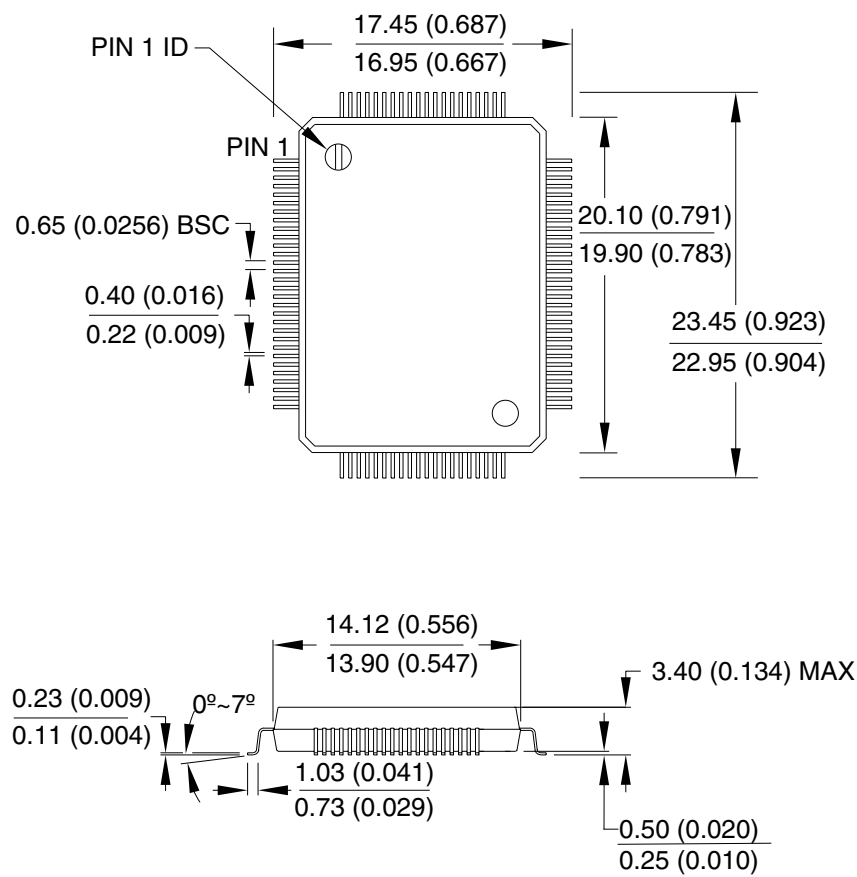
84J

REV.


B

100Q1 – PQFP

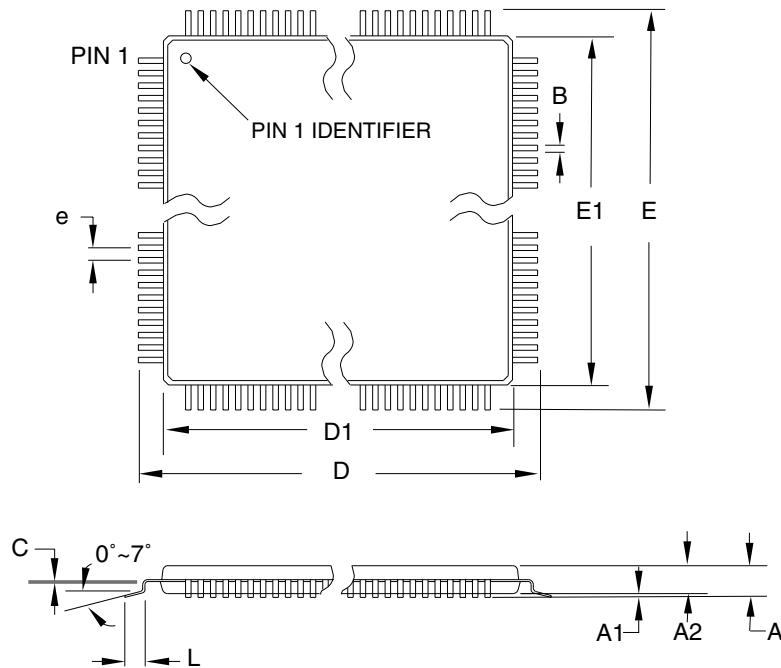
Dimensions in Millimeters and (Inches)*
 *Controlling dimensions: millimeters
 JEDEC STANDARD MS-022, GC-1



04/11/2001

 2325 Orchard Parkway San Jose, CA 95131	TITLE 100Q1 , 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	DRAWING NO. 100Q1	REV. A
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100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.08 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

100A, 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness,
0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

100A

REV.

C