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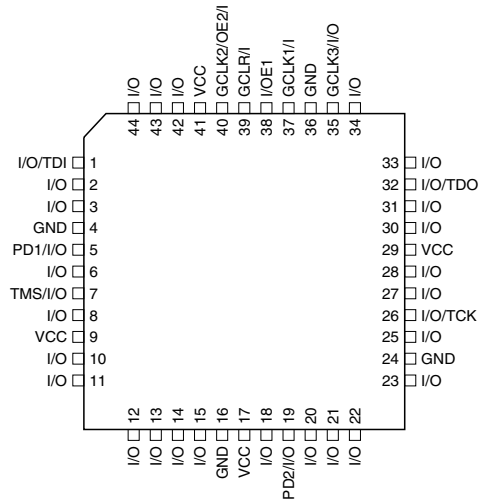
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

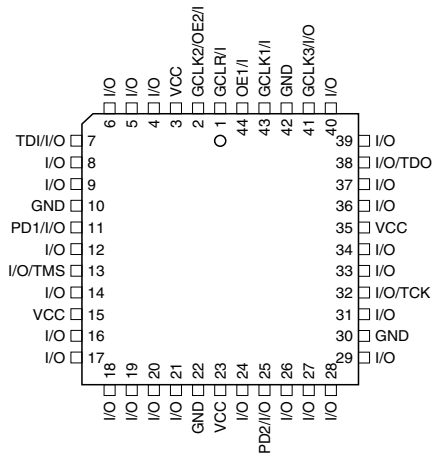
## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable (min 10K program/erase cycles) |
| Delay Time tpd(1) Max | 25 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 64 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atf1504asl-25qi100 |

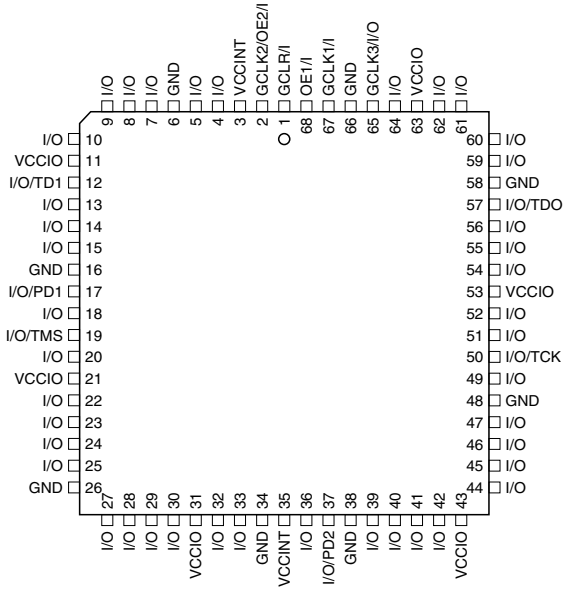
**44-lead TQFP**
**Top View**



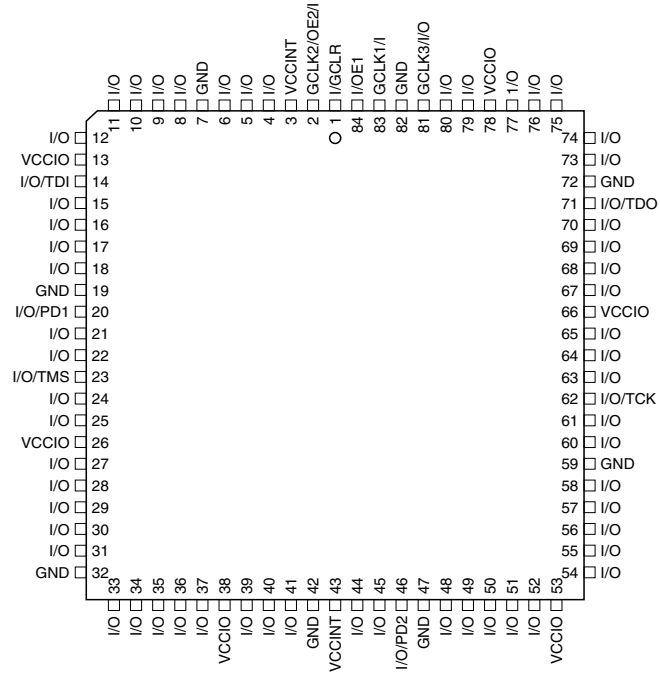

**44-lead PLCC**
**Top View**



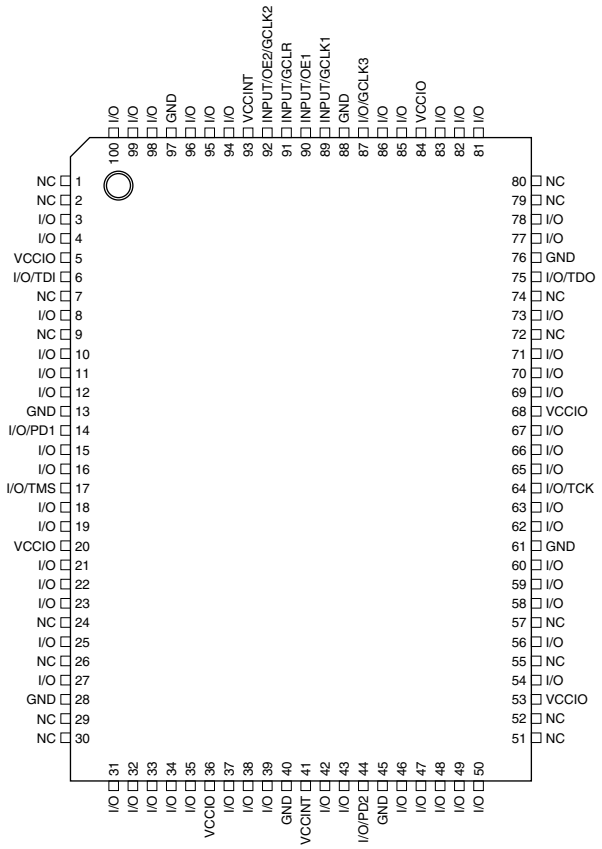

**68-lead PLCC**
**Top View**



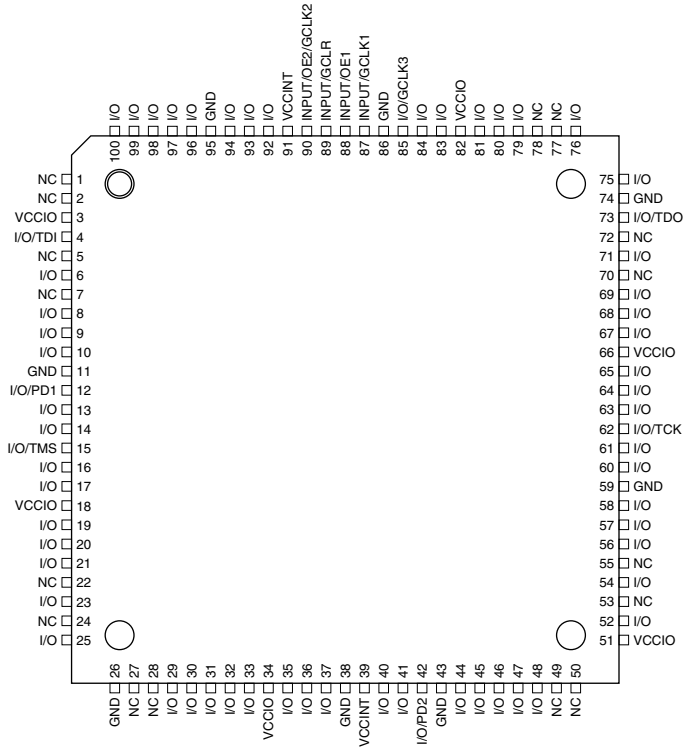

**84-lead PLCC**
**Top View**



**100-lead PQFP**
**Top View**




**100-lead TQFP**
**Top View**



## Description

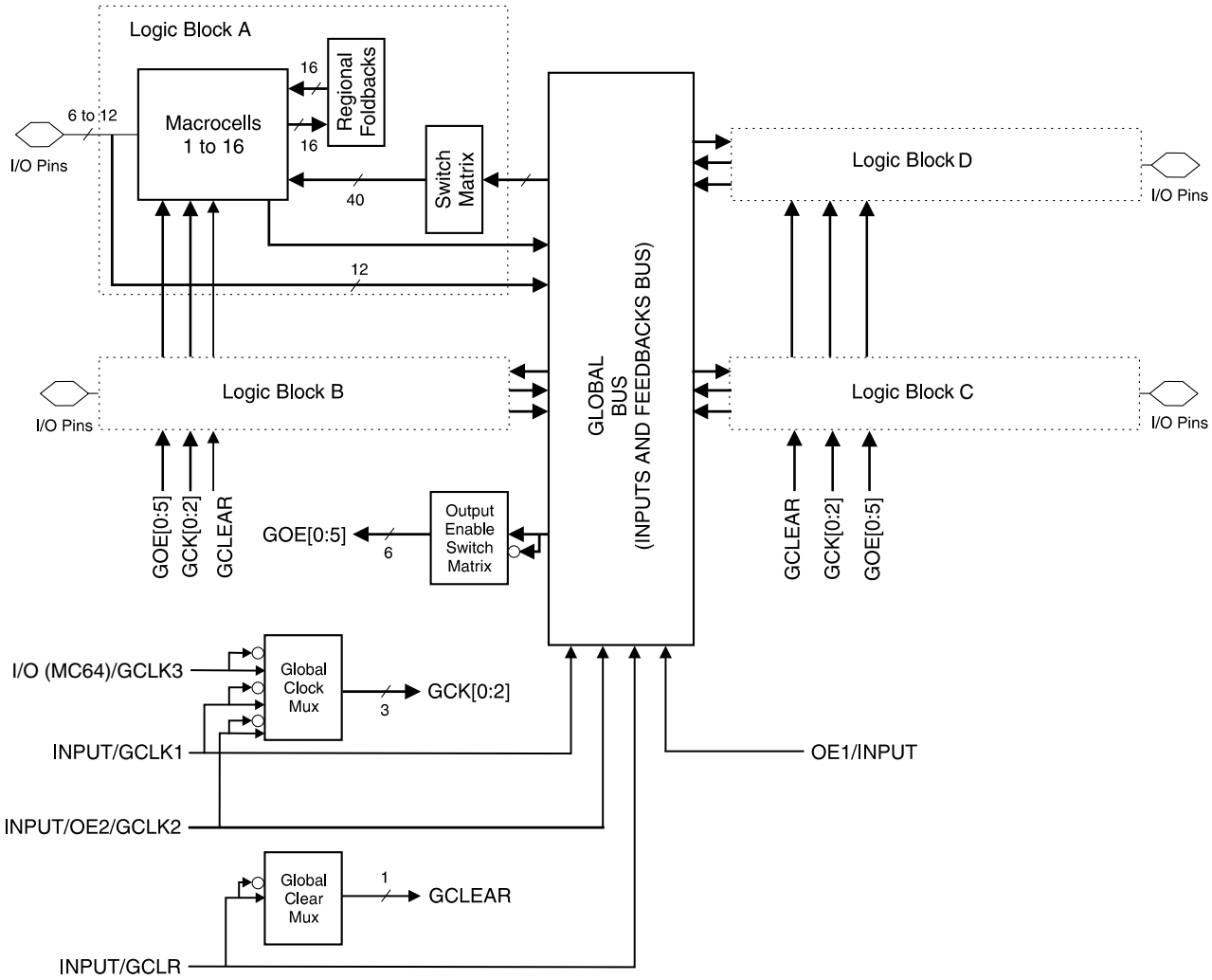
The ATF1504AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504AS's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504AS has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504AS allows fast, efficient generation of complex logic functions. The ATF1504AS contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

## Block Diagram




Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

**Product Terms and Select Mux**

Each ATF1504AS macrocell has five product terms. Each product term receives as its possible inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

**OR/XOR/CASCADE Logic**

The ATF1504AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a little small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

**Flip-flop**

The ATF1504AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either one of the Global CLK Signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

**Output Select and Enable**

The ATF1504AS macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.

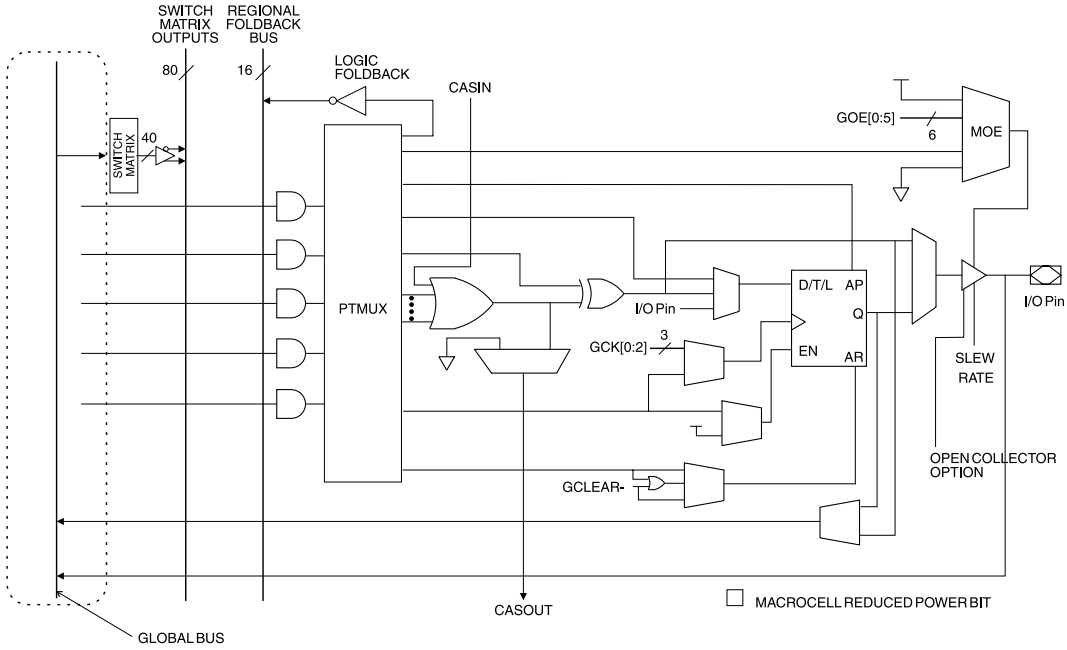
**Global Bus/Switch Matrix**

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its possible inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

**Foldback Bus**

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The sixteen foldback terms in each region allow generation of high fan-in sum terms (up to sixteen product terms) with a nominal additional delay.

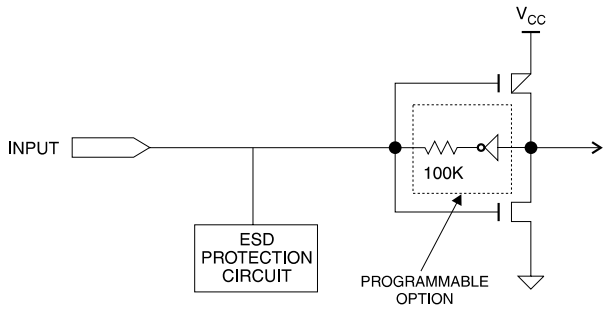
**Figure 1.** ATF1504AS Macrocell



## Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504AS offers the option of programming all input and I/O pins so that pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

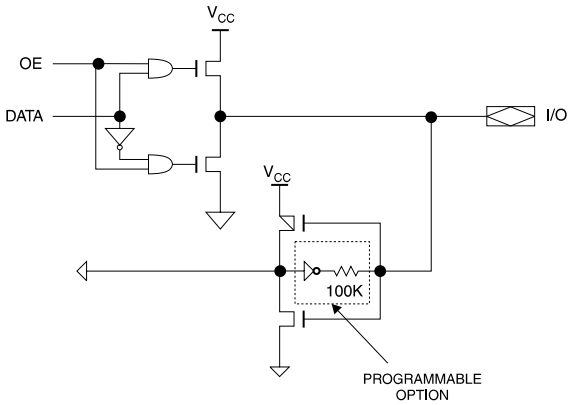
## Input Diagram




## Speed/Power Management

The ATF1504AS has several built-in speed and power management features. The ATF1504AS contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

## I/O Diagram




To further reduce power, each ATF1504AS macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504AS also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power-down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

## Programming

ATF1504AS devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504AS devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

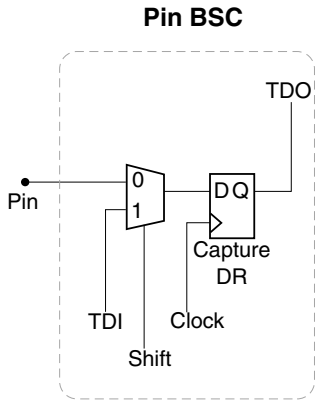
## ISP Programming Protection

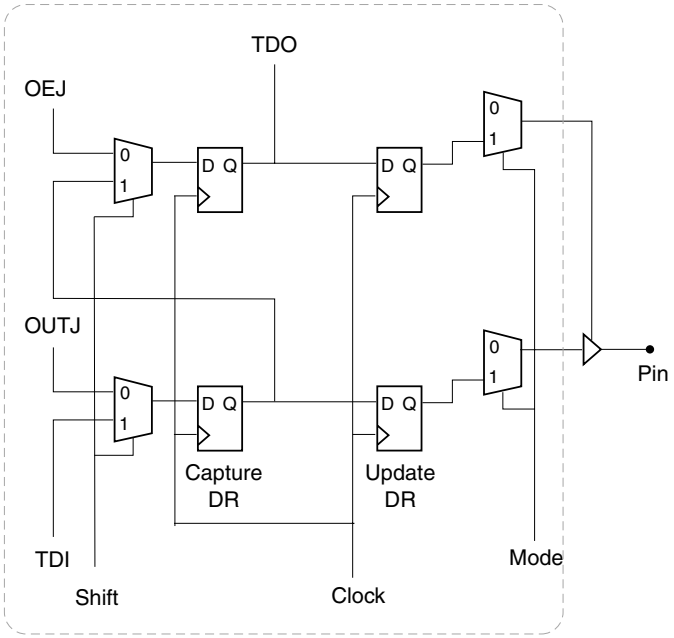
The ATF1504AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504AS is being programmed via ISP.

All ATF1504AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

## BSC Configuration for Macrocell



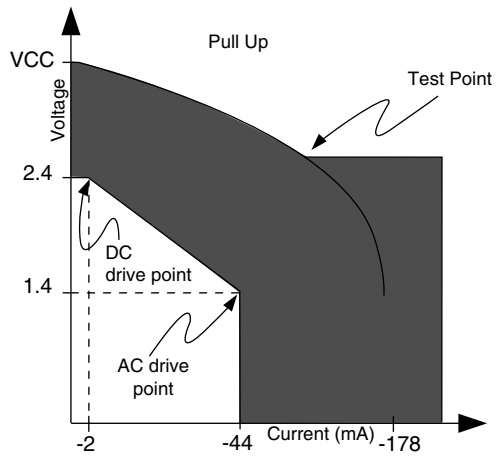




**Macrocell BSC**

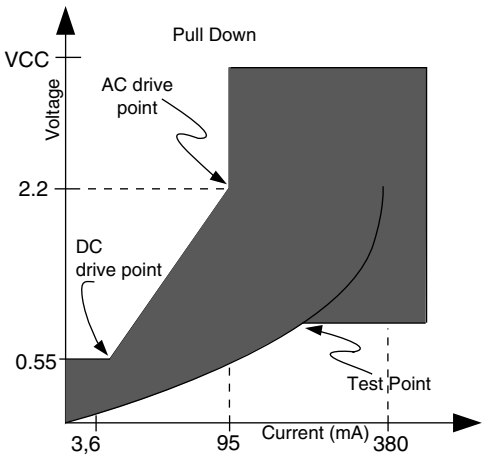
## PCI Compliance

The ATF1504AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS allows this without contributing to system noise while delivering low output-to-output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance. The PCI electrical characteristics appear on the next page.

## PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode




## PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



## PCI DC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5.25 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage | | -0.5 | 0.8 | V |
| $I_{IH}$ | Input High Leakage Current | $V_{IN}$ = 2.7V | | 70 | µA |
| $I_{IL}$ | Input Low Leakage Current | $V_{IN}$ = 0.5V | | -70 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = -2 mA | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 3 mA, 6 mA | | 0.55 | V |
| $C_{IN}$ | Input Pin Capacitance | | | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | | 12 | pF |
| $C_{IDSEL}$ | IDSEL Pin Capacitance | | | 8 | pF |
| $L_{PIN}$ | Pin Inductance | | | 20 | nH |

Note: Leakage current is with pin-keeper off.

## PCI AC Characteristics

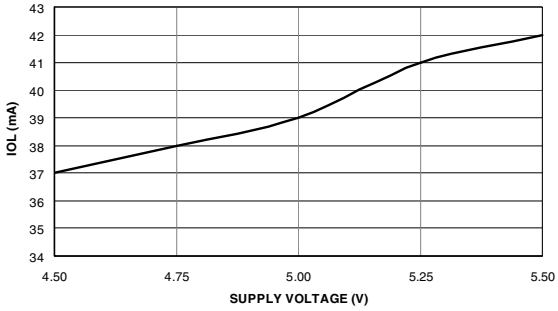
| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High (Test High) | $0 < V_{OUT} \leq 1.4$ | -44 | | mA |
| | | $1.4 < V_{OUT} < 2.4$ | $-44+(V_{OUT} - 1.4)/0.024$ | | mA |
| | | $3.1 < V_{OUT} < V_{CC}$ | | Equation A | mA |
| | | $V_{OUT}$ = 3.1V | | -142 | µA |
| $I_{OL(AC)}$ | Switching Current Low (Test Point) | $V_{OUT} > 2.2V$ | 95 | | mA |
| | | $2.2 > V_{OUT} > 0$ | $V_{OUT}/0.023$ | | mA |
| | | $0.1 > V_{OUT} > 0$ | | Equation B | mA |
| | | $V_{OUT}$ = 0.71 | | 206 | mA |
| $I_{CL}$ | Low Clamp Current | $-5 < V_{IN} \leq -1$ | $-25+(V_{IN} + 1)/0.015$ | | mA |
| $SLEW_R$ | Output Rise Slew Rate | 0.4V to 2.4V load | 0.5 | 3 | V/ns |
| $SLEW_F$ | Output Fall Slew Rate | 2.4V to 0.4V load | 0.5 | 3 | V/ns |

Notes: 1. Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

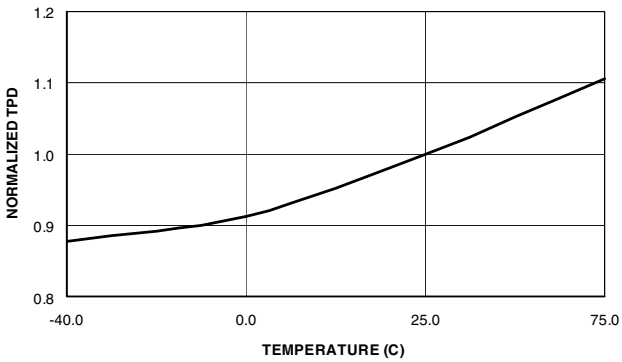
## ATF1504AS I/O Pinouts

| MC | PLC | 44-lead PLCC | 44-lead TQFP | 68-lead PLCC | 84-lead PLCC | 100-lead PQFP | 100-lead TQFP | MC | PLC | 44-lead PLCC | 44-lead TQFP | 68-lead PLCC | 84-lead PLCC | 100-lead PQFP | 100-lead TQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | A | 12 | 6 | 18 | 22 | 16 | 14 | 33 | C | 24 | 18 | 36 | 44 | 42 | 40 |
| 2 | A | – | – | – | 21 | 15 | 13 | 34 | C | – | – | – | 45 | 43 | 41 |
| 3 | A/ **PD1** | 11 | 5 | 17 | 20 | 14 | 12 | 35 | C/ **PD2** | 25 | 19 | 37 | 46 | 44 | 42 |
| 4 | A | 9 | 3 | 15 | 18 | 12 | 10 | 36 | C | 26 | 20 | 39 | 48 | 46 | 44 |
| 5 | A | 8 | 2 | 14 | 17 | 11 | 9 | 37 | C | 27 | 21 | 40 | 49 | 47 | 45 |
| 6 | A | – | – | 13 | 16 | 10 | 8 | 38 | C | – | – | 41 | 50 | 48 | 46 |
| 7 | A | – | – | – | 15 | 8 | 6 | 39 | C | – | – | – | 51 | 49 | 47 |
| 8/ **TDI** | A | 7 | 1 | 12 | 14 | 6 | 4 | 40 | C | 28 | 22 | 42 | 52 | 50 | 48 |
| 9 | A | – | – | 10 | 12 | 4 | 100 | 41 | C | 29 | 23 | 44 | 54 | 54 | 52 |
| 10 | A | – | – | – | 11 | 3 | 99 | 42 | C | – | – | – | 55 | 56 | 54 |
| 11 | A | 6 | 44 | 9 | 10 | 100 | 98 | 43 | C | – | – | 45 | 56 | 58 | 56 |
| 12 | A | – | – | 8 | 9 | 99 | 97 | 44 | C | – | – | 46 | 57 | 59 | 57 |
| 13 | A | – | – | 7 | 8 | 98 | 96 | 45 | C | – | – | 47 | 58 | 60 | 58 |
| 14 | A | 5 | 43 | 5 | 6 | 96 | 94 | 46 | C | 31 | 25 | 49 | 60 | 62 | 60 |
| 15 | A | – | – | – | 5 | 95 | 93 | 47 | C | – | – | – | 61 | 63 | 61 |
| 16 | A | 4 | 42 | 4 | 4 | 94 | 92 | 48/ **TCK** | C | 32 | 26 | 50 | 62 | 64 | 62 |
| 17 | B | 21 | 15 | 33 | 41 | 39 | 37 | 49 | D | 33 | 27 | 51 | 63 | 65 | 63 |
| 18 | B | – | – | – | 40 | 38 | 36 | 50 | D | – | – | – | 64 | 66 | 64 |
| 19 | B | 20 | 14 | 32 | 39 | 37 | 35 | 51 | D | 34 | 28 | 52 | 65 | 67 | 65 |
| 20 | B | 19 | 13 | 30 | 37 | 35 | 33 | 52 | D | 36 | 30 | 54 | 67 | 69 | 67 |
| 21 | B | 18 | 12 | 29 | 36 | 34 | 32 | 53 | D | 37 | 31 | 55 | 68 | 70 | 68 |
| 22 | B | – | – | 28 | 35 | 33 | 31 | 54 | D | – | – | 56 | 69 | 71 | 69 |
| 23 | B | – | – | – | 34 | 32 | 30 | 55 | D | – | – | – | 70 | 73 | 71 |
| 24 | B | 17 | 11 | 27 | 33 | 31 | 29 | 56/ **TDO** | D | 38 | 32 | 57 | 71 | 75 | 73 |
| 25 | B | 16 | 10 | 25 | 31 | 27 | 25 | 57 | D | 39 | 33 | 59 | 73 | 77 | 75 |
| 26 | B | – | – | – | 30 | 25 | 23 | 58 | D | – | – | – | 74 | 78 | 76 |
| 27 | B | – | – | 24 | 29 | 23 | 21 | 59 | D | – | – | 60 | 75 | 81 | 79 |
| 28 | B | – | – | 23 | 28 | 22 | 20 | 60 | D | – | – | 61 | 76 | 82 | 80 |
| 29 | B | – | – | 22 | 27 | 21 | 19 | 61 | D | – | – | 62 | 77 | 83 | 81 |
| 30 | B | 14 | 8 | 20 | 25 | 19 | 17 | 62 | D | 40 | 34 | 64 | 79 | 85 | 83 |
| 31 | B | – | – | – | 24 | 18 | 16 | 63 | D | – | – | – | 80 | 86 | 84 |
| 32/ **TMS** | B | 13 | 7 | 19 | 23 | 17 | 15 | 64 | D/ **GCLK3** | 41 | 35 | 65 | 81 | 87 | 85 |

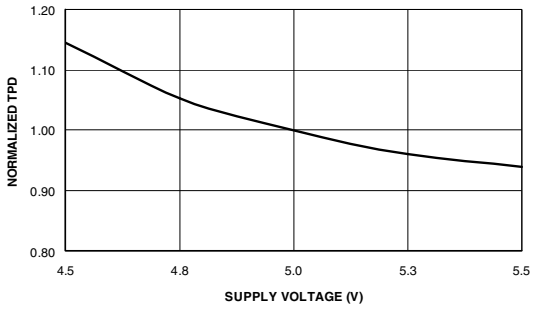
**OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE**
**(VOL = 0.5V, $T_A$ = 25°C)**



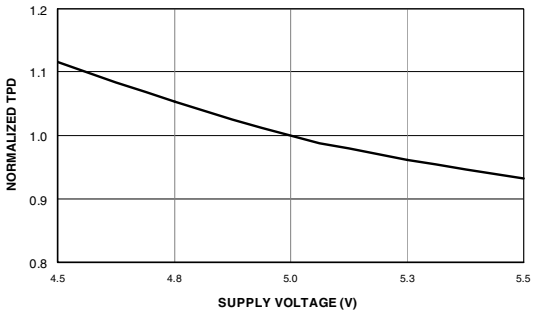

**NORMALIZED TPD**
**VS. TEMPERATURE ($V_{CC}$ = 5.0V)**



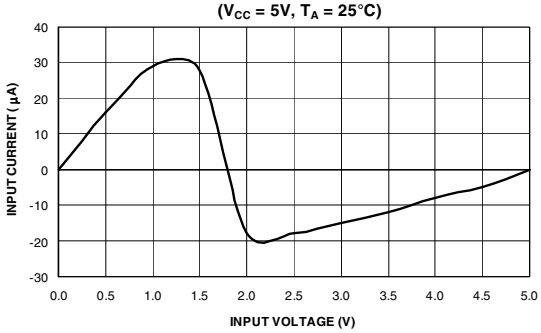

**NORMALIZED TPD**
**VS. SUPPLY VOLTAGE ($T_A$ = 25°C)**



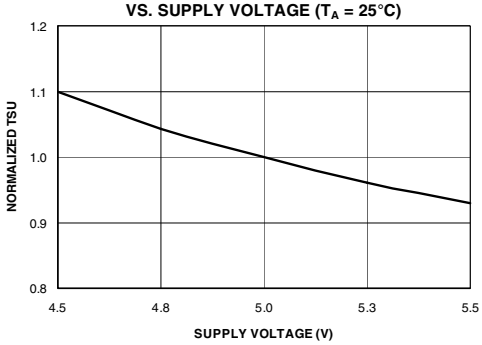

**NORMALIZED TCO**
**VS. SUPPLY VOLTAGE ($T_A$ = 25°C)**



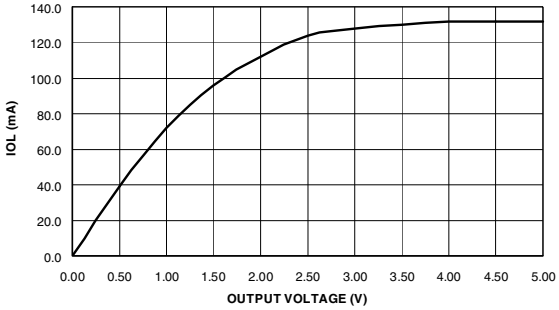

**INPUT CURRENT VS. INPUT VOLTAGE**
**($V_{CC}$ = 5V, $T_A$ = 25°C)**



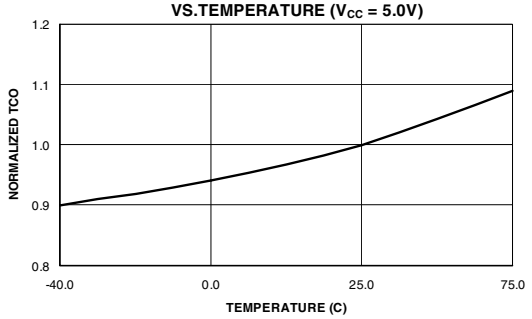

**NORMALIZED TSU**
**VS. SUPPLY VOLTAGE ($T_A$ = 25°C)**



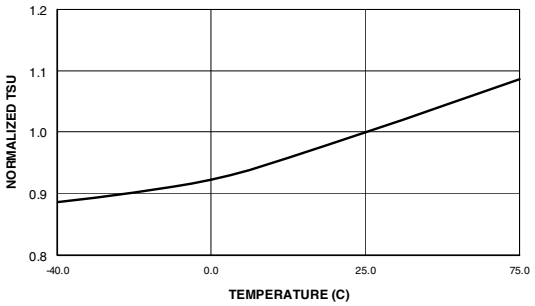

**OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE**
**($V_{CC}$ = 5V, $T_A$ = 25°C)**



**NORMALIZED TCO**
**VS.TEMPERATURE ($V_{CC}$ = 5.0V)**




**NORMALIZED TSU**
**VS. TEMPERATURE ($V_{CC}$ = 5.0V)**



## ATF1504AS Ordering Information

| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 7.5 | 4.5 | 166.7 | ATF1504AS-7 AC44 | 44A | Commercial (0°C to 70°C) |
| | | | ATF1504AS-7 JC44 | 44J | |
| | | | ATF1504AS-7 JC68 | 68J | |
| | | | ATF1504AS-7 JC84 | 84J | |
| | | | ATF1504AS-7 QC100 | 100Q1 | |
| | | | ATF1504AS-7 AC100 | 100A | |
| 10 | 5 | 125 | ATF1504AS-10 AC44 | 44A | Commercial (0°C to 70°C) |
| | | | ATF1504AS-10 JC44 | 44J | |
| | | | ATF1504AS-10 JC68 | 68J | |
| | | | ATF1504AS-10 JC84 | 84J | |
| | | | ATF1504AS-10 QC100 | 100Q1 | |
| | | | ATF1504AS-10 AC100 | 100A | |
| 10 | 5 | 125 | ATF1504AS-10 AI44 | 44A | Industrial (-40°C to +85°C) |
| | | | ATF1504AS-10 JI44 | 44J | |
| | | | ATF1504AS-10 JI68 | 68J | |
| | | | ATF1504AS-10 JI84 | 84J | |
| | | | ATF1504AS-10 QI100 | 100Q1 | |
| | | | ATF1504AS-10 AI100 | 100A | |
| 15 | 8 | 100 | ATF1504AS-15 AC44 | 44A | Commercial (0°C to 70°C) |
| | | | ATF1504AS-15 JC44 | 44J | |
| | | | ATF1504AS-15 JC68 | 68J | |
| | | | ATF1504AS-15 JC84 | 84J | |
| | | | ATF1504AS-15 QC100 | 100Q1 | |
| | | | ATF1500AS-15 AC100 | 100A | |
| 15 | 8 | 100 | ATF1504AS-15 AI44 | 44A | Industrial (-40°C to +85°C) |
| | | | ATF1504AS-15 JI44 | 44J | |
| | | | ATF1504AS-15 JI68 | 68J | |
| | | | ATF1504AS-15 JI84 | 84J | |
| | | | ATF1504AS-15 QI100 | 100Q1 | |
| | | | ATF1504AS-15 AI100 | 100A | |

## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

## ATF1504ASL Ordering Information

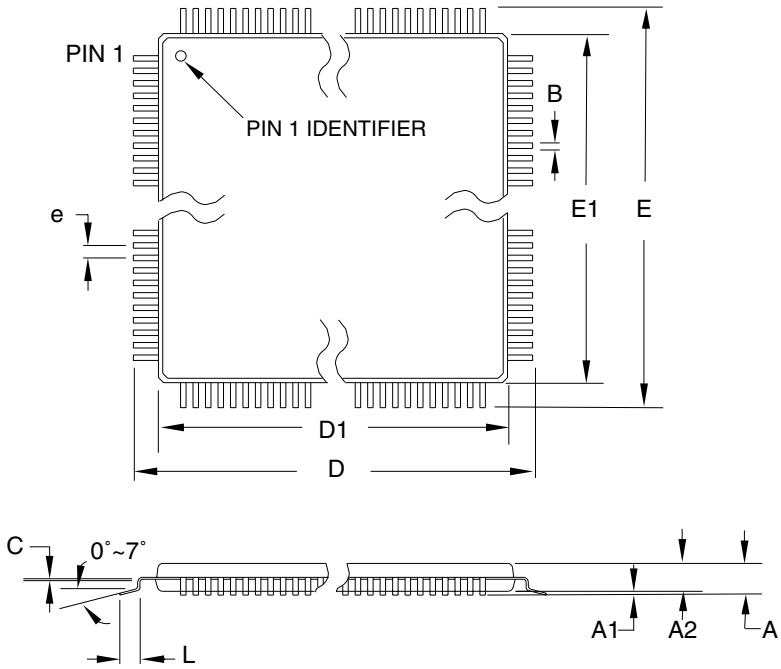
| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 20 | 12 | 83.3 | ATF1504ASL-20 AC44 | 44A | Commercial |
| | | | ATF1504ASL-20 JC44 | 44J | (0°C to 70°C) |
| | | | ATF1504ASL-20 JC68 | 68J | |
| | | | ATF1504ASL-20 JC84 | 84J | |
| | | | ATF1504ASL-20 QC100 | 100Q1 | |
| | | | ATF1504ASL-20 AC100 | 100A | |
| 25 | 15 | 70 | ATF1504ASL-25 AI44 | 44A | Industrial |
| | | | ATF1504ASL-25 JI84 | 44J | (-40°C to +85°C) |
| | | | ATF1504ASL-25 JI68 | 68J | |
| | | | ATF1504ASL-25 JI84 | 84J | |
| | | | ATF1504ASL-25 QI100 | 100Q1 | |
| | | | ATF1504ASL-25 AI100 | 100A | |

## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

## Packaging Information

### 44A – TQFP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

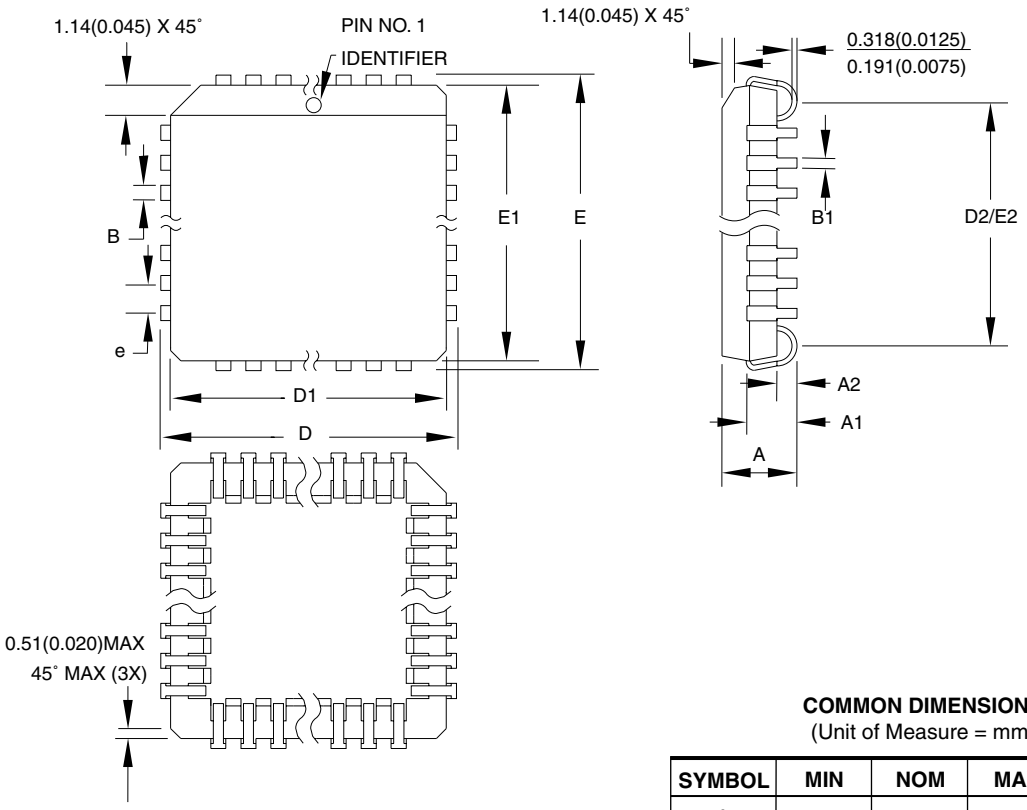
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 44A | B |

## 44J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

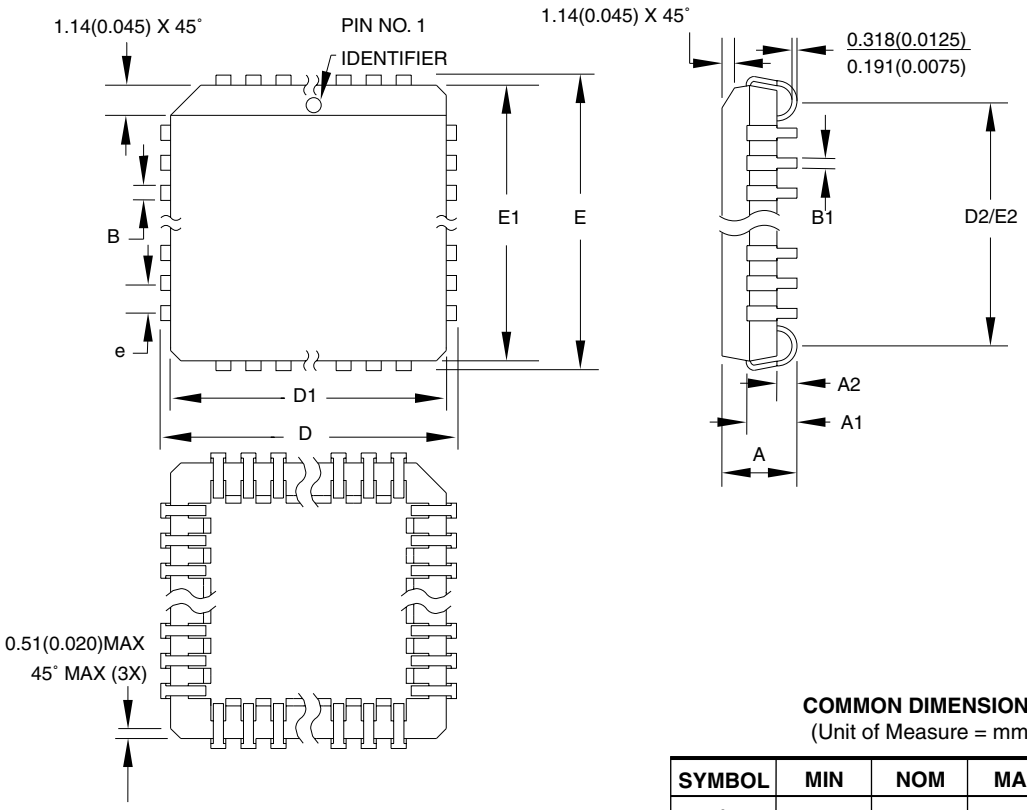
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 17.399 | – | 17.653 | |
| D1 | 16.510 | – | 16.662 | Note 2 |
| E | 17.399 | – | 17.653 | |
| E1 | 16.510 | – | 16.662 | Note 2 |
| D2/E2 | 14.986 | – | 16.002 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC) | 44J | B |

## 68J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

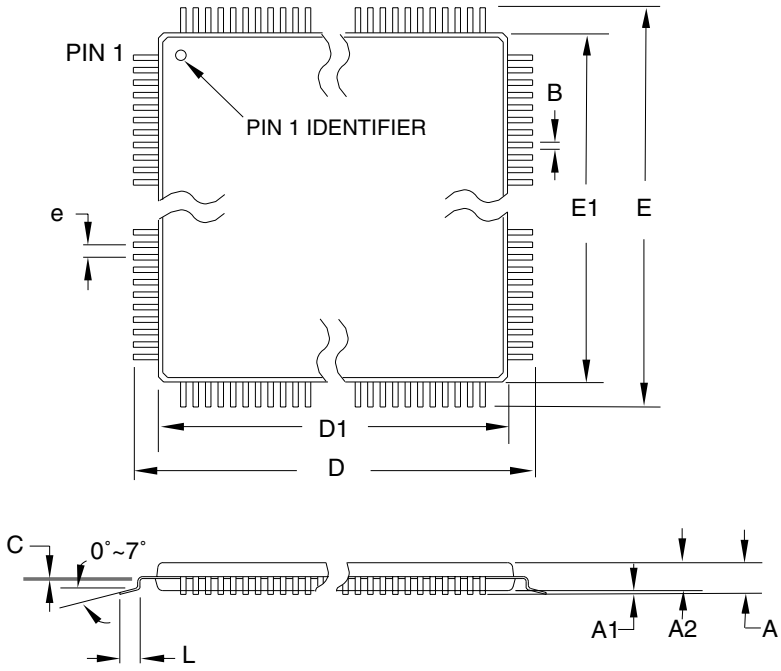
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 25.019 | – | 25.273 | |
| D1 | 24.130 | – | 24.333 | Note 2 |
| E | 25.019 | – | 25.273 | |
| E1 | 24.130 | – | 24.333 | Note 2 |
| D2/E2 | 22.606 | – | 23.622 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **68J**, 68-lead, Plastic J-leaded Chip Carrier (PLCC) | 68J | B |

## 100A – TQFP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 15.75 | 16.00 | 16.25 | |
| D1 | 13.90 | 14.00 | 14.10 | Note 2 |
| E | 15.75 | 16.00 | 16.25 | |
| E1 | 13.90 | 14.00 | 14.10 | Note 2 |
| B | 0.17 | – | 0.27 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.50 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 100A | C |