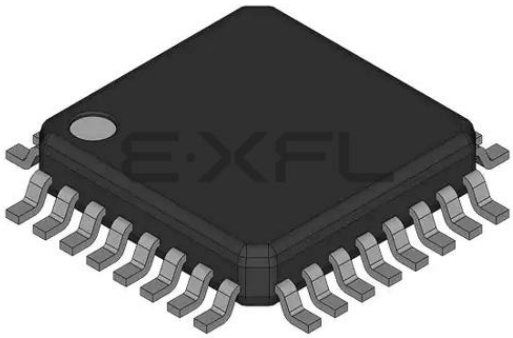

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	LVD, POR, PWM, RF Mod
Number of I/O	12
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908rf2cfa

Table of Contents

Section 10. System Integration Module (SIM)

Section 11. Timer Interface Module (TIM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FFF0	FLASH 2TS Block Protect Register (FLBPR)† See page 34.	Read: Write:	R	R	R	R	BPR3	BPR2	BPR1	BPR0
		Reset:	Unaffected by reset							
$FFFF	COP Control Register (COPCTL) See page 49.	Read:	LOW BYTE OF RESET VECTOR							
		Write:	WRITING CLEARS COP COUNTER (ANY VALUE)							
		Reset:	Unaffected by reset							

† Non-volatile FLASH register

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 5)

Table 2-1 is a list of vector locations.

Table 2-1. Vector Locations

	Address	Vector
Low	$FFF2	ICG vector (high)
	$FFF3	ICG vector (low)
	$FFF4	TIM overflow vector (high)
	$FFF5	TIM overflow vector (low)
	$FFF6	TIM channel 1 vector (high)
	$FFF7	TIM channel 1 vector (low)
Priority	$FFF8	TIM channel 0 vector (high)
	$FFF9	TIM channel 0 vector (low)
	$FFFA	IRQ/keyboard vector (high)
	$FFFB	IRQ/keyboard vector (low)
	$FFFC	SWI vector (high)
	$FFFD	SWI vector (low)
High	$FFFE	Reset vector (high)
	$FFFF	Reset vector (low)

2.3 Monitor ROM

The 768 bytes at addresses $F000–F2EF and $FEF0–$FEFF are utilized by the monitor ROM.

The address range $F000–F2EF is reserved for the monitor code functions, FLASH memory programming, and erase algorithms.

The address range $FEF0–$FEFF holds reserved ROM addresses that contain the monitor code reset vectors.

2.5.5 FLASH 2TS Block Protection

NOTE: *In performing a program or erase operation, the FLASH 2TS block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

Due to the ability of the on-board charge pump to erase and program the FLASH 2TS memory in the target application, provision is made for protecting blocks of memory from unintentional erase or program operations due to system malfunction. This protection is implemented by a reserved location in the memory for block protect information. This block protect register must be read before setting HVEN = 1. When the block protect register is read, its contents are latched by the FLASH 2TS control logic. If the address range for an erase or program operation includes a protected block, the PGM or ERASE bit is cleared which prevents the HVEN bit in the FLASH 2TS control register from being set such that no high-voltage operation is allowed in the array.

When the block protect register is erased (all 0s), the entire memory is accessible for program and erase. When bits within the register are programmed, they lock blocks of memory address ranges as shown in **2.5.6 FLASH 2TS Block Protect Register**. The block protect register itself can be erased or programmed only with an external voltage V_{TST} present on the $\overline{IRQ}$ pin. The presence of V_{TST} on the $\overline{IRQ}$ pin also allows entry into monitor mode out of reset. Therefore, the ability to change the block protect register is voltage-level dependent and can occur in either user or monitor modes.

2.5.6 FLASH 2TS Block Protect Register

The block protect register (FLBPR) is implemented as a byte within the FLASH 2TS memory. Each bit, when programmed, protects a range of addresses in the FLASH 2TS.

Address: $FFF0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	R	R	R	BPR3	BPR2	BPR1	BPR0
Reset:	Unaffected by reset							

R = Reserved

Figure 2-5. FLASH 2TS Block Protect Register (FLBPR)

BPR3 — Block Protect Register Bit 3

This bit protects the memory contents in the address ranges $7A00–$7FEF and $FFF0–$FFFF.

1 = Address range protected from erase or program

0 = Address range open to erase or program

The row whose cycling bit is different will be erased and the entire row will be programmed with the given data, including a toggled version of the cycling bit.

2.5.8.5 Example Routine Calls

This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
RAM             EQU     $80
RDVRRNG         EQU     $F000
PRGRNGE         EQU     $F003
ERANRGE         EQU     $F006
REDPROG         EQU     $F009
;*************************************************************
 RAM Definitions for Subroutines
;*************************************************************

ORG     RAM+8

CTRLBYT         RMB     1
CPUSPD          RMB     1
LADDR           RMB     2
BUMPS           RMB     1
DERASE          RMB     2

;Allocation of "DATA" space is dependent on the device and
;application

DATA    RMB     8
;*************************************************************
; CALLING EXAMPLE FOR READ/VERIFY A RANGE (RDVRRNG)
;*************************************************************
LDA     #$FF            ;TARGET IS RAM
LDHX    #$7807          ;END AFTER FIRST ROW
STHX    LADDR
LDHX    #$7800          ;START AT FIRST ROW
JSR     RDVRRNG         ;DATA WILL CONTAIN FLASH INFO
;*************************************************************;
CALLING EXAMPLE FOR ERASE A RANGE (RNGEERA)
;*************************************************************
MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$60,CTRLBYT    ;Bits 5&6 hold the block size to erase
                        ;00  Full Array
                        ;20  One-Half Array
                        ;40  Eight Rows
                        ;60  Singe Row
                        ;Remember a Row is 1 byte

                        ;Set erase time in uS/24, number in
                        ;decimal
LDHX    #100000/24
STHX    DERASE
```

```
LDHX    #$7800          ;Address in the range to erase
JSR     ERARNGE         ;Call through jump table

;*************************************************************;
; CALLING EXAMPLE FOR PROGRAM A RANGE (RNGEPROG)
;*************************************************************
MOV     #'P',DATA
MOV     #'R',DATA+1
MOV     #'O',DATA+2
MOV     #'G',DATA+3
MOV     #'T',DATA+4
MOV     #'E',DATA+5
MOV     #'S',DATA+6
MOV     #'T',DATA+7

MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$0A,BUMPS      ;Load max number of programming steps
                        ;before a failure is returned
LDHX     #$7807         ;Load the last address to program
STHX     LADDR          ;into LADDR
LDHX    #$7800          ;Load the first address to program
                        ;into H:X
                        ;This range may cross page boundaries
                        ;and may be any length, so long as the
                        ;data to program is loaded in RAM
                        ;beginning at DATA.
JSR     PRGRNGE         ;Call through jump table.
;*************************************************************
; CALLING EXAMPLE FOR REDUNDANT PROGRAM A ROW (REDPROG)
;*************************************************************
MOV     #$56,DATA
MOV     #'P',DATA+1
MOV     #'R',DATA+2
MOV     #'O',DATA+3
MOV     #'G',DATA+4
MOV     #'R',DATA+5
MOV     #'E',DATA+6
MOV     #'D',DATA+7

MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$0A,BUMPS      ;Load max number of programming steps
                        ;before a failure is returned
                        ;Set erase time in uS/24
LDHX    #100000/24
STHX    DERASE

LDHX     #$7808         ;Load the last address of the multi-row
                        ;range; (in this case, 2 rows)
STHX     LADDR          ;into LADDR
LDHX    #$7800          ;Load the first address of the
                        ;multi-row range into H:X
JSR     REDPROG         ;Call through jump table.
```

5.3 CPU Registers

Figure 5-1 shows the five CPU registers. CPU registers are not part of the memory map.

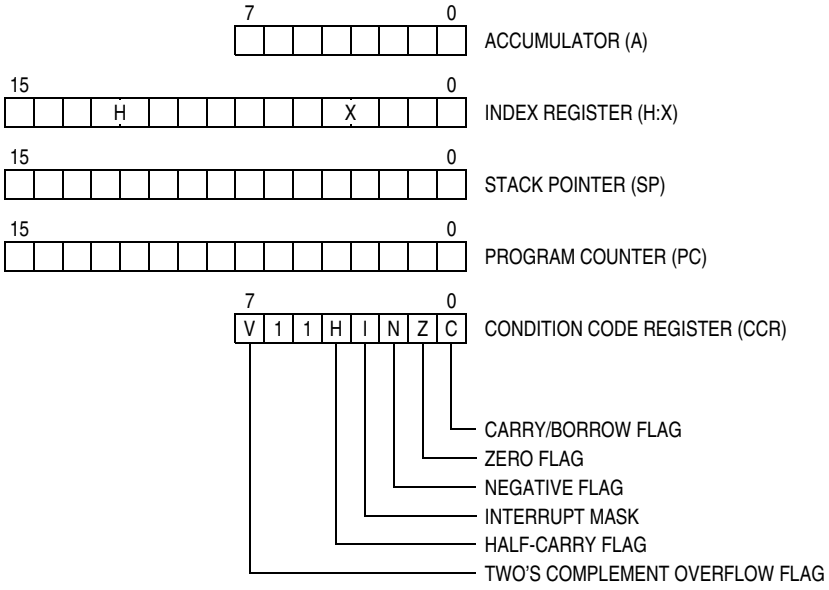

Figure 5-1. CPU Registers

5.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

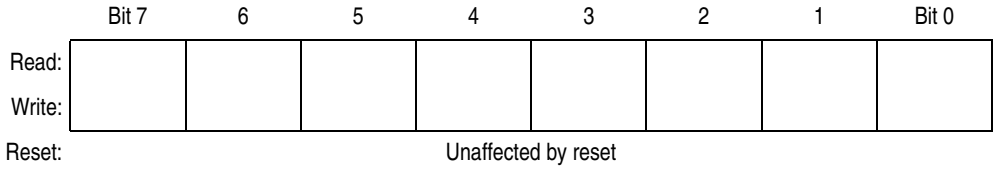

Figure 5-2. Accumulator (A)

6.6 Configuration Register Option

One configuration register option affects the functionality of the ICG: EXTSLOW (slow external clock).

All configuration register options will have a default setting. Refer to **Section 3. Configuration Register (CONFIG)** on how the configuration register is used.

6.6.1 EXTSLOW

Slow external clock (EXTSLOW), when set, will decrease the drive strength of the oscillator amplifier, enabling low-frequency crystal operation (30 kHz–100 kHz). When clear, EXTSLOW enables high frequency crystal operation (1 MHz to 8 MHz).

EXTSLOW, when set, also configures the clock monitor to expect an external clock source that is slower than the low-frequency base clock (60 Hz–307.2 kHz). When EXTSLOW is clear, the clock monitor will expect an external clock faster than the low-frequency base clock (307.2 kHz–32 MHz).

The default state for this option is clear.

6.7 I/O Registers

The ICG contains five registers, summarized in **Figure 6-10**. These registers are:

- ICG control register, ICGCR
- ICG multiplier register, ICGMR
- ICG trim register, ICGTR
- ICG DCO divider control register, ICGDVR
- ICG DCO stage control register, ICGDSR

Several of the bits in these registers have interaction where the state of one bit may force another bit to a particular state or prevent another bit from being set or cleared. A summary of this interaction is shown in **Table 6-5**.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	Internal Clock Generator Control Register (ICGCR) See page 88.	Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$0037	Internal Clock Generator Multiplier Register (ICGMR) See page 90.	Read:	R	N6	N5	N4	N3	N2	N1	N0
		Write:								
		Reset:	0	0	0	1	0	1	0	1

Figure 6-10. ICG I/O Register Summary

6.7.1 ICG Control Register

The ICG control register (ICGCR) contains the control and status bits for the internal clock generator, external clock generator, and clock monitor as well as the clock select and interrupt enable bits.

Address: $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
Write:								
Reset:	0	0	0	0	1	0	0	0

= Unimplemented

Figure 6-11. ICG Control Register (ICGCR)

CMIE — Clock Monitor Interrupt Enable Bit

This read/write bit enables clock monitor interrupts. An interrupt will occur when both CMIE and CMF are set. CMIE can be set when the CMON bit has been set for at least one cycle. CMIE is forced clear when CMON is clear or during reset.

1 = Clock monitor interrupts enabled
0 = Clock monitor interrupts disabled

CMF — Clock Monitor Interrupt Flag

This read-only bit is set when the clock monitor determines that either ICLK or ECLK becomes inactive and the CMON bit is set. This bit is cleared by first reading the bit while it is set, followed by writing the bit low. This bit is forced clear when CMON is clear or during reset.

1 = Either ICLK or ECLK has become inactive.
0 = ICLK and ECLK have not become inactive since the last read of the ICGCR or the clock monitor is disabled.

CMON — Clock Monitor On Bit

This read/write bit enables the clock monitor. CMON can be set when both ICLK and ECLK have been on and stable for at least one bus cycle (ICGON, ECGON, ICGS, and ECGS are all set). CMON is forced set when CMF is set, to avoid inadvertent clearing of CMF. CMON is forced clear when either ICGON or ECGON is clear or during reset.

1 = Clock monitor output enabled
0 = Clock monitor output disabled

In addition to forcing a reset condition, the LVI module has a second circuit dedicated to low-voltage detection. When V_{DD} falls below V_{LVS}, the output of the low-voltage comparator asserts the LOWV flag in the LVI status register (LVISR). In applications that require detecting low batteries, software can monitor by polling the LOWV bit.

8.3.1 False Trip Protection

The V_{DD} pin level is digitally filtered to reduce false dead battery detection due to power supply noise. For the LVI module to reset due to a low-power supply, V_{DD} must remain at or below the V_{LVR} level for a minimum 32–40 CGMXCLK cycles. See **Table 8-1**.

Table 8-1. LOWV Bit Indication

V_{DD}		Result
At Level:	**For Number of CGMXCLK Cycles:**	
$V_{DD} > V_{LVR}$	ANY	Filter counter remains clear
$V_{DD} < V_{LVR}$	< 32 CGMXCLK cycles	No reset, continue counting CGMXCLK
$V_{DD} < V_{LVR}$	Between 32 and 40 CGMXCLK cycles	LVI may generate a reset after 32 CGMXCLK cycles
$V_{DD} < V_{LVR}$	> 40 CGMXCLK cycles	LVI is guaranteed to generate a reset

8.3.2 Short Stop Recovery Option

The LVI has an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32 CGMXCLK delay must be greater than the LVI turn on time to avoid a period in startup where the LVI is not protecting the MCU.

NOTE: *The LVI is enabled automatically after reset or stop recovery, if the LVISTOP of the CONFIG register is set. (See **Section 3. Configuration Register (CONFIG)**.)*

TCH0 — Timer Channel I/O Bit

The PTB2/TCH0 pin is the TIM channel 0 input capture/output compare pin. The edge/level select bits, ELS0B:ELS0A, determine whether the PTB2/TCH0 pin is a timer channel I/O or a general-purpose I/O pin. See **Section 11. Timer Interface Module (TIM)**.

TCLK — Timer Clock Bit

The PTB3/TCLK pin is the external clock input for TIM. The prescaler select bits, PS[2:0], select PTB3/TCLK as the TIM clock input. (See **11.8.1 TIM Status and Control Register**.) When not selected as the TIM clock, PTB3/TCLK is available for general-purpose I/O.

MCLK — Bus Clock Bit

The bus clock (MCLK) is driven out of pin PTB0/MCLK when enabled by the MCLKEN bit in port B data direction register bit 7.

9.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MCLKEN	0			DDRB3	DDRB2	DDRB1	DDRB0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-6. Data Direction Register B (DDRB)

MCLKEN — MCLK Enable Bit

This read/write bit enables MCLK to be an output signal on PTB0. If MCLK is enabled, PTB0 is under the control of MCLKEN. Reset clears this bit.

1 = MCLK output enabled
0 = MCLK output disabled

DDRB[3:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[3:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 9-7 shows the port B I/O logic.

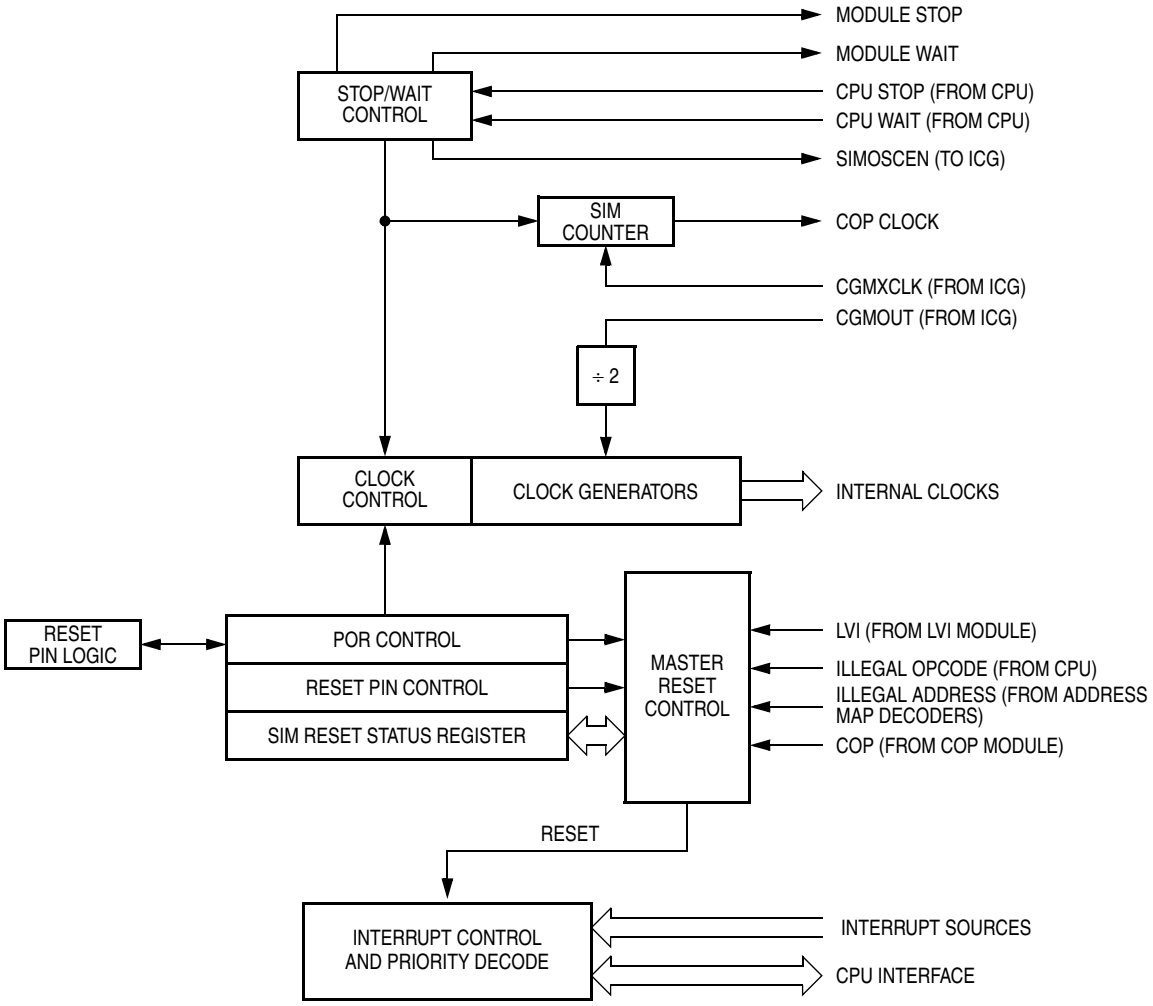

Figure 10-2. SIM Block Diagram

Table 10-1 shows the internal signal names used in this section.

Table 10-1. Signal Name Conventions

Signal Name	Description
CGMXCLK	Selected clock source from internal clock generator module (ICG)
CGMOUT	Clock output from ICG module (bus clock = CGMOUT divided by two)
ICLK	Output from internal clock generator
ECLK	External clock source
IAB	Internal address bus
IDB	internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/$\overline{W}$	Read/write signal

signal then follows the sequence from the falling edge of $\overline{RST}$ shown in **Figure 10-5**.

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

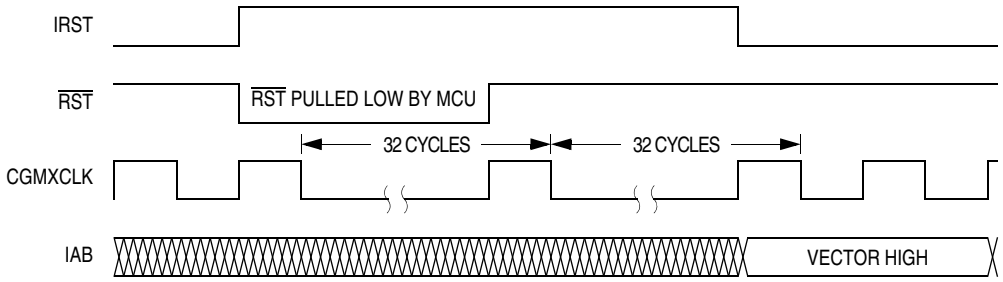

Figure 10-5. Internal Reset Timing

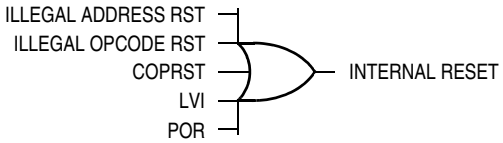

Figure 10-6. Sources of Internal Reset

10.3.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ($\overline{RST}$) is held low while the SIM counter counts out 4096 CGMXCLK cycles. Another 64 CGMXCLK cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, these events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables CGMOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 CGMXCLK cycles to allow stabilization of the oscillator.
- The $\overline{RST}$ pin is driven low during the oscillator stabilization time.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

11.4.1 TIM Counter Prescaler

The TIM clock source can be one of the seven prescaler outputs or the TIM clock pin, TCLK. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register select the TIM clock source.

11.4.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH and TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

NOTE: *TIM channel 1 should not be configured in this mode.*

11.4.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM channel 0 can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests for both TIM channel 0 and TIM channel 1.

NOTE: *TIM channel 1 does not have an external pin associated with it.*

11.4.4 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in **11.4.3 Output Compare**. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use these methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

NOTE: *Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM counter is reset and always reads as 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared
0 = No effect

NOTE: *Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of $0000.*

PS2–PS0 — Prescaler Select Bits

These read/write bits select either the TCLK pin or one of the seven prescaler outputs as the input to the TIM counter as **Table 11-2** shows. Reset clears the PS2–PS0 bits.

Table 11-2. Prescaler Selection

PS2–PS0	TIM Clock Source
000	Internal bus clock ÷1
001	Internal bus clock ÷ 2
010	Internal bus clock ÷ 4
011	Internal bus clock ÷ 8
100	Internal bus clock ÷ 16
101	Internal bus clock ÷ 32
110	Internal bus clock ÷ 64
111	TCLK

Register Name and Address: TCH0H—$0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	Indeterminate after reset							

Register Name and Address: TCH0L—$0027

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	Indeterminate after reset							

Figure 11-10. TIM Channel 0 Registers (TCH0H and TCH0L)

Register Name and Address: TCH1H—$0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	Indeterminate after reset							

Register Name and Address: TCH1L—$002A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	Indeterminate after reset							

Figure 11-11. TIM Channel 1 Registers (TCH1H and TCH1L)

Section 12. PLL Tuned UHF Transmitter Module

12.1 Introduction

This section describes the integrated radio frequency (RF) module. This module integrates an ultra high frequency (UHF) transmitter offering these key features:

- Switchable frequency bands: 315, 434, and 868 MHz
- On/off keying (OOK) and frequency shift keying (FSK) modulation
- Adjustable output power range
- Fully integrated voltage-controlled oscillator (VCO)
- Supply voltage range: 1.9 to 3.7 V
- Very low standby current: 0.5 nA @ T_A = 25°C
- Low supply voltage shutdown
- Data clock output for microcontroller
- Low external component count

Architecture of the module is described in **Figure 12-1**.

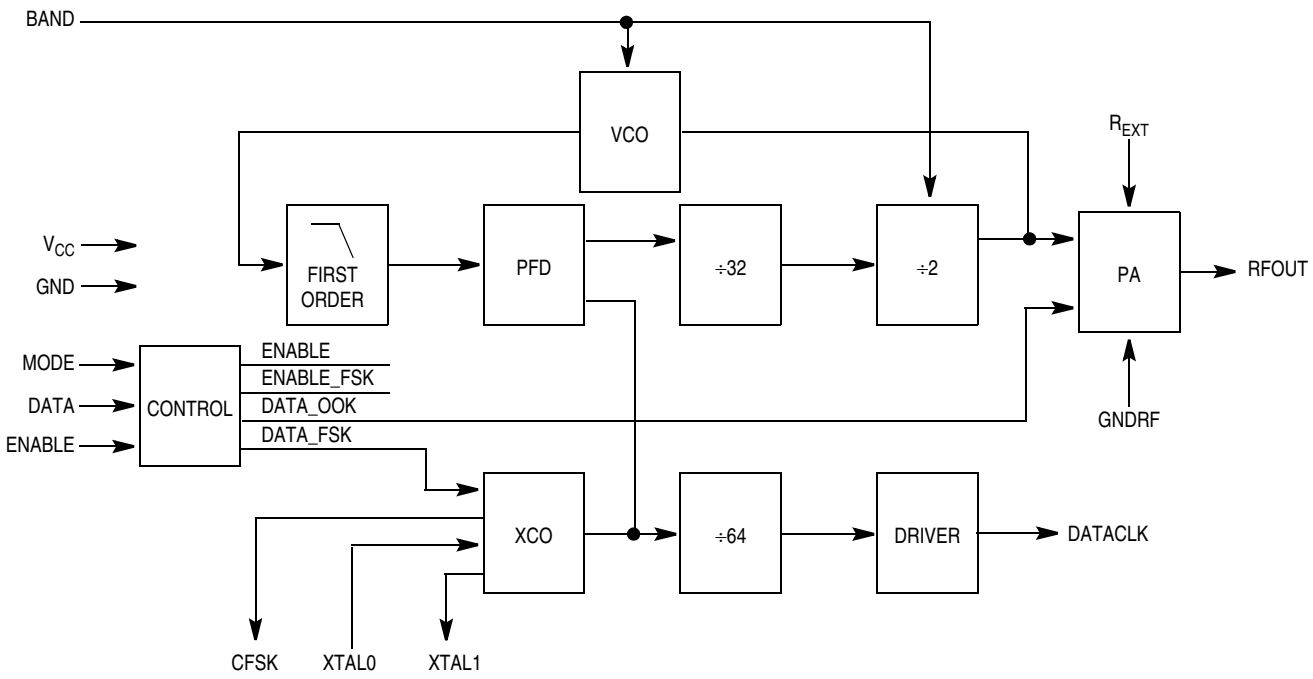

Figure 12-1. Simplified Integrated RF Module Block Diagram

14.5 1.8-Volt to 3.3-Volt DC Electrical Characteristics Excluding UHF Module

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –1.2 mA) (I_{Load} = –2.0 mA)	V_{OH}	 V_{DD} –0.3 V_{DD} –1.0	 — —	 — —	V
Output low voltage (I_{Load} = 1.2 mA) (I_{Load} = 3.0 mA) (I_{Load} = 3.0 mA) PTA7–PTA0 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.3	V
Input high voltage, all ports, $\overline{IRQ1}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage, all ports, $\overline{IRQ1}$, OSC1	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
V_{DD} supply current Run[3] (f_{op}= 2.0 MHz) Wait[4] (f_{op}= 2.0 MHz) Stop[5] 25°C –40°C to 85°C –40°C to 125°C 25°C with LVI enabled –40°C to 85°C with LVI enabled	I_{DD}	 — — — — — — —	 — — 10 — 800 50 —	 4.3 1.2 — 100 1100 — 350	 mA mA nA nA nA µA µA
I/O ports high-impedance leakage current[6]	I_{IL}	—	—	±1	µA
Input current	I_{In}	—	—	±1	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	200	mV
POR reset voltage[8]	V_{POR}	0	700	800	mV
POR rise time ramp rate[9]	R_{POR}	0.02	—	—	V/ms
Monitor mode entry voltage	V_{HI}	V_{DD} + 2.5	—	8	V
Pullup resistor, PTA6–PTA1, $\overline{IRQ}$	R_{PU}	50	80	120	kΩ

1. Parameters are design targets at V_{DD} = 1.8 V to 3.3 V, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Run (operating) I_{DD} measured using internal clock generator module (f_{op}= 2.0 MHz). V_{DD} = 3.3 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. C_L = 20 pF. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using internal clock generator module, f_{op} = 2.0 MHz. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF. OSC2 capacitance linearly affects wait I_{DD}. All ports configured as inputs.
5. Stop I_{DD} measured with no port pins sourcing current, all modules disabled except as noted.
6. Pullups and pulldowns are disabled.
7. Maximum is highest voltage that POR is guaranteed.
8. Maximum is highest voltage that POR is possible.
9. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.

Parameter	Test Conditions and Comments	Min	Typ	Max	Unit
Supply voltage		—	3	3.7	V
Shutdown voltage threshold	T_A = –40°C	—	2.04	2.11	V
	T_A = –20°C	—	1.99	2.06	V
	T_A = 25°C	—	1.86	1.95	V
	T_A = 60°C	—	1.76	1.84	V
	T_A = 85°C	—	1.68	1.78	V
	T_A = 125°C	—	1.56	1.67	V
RF Parameters (assuming a 50 Ω matching network connected to the D.U.T. output)					
R_{EXT} value		12	—	21	kΩ
Output power	315 and 434 MHz bands, with 50 Ω matching network	—	5	—	dBm
	868 MHz band, with 50 Ω matching network	—	1	—	dBm
	315 and 434 MHz bands, –40°C ≤ T_A ≤ 125°C	–3	0	3	dBm
	868 MHz band, –40°C ≤ T_A ≤ 125°C	–7	–3	0	dBm
Current and output power variation vs R_{EXT} value	314 and 434 MHz bands, with 50 Ω matching network	—	–0.35	—	dB/kΩ mA/kΩ
Harmonic 2 level	315 and 434 MHz bands, with 50 Ω matching network	—	–34	—	dBc
	868 MHz band, with 50 Ω matching network	—	–49	—	dBc
	315 and 434 MHz bands	—	–23	–17	dBc
	868 MHz band	—	–38	–27	dBc
Harmonic 3 level	315 and 434MHz bands, with 50 Ω matching network	—	–32	—	dBc
	868 MHz band, with 50 Ω matching network	—	–57	—	dBc
	315 and 434 MHz bands	—	–21	–15	dBc
	868 MHz band	—	–48	–39	dBc
Spurious level @ $f_{Carrier} \pm f_{DATACLK}$	315 and 434 MHz bands	—	–36	–24	dBc
	868 MHz band		–29	–17	dBc
Spurious level @ $f_{Carrier} \pm f_{Reference}$	315 MHz band	—	–37	–30	dBc
	434 MHz band	—	–44	–34	dBc
	868 MHz band	—	–37	–27	dBc
Spurious level @ $f_{Carrier}/2$	315 MHz bands	—	–62	–53	dBc
	434 MHz bands	—	–80	–60	dBc
	868 MHz band	—	–45	–39	dBc

Table concluded on next page

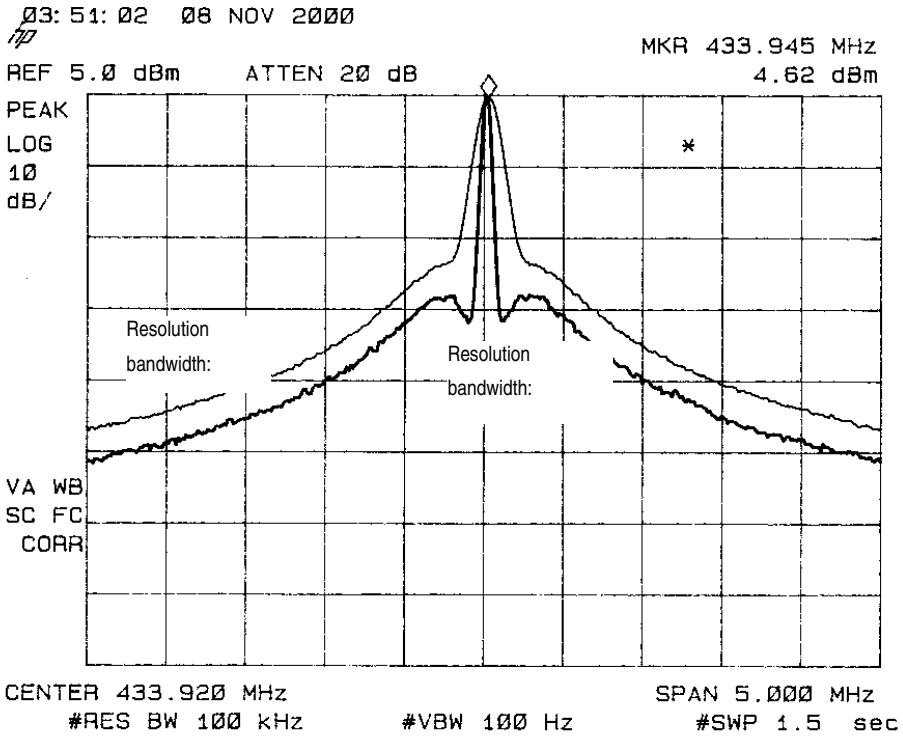

Figure 14-1. RF Spectrum at 434-MHz Frequency Band Displayed with a 5-MHz Span

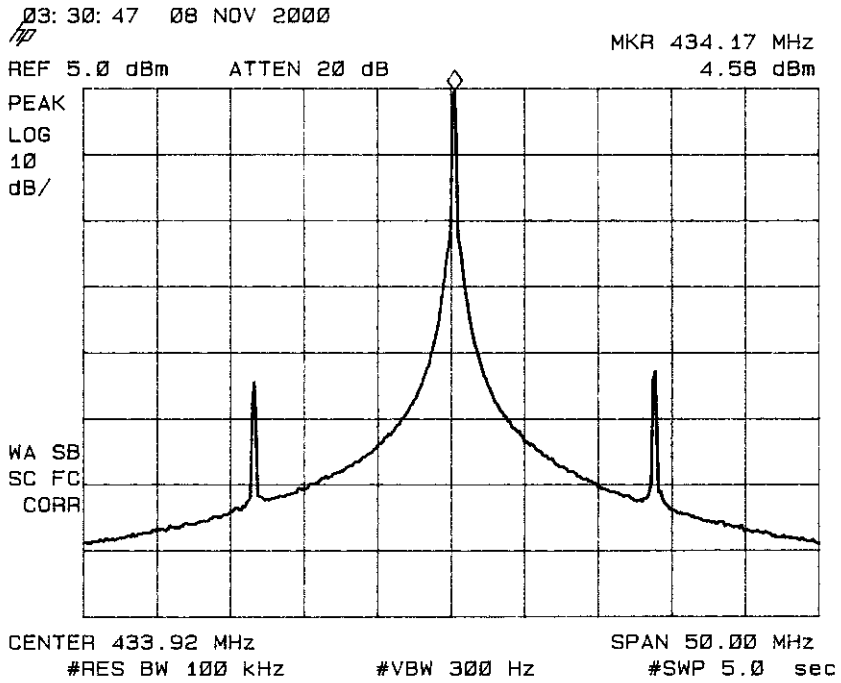

Figure 14-2. RF Spectrum at 434-MHz Frequency Band Displayed with a 50-MHz Span