Renesas Electronics America Inc - 79RC32K438-200BBG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	416-BGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-200bbg

card application, or as the primary PCI controller in the system. The PCI interface can be operated synchronously or asynchronously to the other I/O interfaces on the RC32438 device.

Ethernet Interface

The RC32438 has two Ethernet Channels supporting 10Mbps and 100Mbps speeds to provide a standard media independent interface (MII) off-chip, allowing a wide range of external devices to be connected efficiently.

UART Interface

The RC32438 contains two completely separate serial channels (UARTs) that are compatible with the industry standard 16550 UART.

System Integrity Functions

The RC32438 contains a programmable watchdog timer that generates NMI when the counter expires and an address space monitor that reports errors in response to accesses to undecoded address regions.

General Purpose I/O Controller

The RC32438 contains 32 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

I^2C Interface

The standard I2C interface allows the RC32438 to connect to a number of standard external peripherals for a more complete system solution. The RC32438 supports both master and slave operations.

Debug Support

The RC32438 supports the industry standard Rev. 2.6 EJTAG interface.

Thermal Considerations

The RC32438 consumes less than 2.7 W peak power. It is guaranteed in a ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

November 7, 2002: Initial publication. Preliminary Information.

November 15, 2002: Added footnotes to Tables 5, 9, and 10.

December 12, 2002: Added Clock Speed parameter to PLL and Core supply in Table 16.

December 19, 2002: Release version.

January 13, 2003: Changed Thermal Considerations to read less than 2.7W instead of 2.5W, added values to CLK parameter in Table 5, and revised EJTAG description.

February 4, 2003: Revised description for EJTAG/JTAG pins in Table 1. Changed DDRDM[7:0] from input/output to output only in Tables 1 and 2 and Logic Diagram. Added new section, Voltage Sense Signal Timing, as part of EJTAG description.

March 4, 2003: In Table 2, removed “pull-up” from PCI pin category and from GPIO [24] and GPIO[30-26]. In Table 20, changed max. values for VccSI/O, VccCore, and VccPLL.

July 9, 2003: In Table 7: changed values for DDRDATA, DDRDM, and DDRADDR—WEN signals, and deleted old footnote #3 and changed values in new footnote #3. In Table 8, changed Tdo values. Changed Figure 7. Changed values in Table 18, Power Consumption. Removed IPBus Monitor feature which included changes to Tables 1, 2, 21, 24, and 25. Deleted Table 13 which resulted in a re-ordering of subsequent tables.

March 8, 2004: Added 300MHz speed grade.

May 25, 2004: In Table 9, signals MIIxRXCLK and MIIxTXCLK, the Min and Max values for Thigh/Tlow_9c were changed to 140 and 260 respectively and the Min and Max values for Thigh/Tlow_9d were changed to 14.0 and 26.0 respectively.

Signal	Type	Name/Description
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI command is driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32438 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted. PCIGNTN[1]: this signal takes on the alternate function of PCIEECS and is used as a PCI Serial EEPROM chip select PCIGNTN[3:2]: unused and driven high. **Note**: When the GPIO register is programmed in the alternate function mode for bits GPIO [26] and [28], these bits become PCIGNTN [4] and [5] respectively.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.

Table 1 Pin Description (Part 3 of 9)

Signal	Type	Name/Description
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send output.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send input.
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1SOUT Alternate function: UART channel 1 serial output.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1SINP Alternate function: UART channel 1 serial input.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1DTRN Alternate function: UART channel 1 data terminal ready output.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1DSRN Alternate function: UART channel 1 data set ready input.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1RTSN Alternate function: UART channel 1 request to send output.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1CTSN Alternate function: UART channel 1 clear to send input.
GPIO[14]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAREQN0 Alternate function: External DMA channel 0 request input.
GPIO[15]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAREQN1 Alternate function: External DMA channel 1 request input.
GPIO[16]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMADONEN0 Alternate function: External DMA channel 0 done input.
GPIO[17]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMADONEN1 Alternate function: External DMA channel 1 done input.

Table 1 Pin Description (Part 5 of 9)

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.

Parameter	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	200	200	233	200	266	200	300	MHz	See Figure 3.
	Tper		5.0	5.0	4.2	5.0	3.8	5.0	3.3	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	100	100	116.5	100	133	100	150	MHz	
	Tper		10.0	10.0	10.0	8.5	10.0	7.5	6.7	10.0	ns	
CLK[5]	Frequency	none	25	66.6	25	77.6	25	88.6	25	100	MHz	
	Tper_5a		15.0	40.0	12.9	40.0	11.2	40.0	10	40	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3).
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

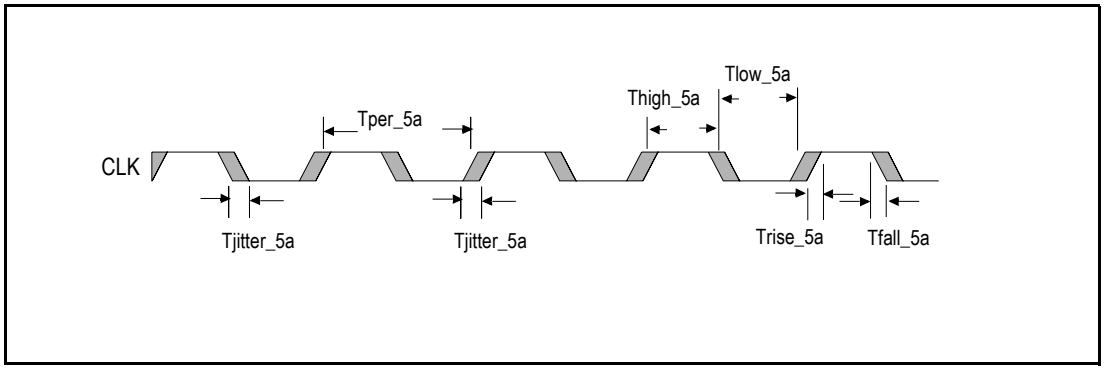
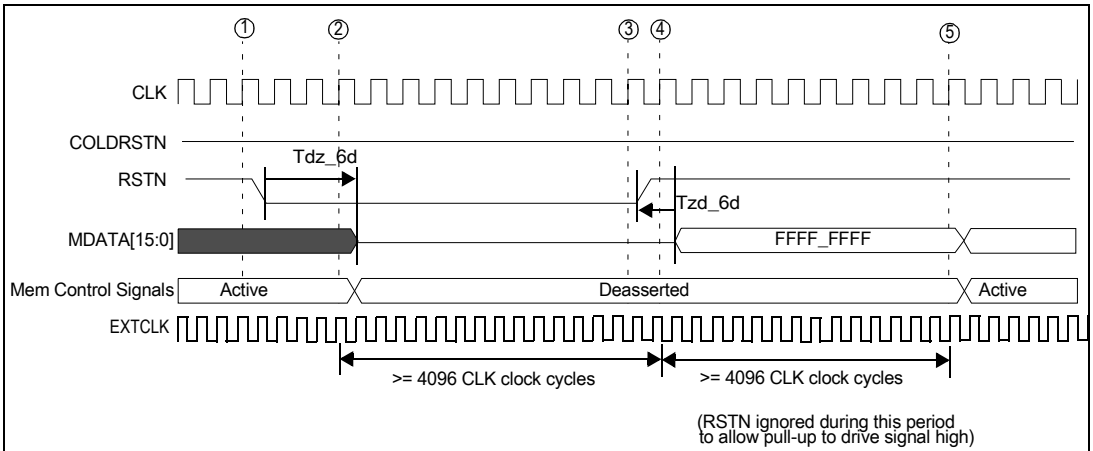


Figure 3 Clock Parameters Waveform



1. Warm reset caused by any of the conditions listed in the Warm Reset section of Chapter 3, Clocking and Initialization, in the RC32438 User Reference Manual.
2. The RC32438 tri-states the data bus, MDATA[15:0], and negates all memory control signals.
3. The RC32438 negates RSTN.
4. The RC32438 starts driving the data bus, MDATA[15:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 5 Warm Reset AC Timing Waveform

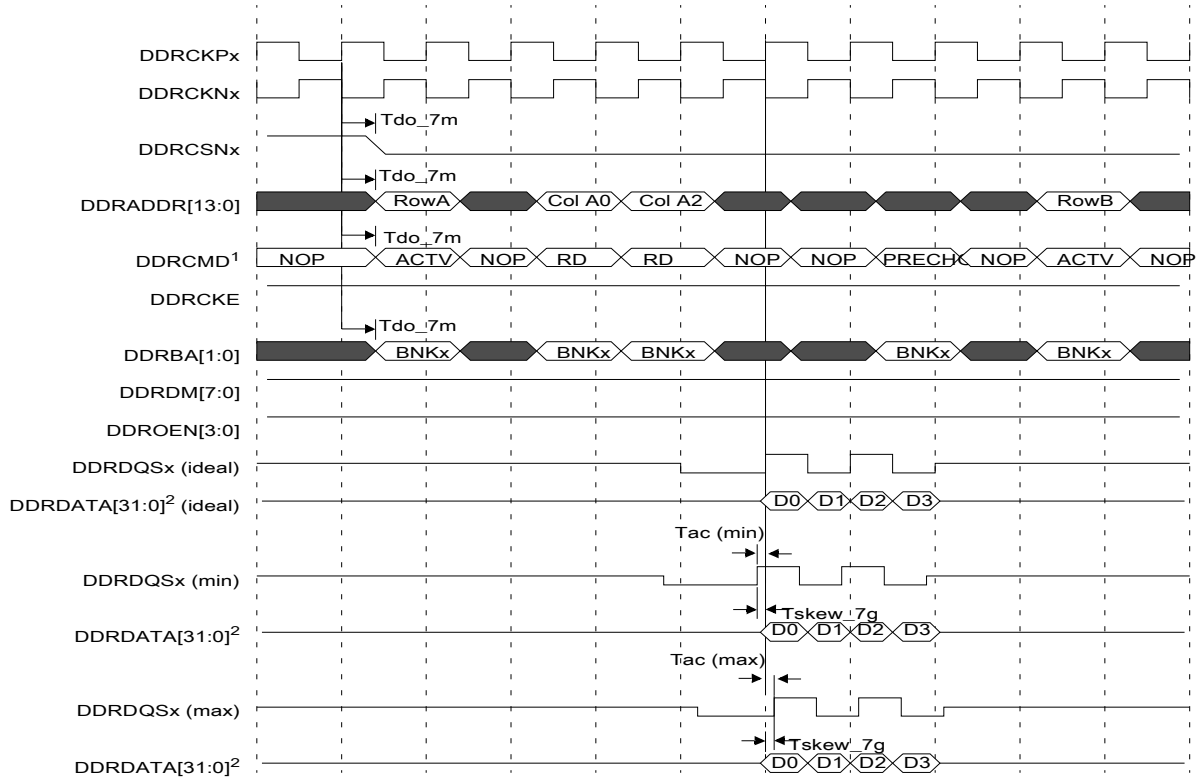
Signal	Symbol[1]	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory Bus - DDR Access													
DDRDATA[31:0]	Tskew_7g[2]	DDRDQSx	0.0	0.9	0.0	0.9	0.0	0.9	0.0	0.8	ns		See Figures 6 and 7.
	Tdo_7k[3]		1.5	3.3	1.1	2.9	0.9	2.7	0.7	2.4	ns		
DDRDM[7:0]	Tdo_7l	DDRDQSx	1.5	3.3	1.1	2.9	0.9	2.7	0.7	2.4	ns		
DDRDQS[3:0]	Tac	DDRCKPx	-0.75	0.75	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns		
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN[1:0], DDROEN[3:0], DDRRASN, DDRWEN	Tdo_7m[4]	DDRCKPx	1.1	4.5	1.1	4.5	1.1	4.5	1.1	4.5	ns		

Table 7 DDR SDRAM Timing Characteristics

1. In the DDR data sheet: Tskew_7g = $t_{DQSQ;}$ Tdo_7k = t_{DH}, $t_{DS;}$ Tdo_7l = t_{DH}, $t_{DS;}$ Tac = $t_{AC;}$ Tdo_7m = t_{IH}, $t_{IS.}$

2. Meets DDR timing requirements for DDR 266 SDRAMs with 400 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32438 DDR layout guidelines are followed.

3. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.5ns, the T_{IS} parameter is 7.5ns minus 4.5ns = 3ns. The DDR spec for this parameter is 1ns, so there is 2ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 2.7ns, we have 3.75ns minus 2.7ns = 1.05ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 0.55ns slack for board propagation delays.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32438 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[15:0]	Tsu_8c	EXTCLK rising	7.0	—	7.0	—	7.0	—	7.0	—	ns		See Figures 8 and 9 (cont.)
	Thld_8c		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_8c		0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8c[2]		0.0	0.1	0.0	0.1	0.0	0.1	0.0	0.1	ns		
	Tzd_8c[2]		0.5	2.2	0.5	2.2	0.5	2.2	0.5	2.2	ns		
EXTCLK[3]	Tper_8d	none	10.0	—	8.33	—	7.5	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
	Tdz_8e[2]		-1.0	-0.1	-1.0	-0.1	-1.0	-0.1	-1.0	-0.1	ns		
	Tzd_8e[2]		0.4	1.0	0.4	1.0	0.4	1.0	0.4	1.0	ns		
BOEN	Tdo_8f	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
	Tdz_8f[2]		0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	ns		
	Tzd_8f[2]		1.1	2.0	1.1	2.0	1.1	2.0	1.1	2.0	ns		
BRN	Tsu_8g	EXTCLK rising	5.5	—	5.5	—	5.5	—	5.5	—	ns		
	Thld_8g		0.0	—	0.0	—	0.0	—	0.0	—	ns		
BGN	Tdo_8h	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	5.8	—	5.8	—	5.8	—	5.8	—	ns		
	Thld_8h		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tpw_8h[2]	none	2(EXT-CLK)	—	2(EXT-CLK)	—	2(EXT-CLK)	—	2(EXT-CLK)	—	ns		
CSN[5:0]	Tdo_8i	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8i[2]		0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	ns		
	Tzd_8i[2]		0.6	2.2	0.6	2.2	0.6	2.2	0.6	2.2	ns		
RWN	Tdo_8j	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8j[2]		-0.7	0.1	-0.7	0.1	-0.7	0.1	-0.7	0.1	ns		
	Tzd_8j[2]		0.6	1.1	0.6	1.1	0.6	1.1	0.6	1.1	ns		
OEN	Tdo_8k	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8k[2]		-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	ns		
	Tzd_8k[2]		0.8	1.5	0.8	1.5	0.8	1.5	0.8	1.5	ns		
BWEN[1:0]	Tdo_8l	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8l[2]		0	0.2	0	0.2	0	0.2	0	0.2	ns		
	Tzd_8l[2]		0.8	1.7	0.8	1.7	0.8	1.7	0.8	1.7	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 3)

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
DMAREQN[1:0]	Tpw_8n[2]	None	2(ICLK)	—	2(ICLK)		2(ICLK)	—	2(ICLK)	—	ns		See Figures 10 and 11.
DMADONEN[1:0]	Tsu_8o	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		
	Thld_8o		1.0	—	1.0	—	1.0	—	1.0	—	ns		
DMAFINN[1:0]	Tdo_8p	EXTCLK rising	1.5	6.0	1.5	6.0	1.5	6.0	1.5	6.0	ns		
CPU, INST	Tdo_8m	EXTCLK rising	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns		See Figures 8 and 9.

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 3 of 3)

1. The RC32438 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32438 are both driving. See Chapter 6, Device Controller, in the RC32438 User Reference Manual.
2. The values for this symbol were determined by calculation, not by testing.
3. The frequency of EXTCLK is programmable. See the External Clock Divider description in Table 3 of this data sheet.
4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

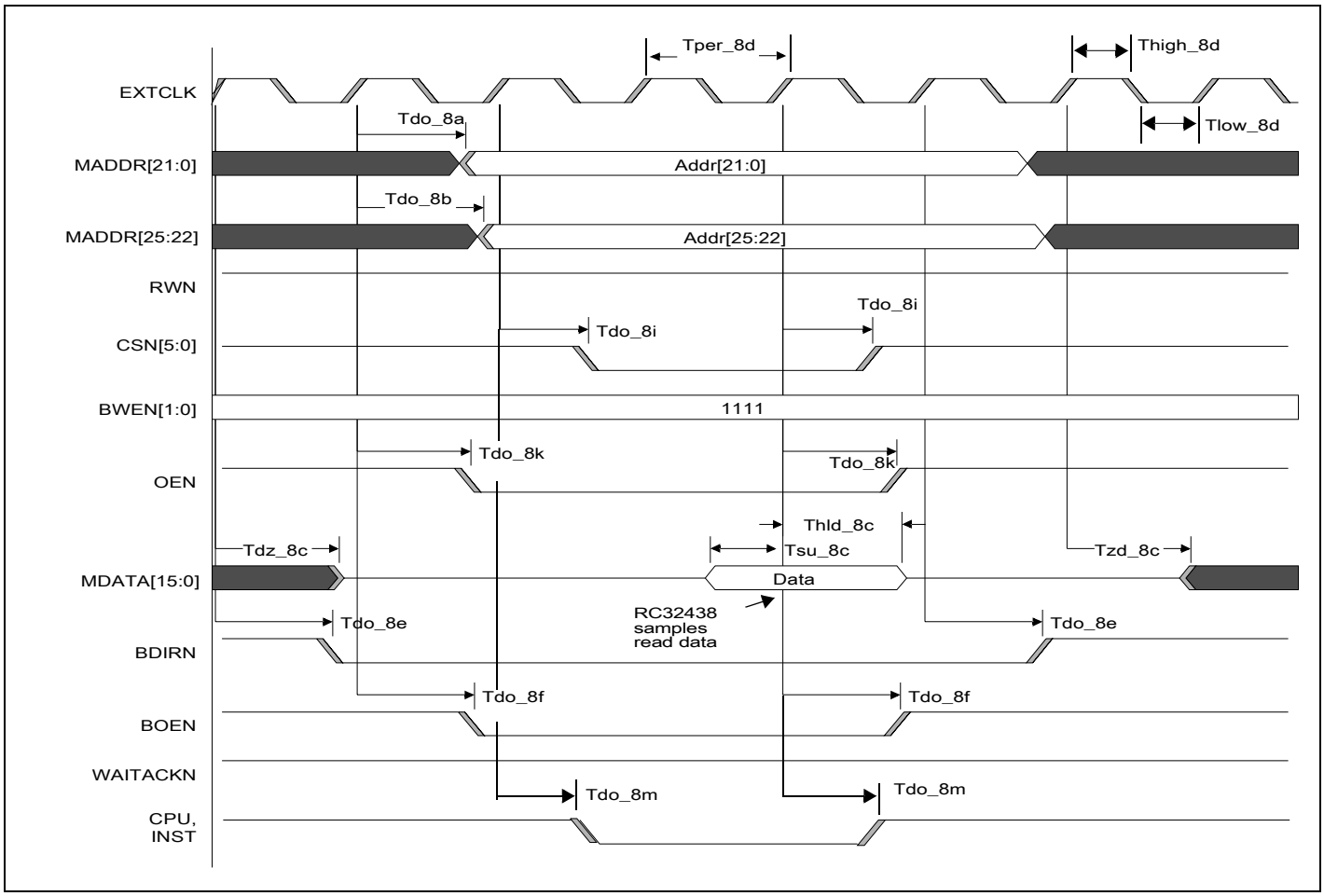


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

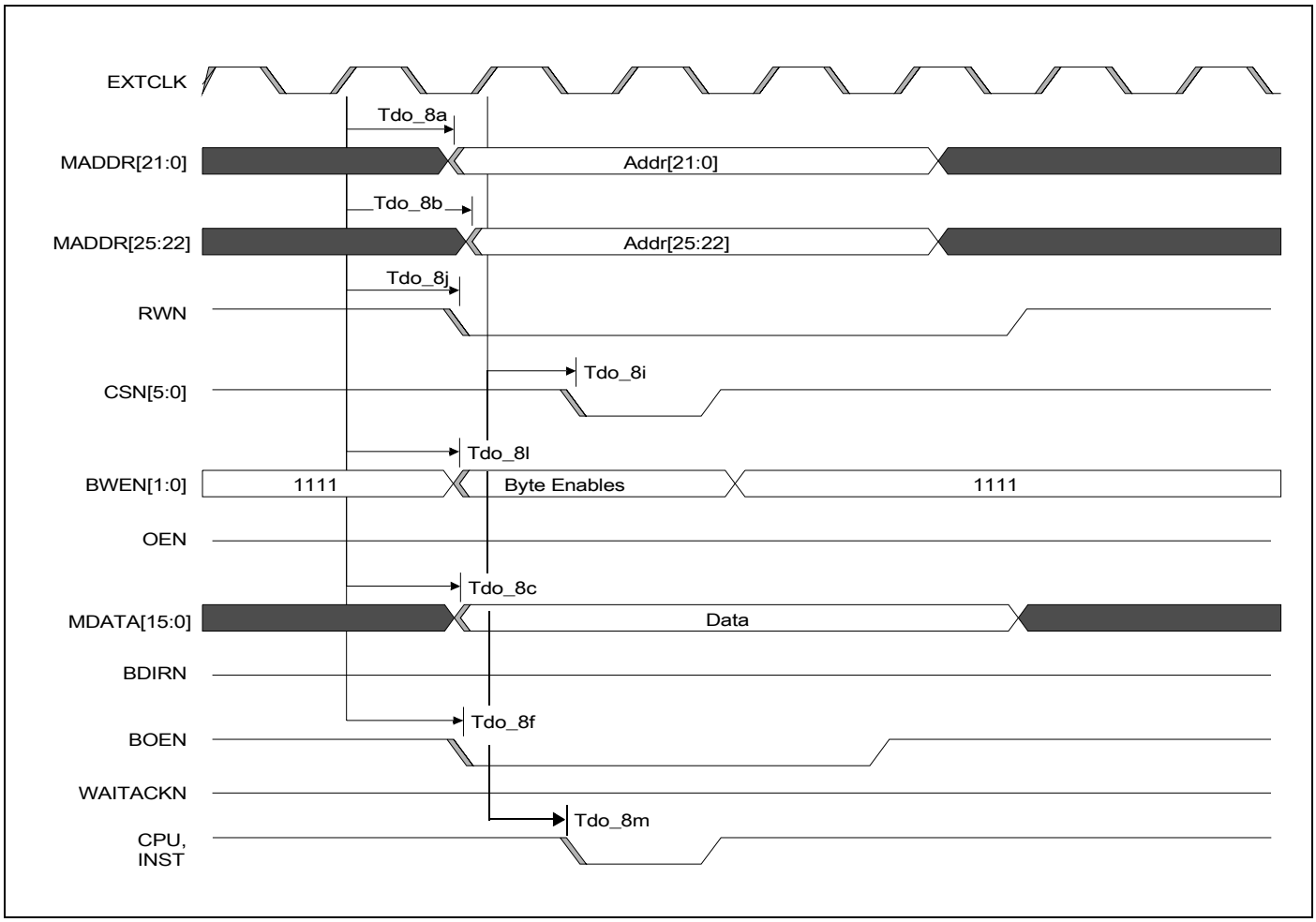


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

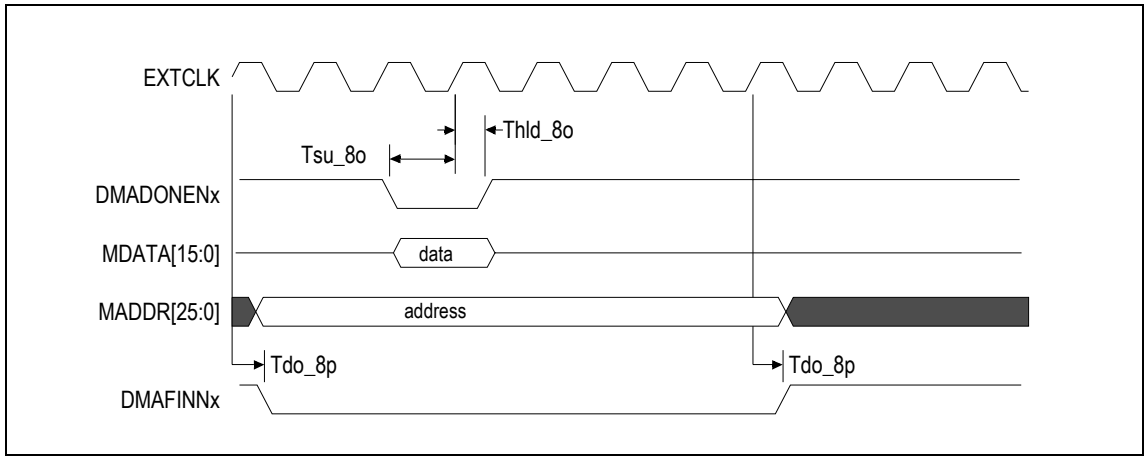


Figure 10 DMADONEN and DMAFINN AC Timing Waveform

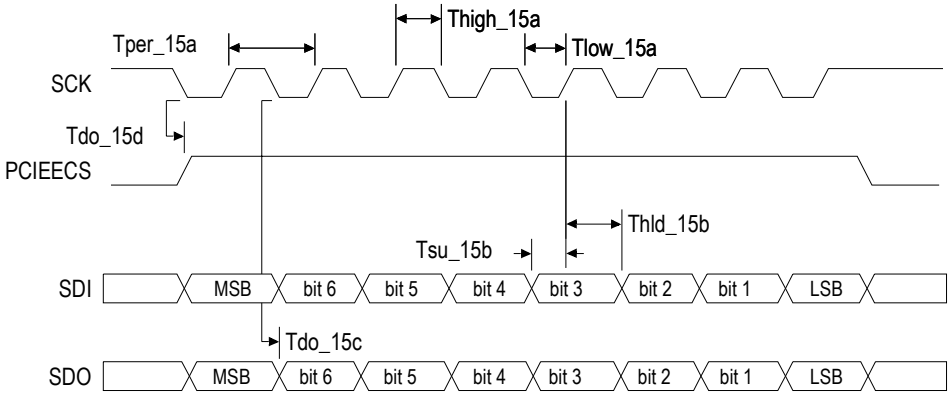
Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	—	1920	—	1920	—	1920	—	1920	ns	33 MHz PCI	See Figures 18, 19, 20 and 21.
	Tper_15a		—	960	—	960	—	960	—	960	ns	66 MHz PCI	
	Tper_15a		100	166667	100	166667	100	166667	100	166667	ns	SPI	
	Thigh_15a, Tlow_15a		930	990	930	990	930	990	930	990	ns	33 MHz PCI	
	Thigh_15a, Tlow_15a		465	495	465	495	465	495	465	495	ns	66 MHz PCI	
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI or PCI	
	Thld_15b		60	—	60	—	60	—	60	—	ns		
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI or PCI	
PCIEECS[2]	Tdo_15d	SCK rising or falling	0	60	0	60	0	60	0	60	ns	PCI	
SCK, SDI, SDO[3]	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

2. PCIEECS is the PCI serial EEPROM chip select. It is an alternate function of PCIGNTN[1].

3. In Bit I/O mode, SCK, SDI, and SDO must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.



Loading PCI configuration registers through SPI from an EEPROM.

Figure 18 SPI AC Timing Waveform — PCI Configurations Load

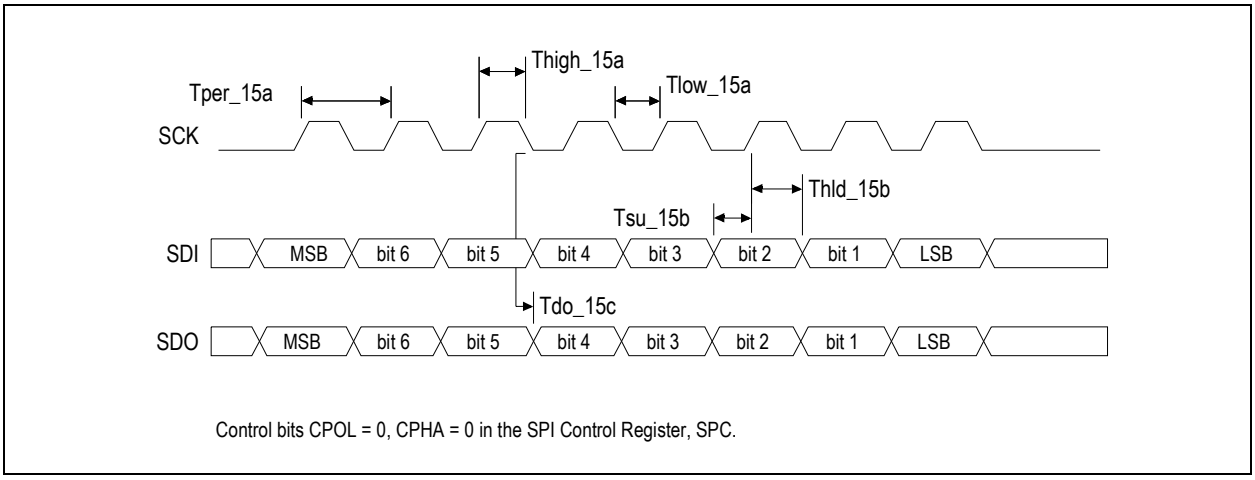


Figure 19 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

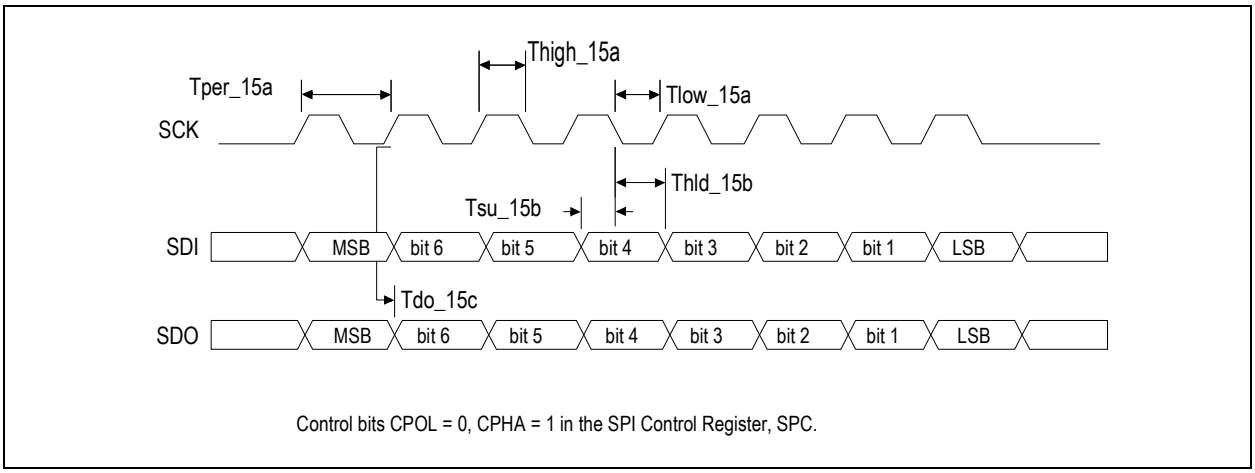


Figure 20 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

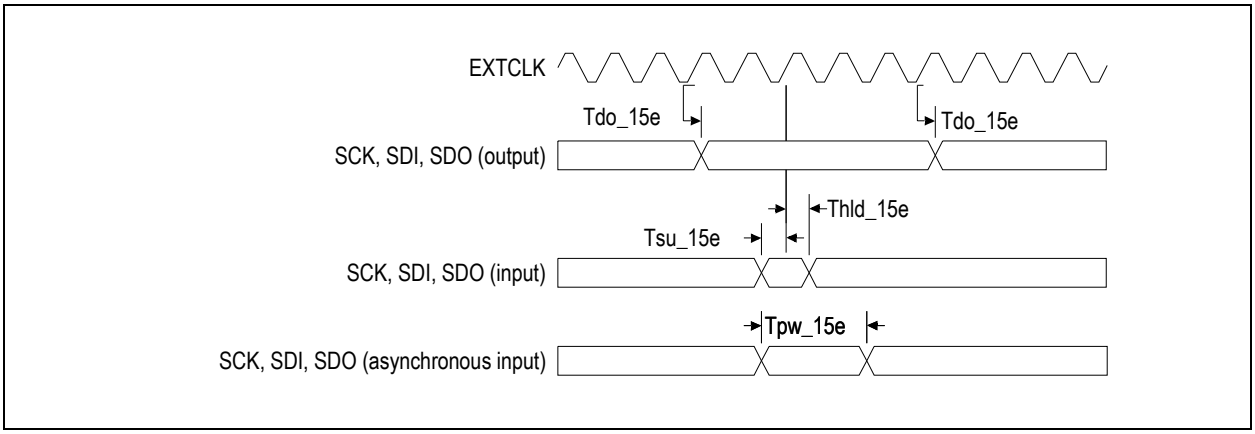


Figure 21 SPI AC Timing Waveform — Bit I/O Mode

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
EJTAG and JTAG													
JTAG_TCK	Tper_16a	none	25.0	50.0	25.0	50.0	25.0	50.0	25.0	50.0	ns		See Figure 22.
	Thigh_16a, Tlow_16a		10.0	25.0	10.0	25.0	10.0	25.0	10.0	25.0	ns		
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	2.4	—	2.4	—	2.4	—	ns		
	Thld_16b		1.0	—	1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	—	11.3	—	11.3	—	11.3	ns		
	Tdz_16c[2]		—	11.3	—	11.3	—	11.3	—	11.3	ns		
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	25.0	—	25.0	—	25.0	—	ns		
EJTAG_TMS[1]	Tsu_16e	JTAG_TCK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
	Thld_6e		1.0	—	1.0	—	1.0	—	1.0	—	ns		
VSENSE	Trise_16f	none	—	2	—	2	—	2	—	2	sec	Measured from 0.5V (T_{active})	See Figure 24.

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

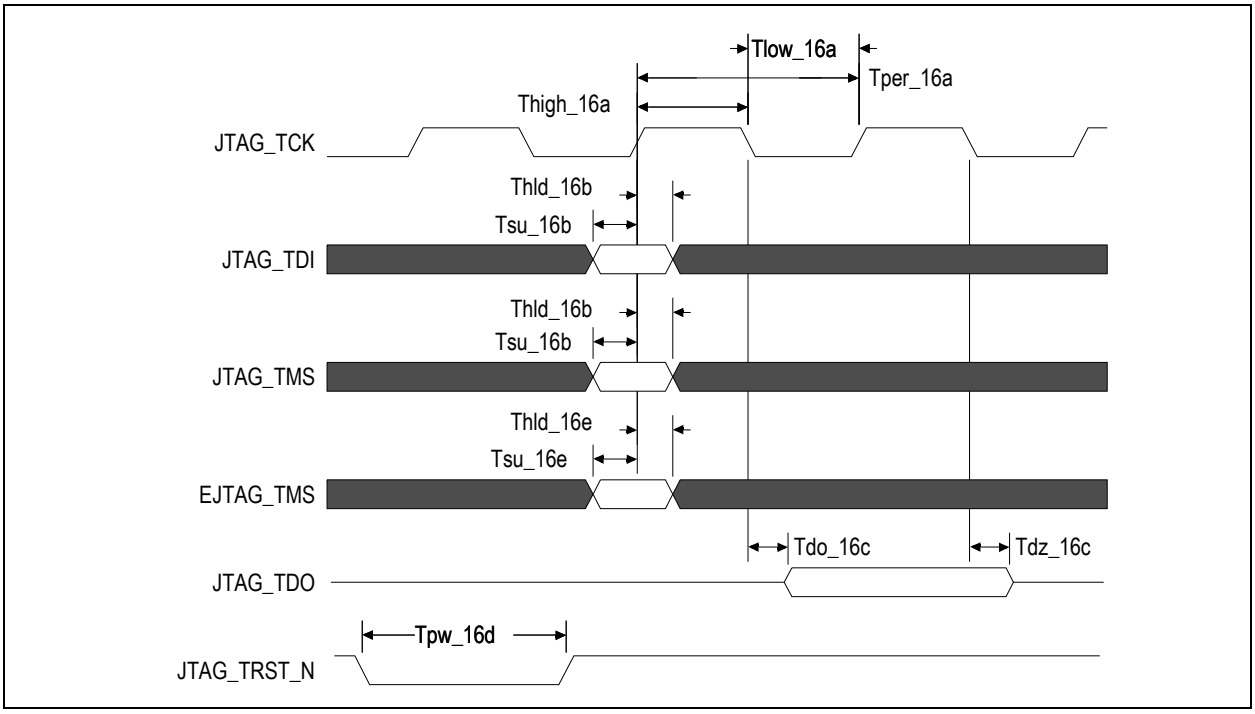


Figure 22 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32438 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 23 shows the electrical connection of the EJTAG probe target system connector.

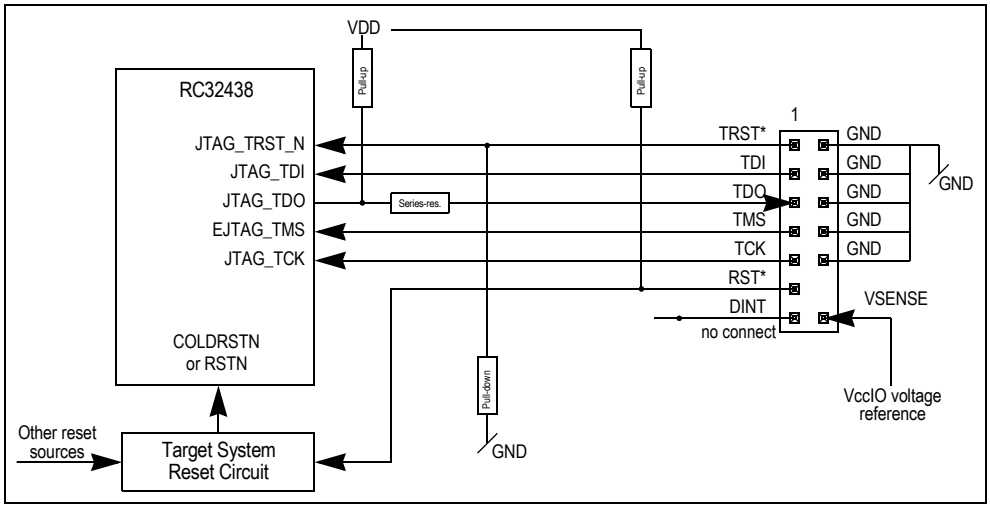


Figure 23 Target System Electrical EJTAG Connection

Power-on Sequence

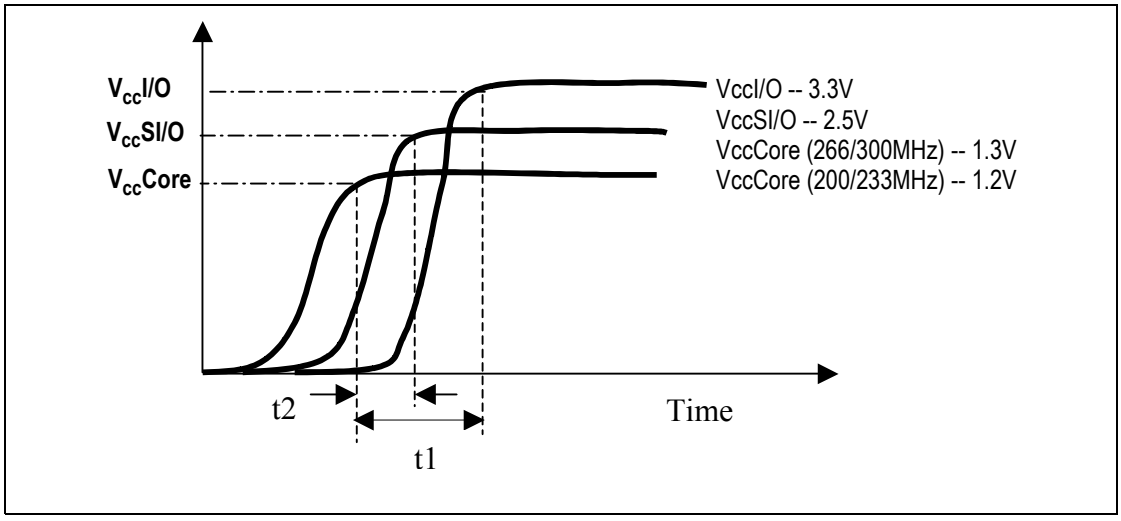
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

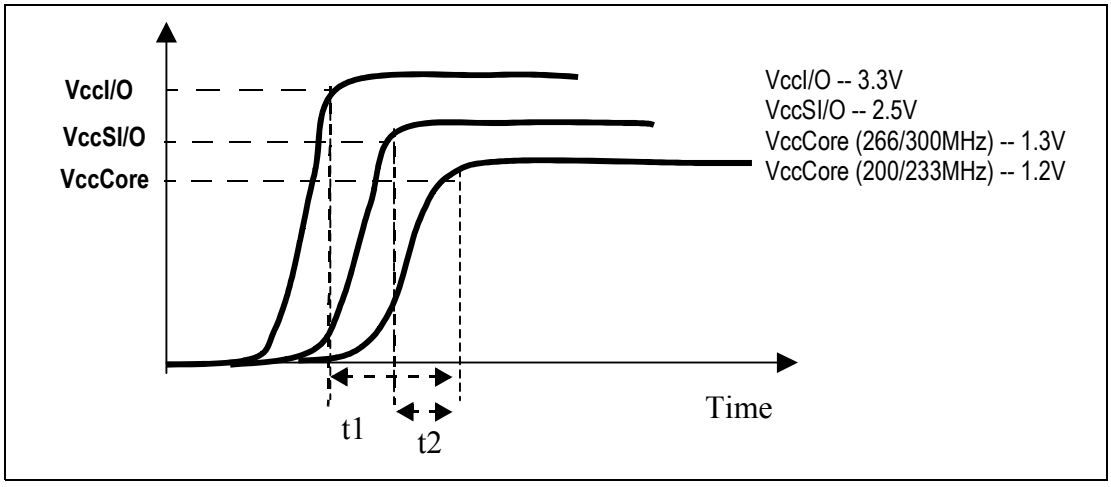
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



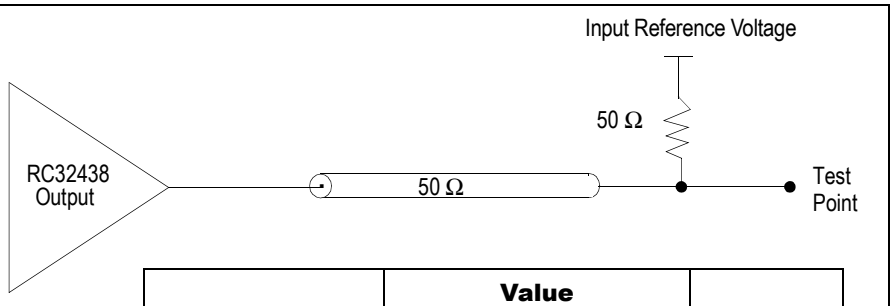
C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

I/O Type	Parameter	Min.	Typical	Max.	Unit	Conditions
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—		mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—		mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	8.0	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs	—	—	± 10	µA	Vcc (max)
	I/O_{LEAK} with Pull-ups/downs	—	—	± 80	µA	Vcc (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

AC Test Conditions



Parameter	Value		Units
	SSTL I/O	Other I/O	
Input pulse levels	0 to 2.5	0 to 3.3	V
Input rise/fall	0.8	1.0	ns
Input reference level	0.5(VccSI/O)	0.5(VccI/O)	V
Output reference levels	1.25	1.5	V
AC test load	35	35	pF

Figure 26 AC Test Conditions

RC32438 Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}	V_{ss} PLL
D4	L10	P13	U15	AA1, AC1
D5	L11	P14	U16	
D6	L12	P15	U17	
D10	L13	P16	U23	
D11	L14	P17	V4	
D12	L15	R3	V23	
D16	L16	R10	W4	
D17	L17	R11	W23	
D18	M10	R12	Y4	
D19	M11	R13	Y23	
E4	M12	R14	AA4	
F4	M13	R15	AA23	
G4	M14	R16	AB4	
G23	M15	R17	AB23	
H4	M16	T10	AC4	
H23	M17	T11	AC5	
J4	N10	T12	AC6	
J23	N11	T13	AC10	
K10	N12	T14	AC11	
K11	N13	T15	AC12	
K12	N14	T16	AC16	
K13	N15	T17	AC17	
K14	N16	U10	AC18	
K15	N17	U11	AC19	
K16	P10	U12		
K17	P11	U13		
K23	P12	U14		

Table 22 RC32438 Ground Pins

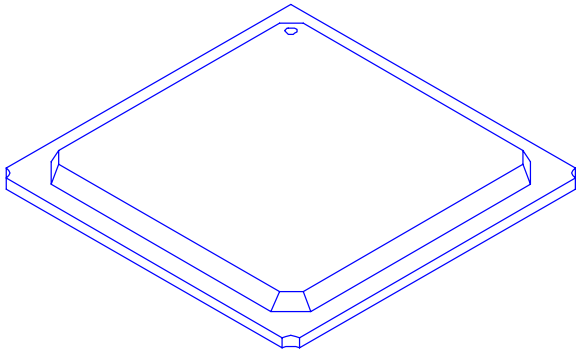
Signal Name	I/O Type	Location	Signal Category
MDATA[02]	I/O	B12	Memory and Peripheral Bus
MDATA[03]	I/O	B10	
MDATA[04]	I/O	C14	
MDATA[05]	I/O	C13	
MDATA[06]	I/O	A12	
MDATA[07]	I/O	A11	
MDATA[08]	I/O	B11	
MDATA[09]	I/O	C11	
MDATA[10]	I/O	A10	
MDATA[11]	I/O	B9	
MDATA[12]	I/O	C10	
MDATA[13]	I/O	B8	
MDATA[14]	I/O	A9	
MDATA[15]	I/O	A8	
MII0CL	I	A1	Ethernet Interfaces
MII0CRS	I	B1	
MII0RXCLK	I	C2	
MII0RXD[00]	I	C1	
MII0RXD[01]	I	D2	
MII0RXD[02]	I	D3	
MII0RXD[03]	I	D1	
MII0RXDV	I	G2	
MII0RXER	I	G1	
MII0TXCLK	I	G3	
MII0TXD[00]	O	E2	
MII0TXD[01]	O	E3	
MII0TXD[02]	O	E1	
MII0TXD[03]	O	F2	
MII0TXENP	O	F3	
MII0TXER	O	F1	
MII1CL	I	H2	
MII1CRS	I	H1	
MII1RXCLK	I	H3	
MII1RXD[00]	I	J2	
MII1RXD[01]	I	J1	

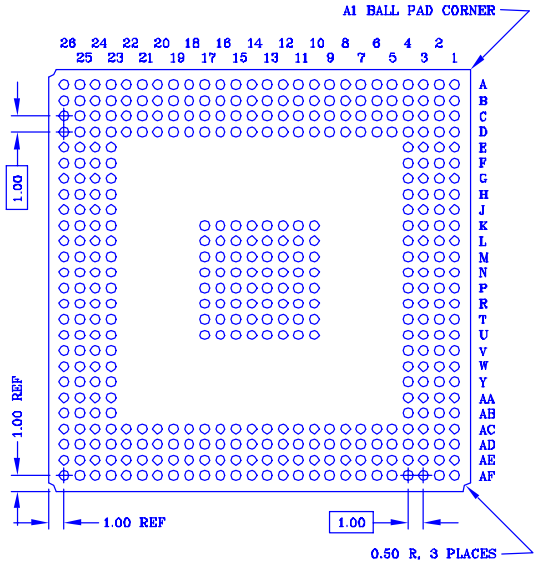
Table 24 RC32438 Alphabetical Signal List (Part 6 of 9)

Signal Name	I/O Type	Location	Signal Category
PCIAD[21]	I/O	AD9	PCI Bus
PCIAD[22]	I/O	AE10	
PCIAD[23]	I/O	AF9	
PCIAD[24]	I/O	AF8	
PCIAD[25]	I/O	AE8	
PCIAD[26]	I/O	AD7	
PCIAD[27]	I/O	AF7	
PCIAD[28]	I/O	AE7	
PCIAD[29]	I/O	AF6	
PCIAD[30]	I/O	AD6	
PCIAD[31]	I/O	AE6	
PCICBEN[00]	I/O	AE21	
PCICBEN[01]	I/O	AE18	
PCICBEN[02]	I/O	AF14	
PCICBEN[03]	I/O	AD8	
PCICLK	I	AD12	
PCIDEVSELN	I/O	AE16	
PCIFRAMEN	I/O	AE15	
PCIGNTN[00]	I/O	AD13	
PCIGNTN[01]	I/O	AE24	
PCIGNTN[02]	I/O	AF24	
PCIGNTN[03]	I/O	AD21	
PCIIRDYN	I/O	AD14	
PCILOCKN	I/O	AE17	
PCIPAR	I/O	AF17	
PCIPERRN	I/O	AD16	
PCIREQN[00]	I/O	AF13	
PCIREQN[01]	I/O	AD11	
PCIREQN[02]	I/O	AE14	
PCIREQN[03]	I/O	AF12	
PCIRSTN	I/O	AE13	
PCISERRN	I/O	AF16	
PCISTOPN	I/O	AD15	
PCITRDYN	I/O	AF15	
RSTN	I/O	A23	System
RWN	O	B3	Memory and Peripheral Bus

Table 24 RC32438 Alphabetical Signal List (Part 8 of 9)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	04/01/02	





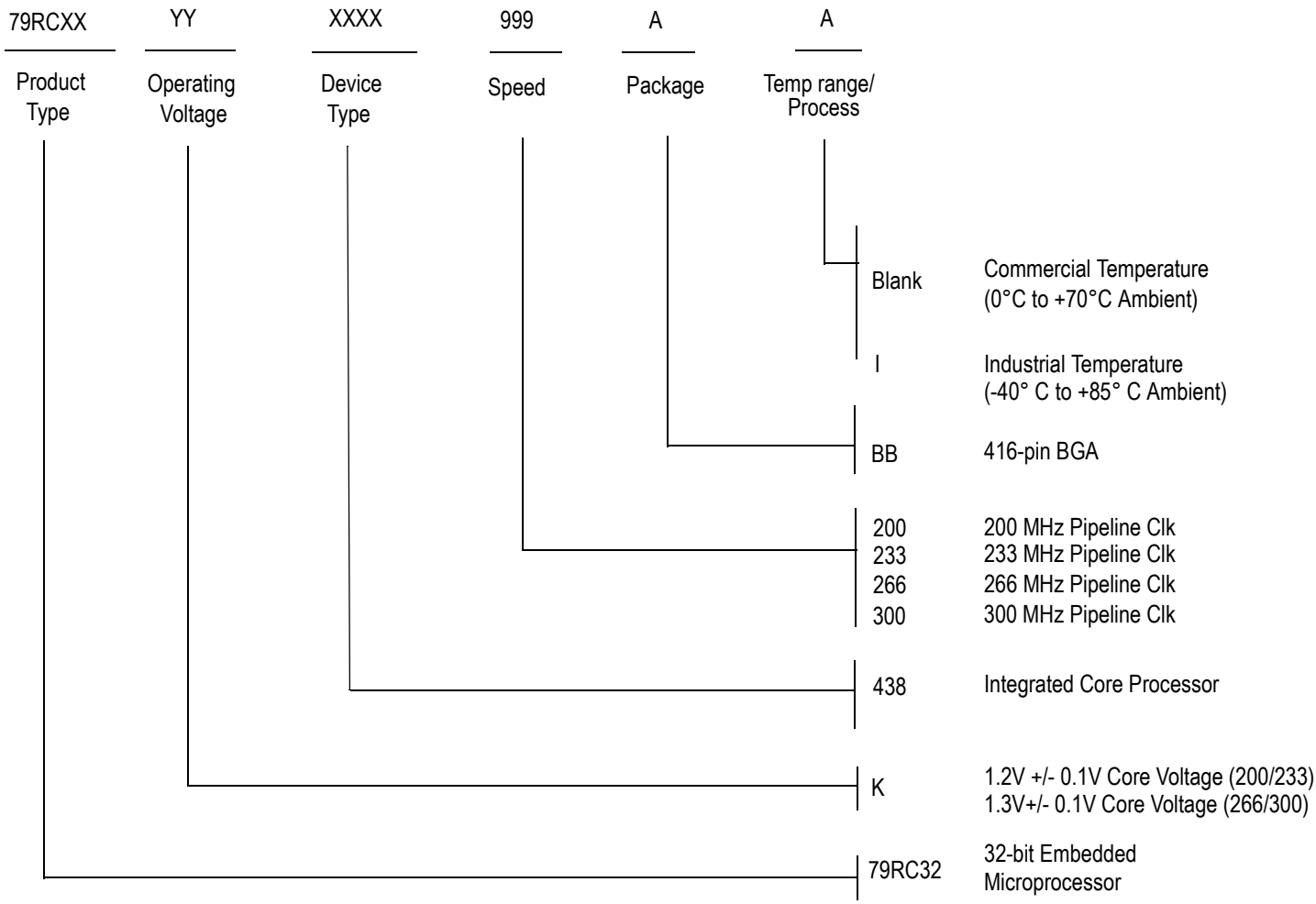
BOTTOM VIEW
(416 SOLDER BALLS)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 26 X 26.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
APPROVALS	DATE	TITLE	BB PACKAGE OUTLINE 27.0 X 27.0 mm BODY PBGA
DRAWN BK	08/06/01		
CHECKED		SIZE C	DRAWING No. PSC-4106 REV 00
DO NOT SCALE DRAWING			SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32K438 -200BB, 233BB, 266BB, 300BB	416-pin BGA package, Commercial Temperature
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