Renesas Electronics America Inc - 79RC32K438-233BBI Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	233MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	416-BGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-233bbi

Pin Description Table

The following table lists the functions of the pins provided on the RC32438. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

Signal	Type	Name/Description
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32438 during a warm reset.
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Memory and peripheral bus external data bus buffer direction control. If the RC32438 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BGN	O	**Bus Grant.** This signal is asserted by the RC32438 to indicate that the RC32438 has relinquished ownership of the memory and peripheral bus.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
BRN	I	**Bus Request.** This signal is asserted by an external device to request ownership of the memory and peripheral bus.
BWEN[1:0]	O	**Byte Write Enables.** These signals are memory and peripheral bus byte write enable signals. BWEN[0] corresponds to byte lane MDATA[7:0] BWEN[1] corresponds to byte lane MDATA[15:8]
CSN[5:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions
MDATA[15:0]	I/O	**Data Bus.** 16-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven on by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.

Table 1 Pin Description (Part 1 of 9)

Signal	Type	Name/Description
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR bus address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable is asserted during normal DDR operation. This signal is negated during following a cold reset or during a power down operation.
DDRCKN[1:0]	O	**DDR Negative DDR clock.** These signals are the negative clock of the differential DDR clock pair. Two copies of this output are provided to reduce signal loading.
DDRCKP[1:0]	O	**DDR Positive DDR clock.** These signals are the positive clock of the differential DDR clock pair. Two copies of this output are provided to reduce signal loading.
DDRCSN[1:0]	O	**DDR Chip Selects.** These active low signals are used to select DDR device(s) on the DDR bus.
DDRDATA[31:0]	I/O	**DDR Data Bus.** 32-bit DDR data bus used to transfer data between the RC32438 and the DDR devices. Data is transferred on both edges of the clock.
DDRDM[7:0]	O	**DDR Data Write Enables.** Byte data write enables used to enable specific byte lanes during DDR writes. DDRDM[0] corresponds to DDRDATA[7:0] DDRDM[1] corresponds to DDRDATA[15:8] DDRDM[2] corresponds to DDRDATA[23:16] DDRDM[3] corresponds to DDRDATA[31:24] DDRDM[4] corresponds to DDRDATA[39:32] DDRDM[5] corresponds to DDRDATA[47:40] DDRDM[6] corresponds to DDRDATA[55:48] DDRDM[7] corresponds to DDRDATA[54:56] (Refer to the DDR Data Bus Multiplexing section in Chapter 7 of the RC32438 User Reference Manual.)
DDRDQS[3:0]	I/O	**DDR Data Strobes.** DDR byte data strobes used to clock data between DDR devices and the RC32438. These strobes are inputs during DDR reads and outputs during DDR writes. DDRDQS[0] corresponds to DDRDATA[7:0]. DDRDQS[1] corresponds to DDRDATA[15:8]. DDRDQS[2] corresponds to DDRDATA[23:16]. DDRDQS[3] corresponds to DDRDATA[31:24].
DDROEN[3:0]	O	**DDR Bus Switch Output Enables.** These pins are used to enable external data bus switches in systems that support data bus multiplexing.
DDRRASN	O	**DDR Row Address Strobe.** The DDR row address strobe is asserted during DDR transactions.

Table 1 Pin Description (Part 2 of 9)

Signal	Type	Name/Description
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI command is driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32438 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted. PCIGNTN[1]: this signal takes on the alternate function of PCIEECS and is used as a PCI Serial EEPROM chip select PCIGNTN[3:2]: unused and driven high. **Note**: When the GPIO register is programmed in the alternate function mode for bits GPIO [26] and [28], these bits become PCIGNTN [4] and [5] respectively.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.

Table 1 Pin Description (Part 3 of 9)

Signal	Type	Name/Description
GPIO[18]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAFINN0 Alternate function: External DMA channel 0 finished output.
GPIO[19]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAFINN1 Alternate function: External DMA channel 1 finished output.
GPIO[20]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address output.
GPIO[21]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address output.
GPIO[22]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address output.
GPIO[23]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address output.
GPIO[24]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4 input or output.
GPIO[25]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: AFSPARE1 Alternate function: *reserved.*
GPIO[26]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4 output.
GPIO[27]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5 input or output.
GPIO[28]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5 output.
GPIO[29]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: Reserved Alternate function: Reserved.

Table 1 Pin Description (Part 6 of 9)

Signal	Type	Name/Description
MII1CRS	I	**Ethernet 1 MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII1RXCLK	I	**Ethernet 1 MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MII1RXD[3:0]	I	**Ethernet 1 MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MII1RXDV	I	**Ethernet 1 MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII1RXER	I	**Ethernet 1 MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII1TXCLK	I	**Ethernet 1 MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII1TXD[3:0]	O	**Ethernet 1 MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MII1TXENP	O	**Ethernet 1 MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MII1TXER	O	**Ethernet 1 MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
JTAG / EJTAG		
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 8 of 9)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Miscellaneous	CLK	I	LVTTL	STI		
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 4 of 4)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.
2. Schmidt Trigger Input (STI).
3. The PCI pins have internal pull-ups but they are too weak to guarantee system validity. Therefore, board pull-ups are mandatory where indicated. GPIO alternate function pins for PCI must also have board pull-ups.
4. PCIMUINTN is an alternate function of GPIO[30]. When configured as an alternate function, this pin is tri-stated when not asserted (i.e., it acts as an open collector output).
5. Use a 2.2K pull-up resistor for I2C pins.

Boot Configuration Vector

The boot configuration vector is read by the RC32438 during a cold reset. The vector defines essential RC32438 parameters that are required once the cold reset completes.

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32438 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MDATA[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.1 in the RC32438 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 6 0x4 - Multiply by 8 0x5 - reserved 0x6 - reserved 0x7 - reserved 0x8 - reserved 0xD - reserved 0xE - reserved 0xF - reserved
MDATA[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MDATA[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian

Table 3 Boot Configuration Encoding (Part 1 of 2)

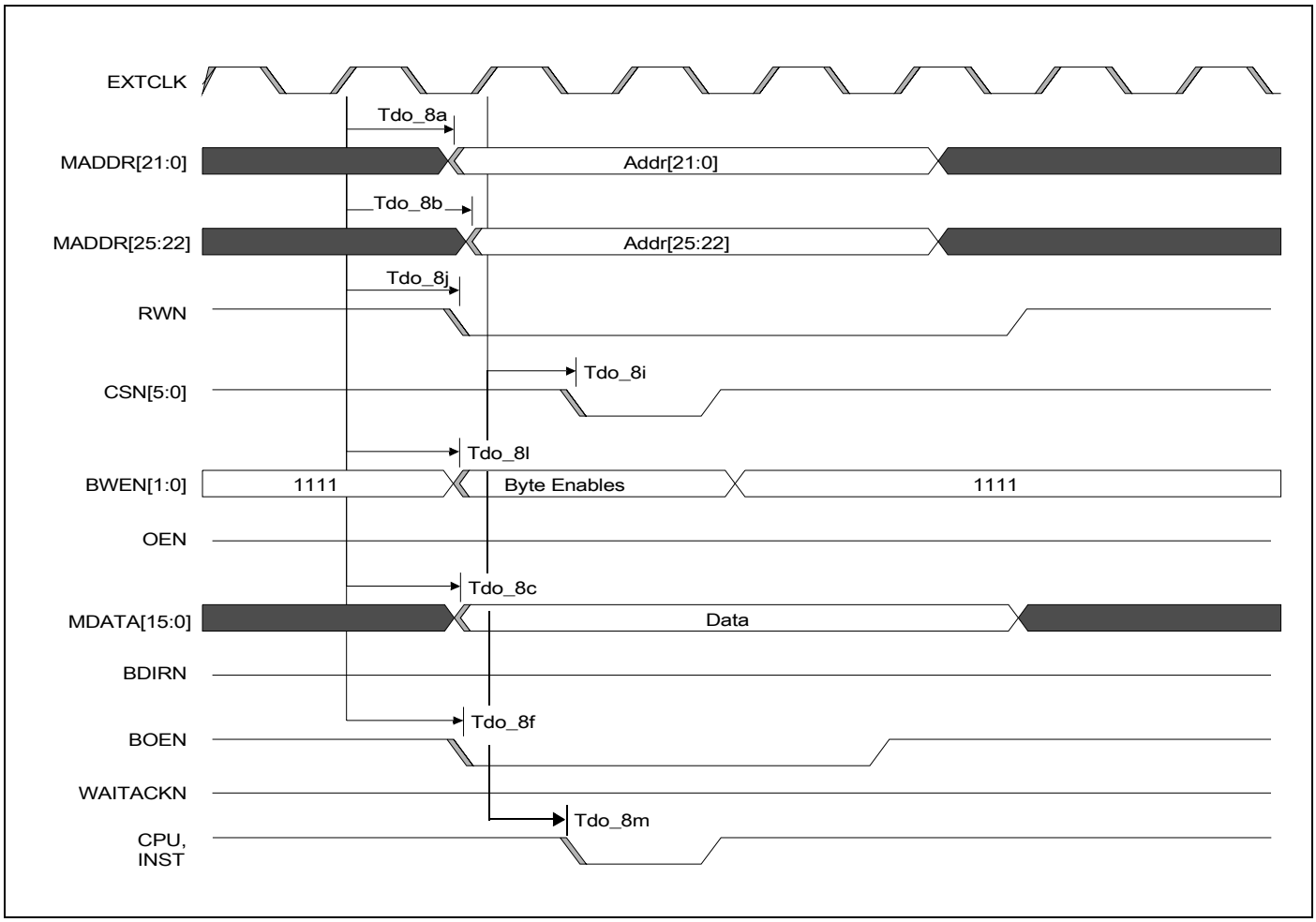


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

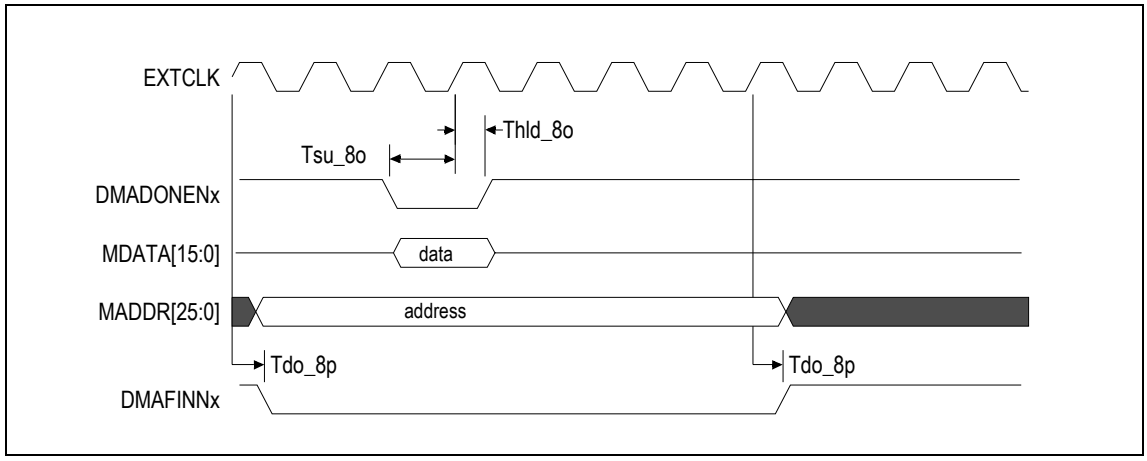


Figure 10 DMADONEN and DMAFINN AC Timing Waveform

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I^2C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 16.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I^2C AC Timing Characteristics

1. For more information, see the I^2C-Bus specification by Philips Semiconductor.

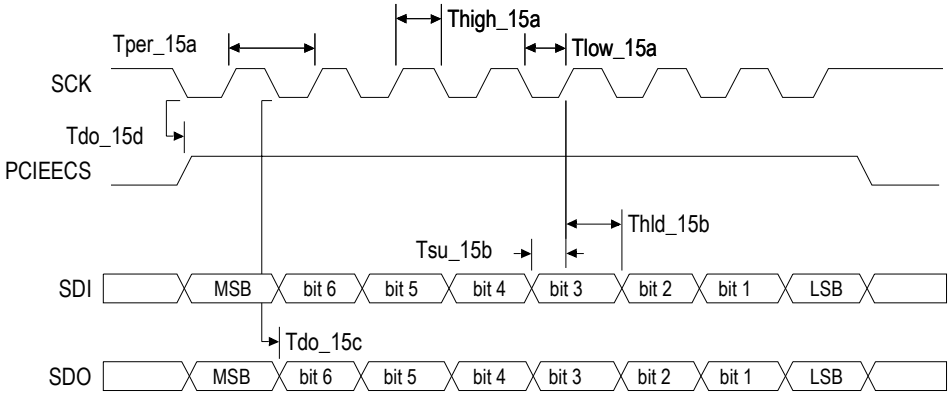
Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	—	1920	—	1920	—	1920	—	1920	ns	33 MHz PCI	See Figures 18, 19, 20 and 21.
	Tper_15a		—	960	—	960	—	960	—	960	ns	66 MHz PCI	
	Tper_15a		100	166667	100	166667	100	166667	100	166667	ns	SPI	
	Thigh_15a, Tlow_15a		930	990	930	990	930	990	930	990	ns	33 MHz PCI	
	Thigh_15a, Tlow_15a		465	495	465	495	465	495	465	495	ns	66 MHz PCI	
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI or PCI	
	Thld_15b		60	—	60	—	60	—	60	—	ns		
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI or PCI	
PCIEECS[2]	Tdo_15d	SCK rising or falling	0	60	0	60	0	60	0	60	ns	PCI	
SCK, SDI, SDO[3]	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

2. PCIEECS is the PCI serial EEPROM chip select. It is an alternate function of PCIGNTN[1].

3. In Bit I/O mode, SCK, SDI, and SDO must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.



Loading PCI configuration registers through SPI from an EEPROM.

Figure 18 SPI AC Timing Waveform — PCI Configurations Load

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
EJTAG and JTAG													
JTAG_TCK	Tper_16a	none	25.0	50.0	25.0	50.0	25.0	50.0	25.0	50.0	ns		See Figure 22.
	Thigh_16a, Tlow_16a		10.0	25.0	10.0	25.0	10.0	25.0	10.0	25.0	ns		
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	2.4	—	2.4	—	2.4	—	ns		
	Thld_16b		1.0	—	1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	—	11.3	—	11.3	—	11.3	ns		
	Tdz_16c[2]		—	11.3	—	11.3	—	11.3	—	11.3	ns		
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	25.0	—	25.0	—	25.0	—	ns		
EJTAG_TMS[1]	Tsu_16e	JTAG_TCK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
	Thld_6e		1.0	—	1.0	—	1.0	—	1.0	—	ns		
VSENSE	Trise_16f	none	—	2	—	2	—	2	—	2	sec	Measured from 0.5V (T_{active})	See Figure 24.

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

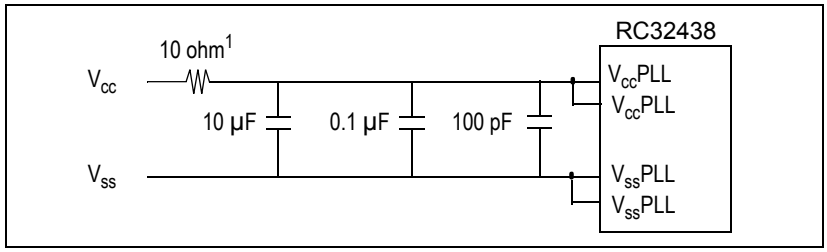


Figure 25 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Clock Speed	Minimum	Typical	Maximum	Unit
V_{ss}	Common ground	All speeds	0	0	0	V
V_{ss}PLL	PLL ground					
V_{cc}I/O	I/O supply except for SSTL_2[1]		3.0	3.3	3.6	V
V_{cc}SI/O	I/O supply for SSTL_2[1]		2.3	2.5	2.7	V
V_{cc}PLL	PLL supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
V_{cc}Core	Internal logic supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
DDRVREF[2]	SSTL_2 input reference voltage	All speeds	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage		DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32438 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.

2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).

3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32438 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32438 IBIS Model on the IDT web site (www.idt.com).

Power-on Sequence

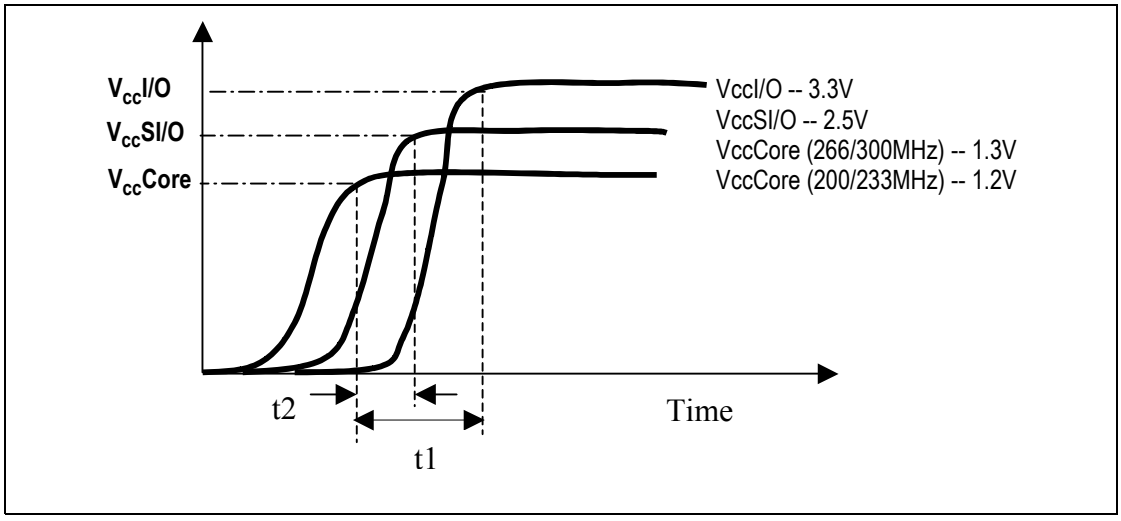
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

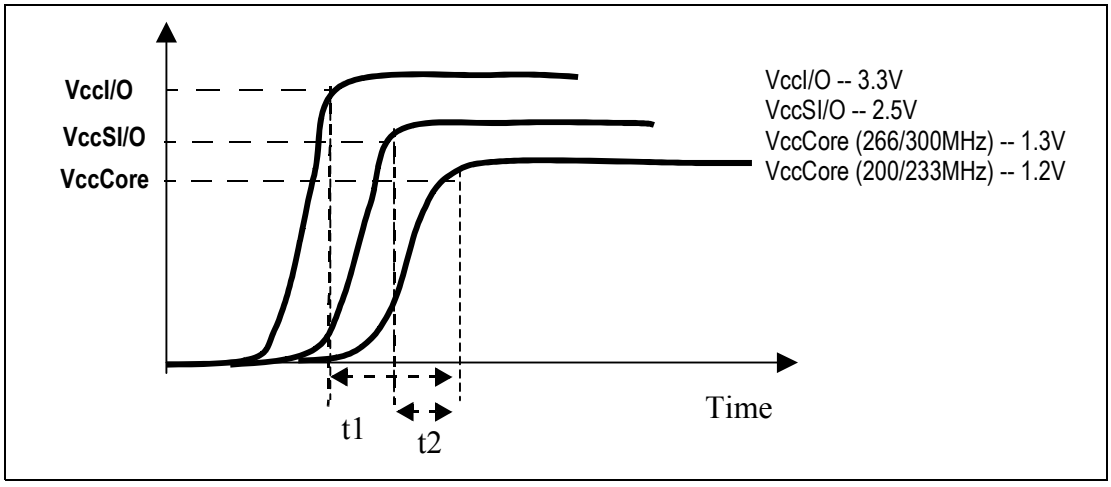
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

Power Consumption

Parameter		200MHz		233MHz		266MHz		300MHz		Unit	Conditions
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{cc} I/O		130	150	180	200	220	250	260	300	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table.
I_{cc} SI/O		100	120	150	170	200	220	250	270	mA	
I_{cc} Core, I_{cc} PLL	Normal mode	460	500	510	550	610	650	680	730	mA	
Power Dissipation	Normal mode	1.2	1.6	1.6	1.9	2.0	2.4	2.4	2.7	W	

Table 17 RC32438 Power Consumption

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-12.0	—	mA	V_{OH} = 1.5V
HIGH Drive Output	I_{OL}	—	24.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-42.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	V_{cc}I/O + 0.5	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	V_{OL} = 0.5V
	I_{OH}	-7.6	—	—	mA	V_{OH} = 1.76V
	V_{IL}	-0.3	—	0.5(V_{cc}SI/O) - 0.18	V	
	V_{IH}	0.5(V_{cc}SI/O) + 0.18	—	V_{cc}SI/O + 0.3	V	

Table 18 DC Electrical Characteristics (Part 1 of 2)

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O	I/O supply for SSTL_2[2]	-0.6	3.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply	-0.6	2.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Signal Name	I/O Type	Location	Signal Category
DDRADDR[00]	O	AC26	DDR Bus
DDRADDR[01]	O	AB25	
DDRADDR[02]	O	AB26	
DDRADDR[03]	O	AA25	
DDRADDR[04]	O	AA26	
DDRADDR[05]	O	Y26	
DDRADDR[06]	O	W25	
DDRADDR[07]	O	W24	
DDRADDR[08]	O	V24	
DDRADDR[09]	O	U26	
DDRADDR[10]	O	T25	
DDRADDR[11]	O	U24	
DDRADDR[12]	O	T26	
DDRADDR[13]	O	R25	
DDRBA[00]	O	Y25	
DDRBA[01]	O	W26	
DDRCASN	O	V26	
DDRCKE	O	K26	
DDRCKN[00]	O	H24	
DDRCKN[01]	O	Y24	
DDRCKP[00]	O	G24	
DDRCKP[01]	O	AA24	
DDRCSN[00]	O	T24	
DDRCSN[01]	O	R26	
DDRDATA[00]	I/O	C23	
DDRDATA[01]	I/O	B23	
DDRDATA[02]	I/O	A24	
DDRDATA[03]	I/O	C24	
DDRDATA[04]	I/O	A25	
DDRDATA[05]	I/O	A26	
DDRDATA[06]	I/O	B26	
DDRDATA[07]	I/O	C26	
DDRDATA[08]	I/O	C25	
DDRDATA[09]	I/O	E24	
DDRDATA[10]	I/O	D26	

Table 24 RC32438 Alphabetical Signal List (Part 2 of 9)

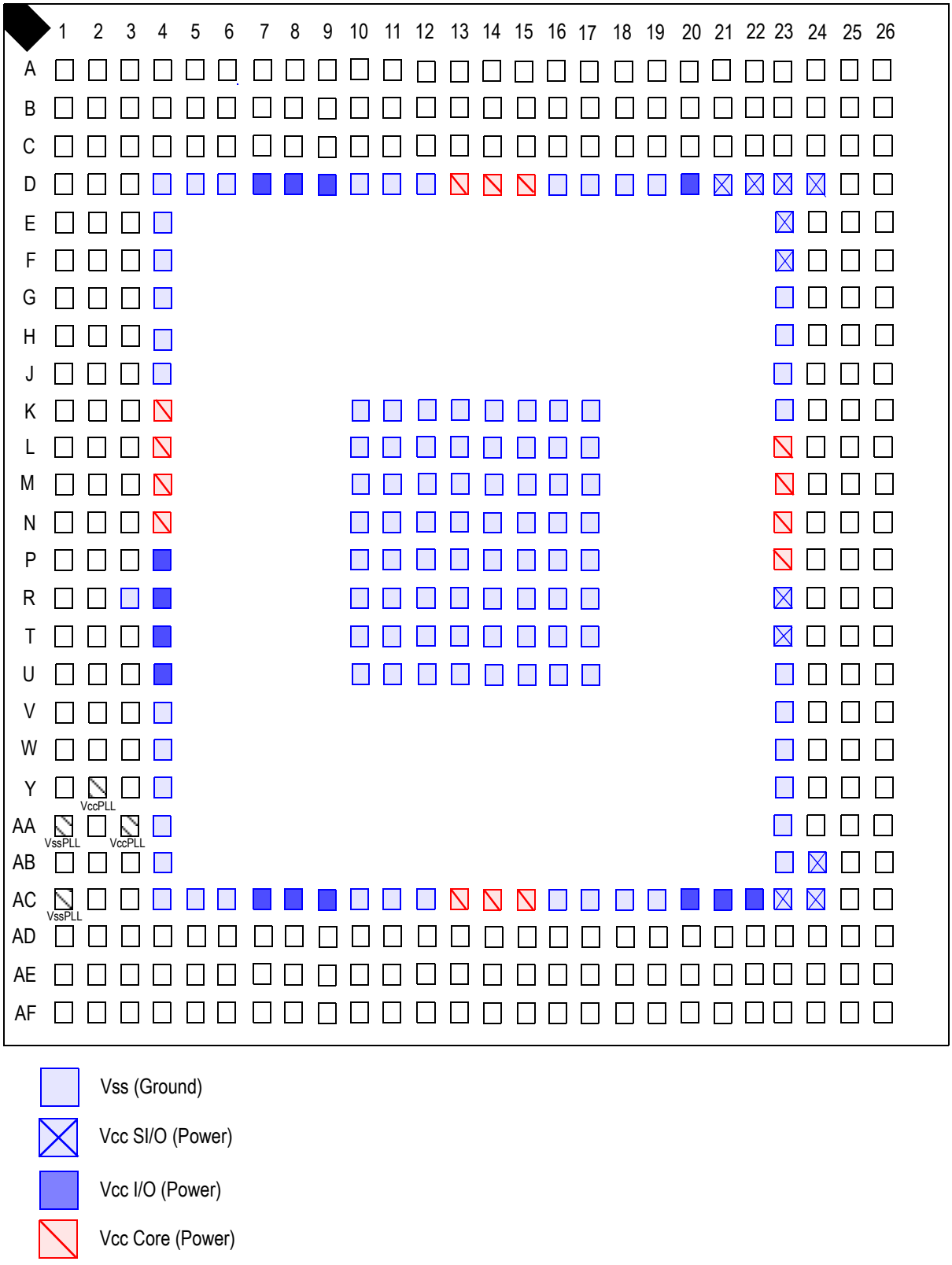
Signal Name	I/O Type	Location	Signal Category
PCIAD[21]	I/O	AD9	PCI Bus
PCIAD[22]	I/O	AE10	
PCIAD[23]	I/O	AF9	
PCIAD[24]	I/O	AF8	
PCIAD[25]	I/O	AE8	
PCIAD[26]	I/O	AD7	
PCIAD[27]	I/O	AF7	
PCIAD[28]	I/O	AE7	
PCIAD[29]	I/O	AF6	
PCIAD[30]	I/O	AD6	
PCIAD[31]	I/O	AE6	
PCICBEN[00]	I/O	AE21	
PCICBEN[01]	I/O	AE18	
PCICBEN[02]	I/O	AF14	
PCICBEN[03]	I/O	AD8	
PCICLK	I	AD12	
PCIDEVSELN	I/O	AE16	
PCIFRAMEN	I/O	AE15	
PCIGNTN[00]	I/O	AD13	
PCIGNTN[01]	I/O	AE24	
PCIGNTN[02]	I/O	AF24	
PCIGNTN[03]	I/O	AD21	
PCIIRDYN	I/O	AD14	
PCILOCKN	I/O	AE17	
PCIPAR	I/O	AF17	
PCIPERRN	I/O	AD16	
PCIREQN[00]	I/O	AF13	
PCIREQN[01]	I/O	AD11	
PCIREQN[02]	I/O	AE14	
PCIREQN[03]	I/O	AF12	
PCIRSTN	I/O	AE13	
PCISERRN	I/O	AF16	
PCISTOPN	I/O	AD15	
PCITRDYN	I/O	AF15	
RSTN	I/O	A23	System
RWN	O	B3	Memory and Peripheral Bus

Table 24 RC32438 Alphabetical Signal List (Part 8 of 9)

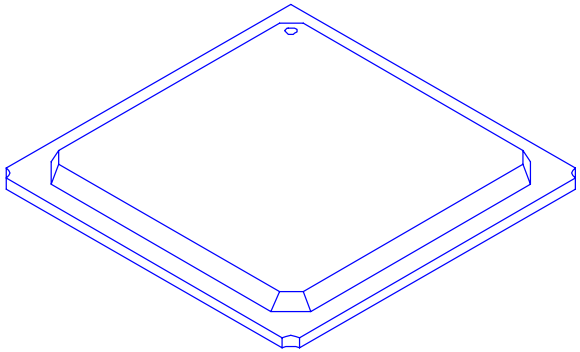
Signal Name	I/O Type	Location	Signal Category
SCK	I/O	W2	SPI Interface
SCL	I/O	AF4	I^2C
SDA	I/O	AD4	
SDI	I/O	V2	SPI Interface
SDO	I/O	V1	
Vcc CORE		D13, D14, D15, K4, L4, L23, M4, M23, N4, N23, P23, AC13, AC14, AC15	
Vcc I/O, Vcc SI/O	See Table 21 for a listing of power pins.		
Vcc PLL			
Vss	See Table 22 for a listing of ground pins.		
Vss PLL			
WAITACKN	I	B2	Memory and Peripheral Bus

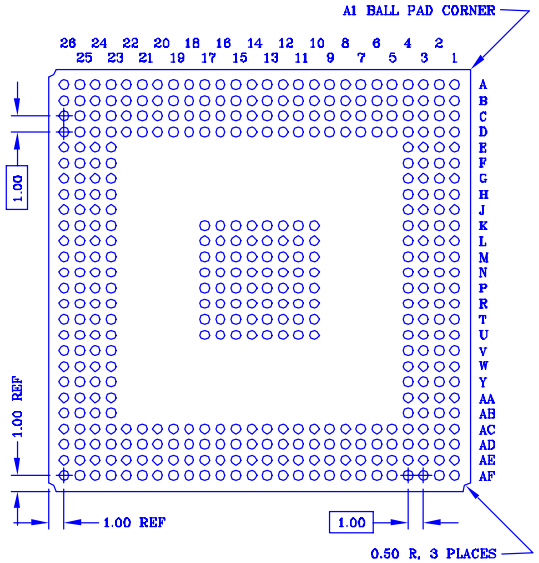
Table 24 RC32438 Alphabetical Signal List (Part 9 of 9)

RC32438 Pinout — Top View



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	04/01/02	





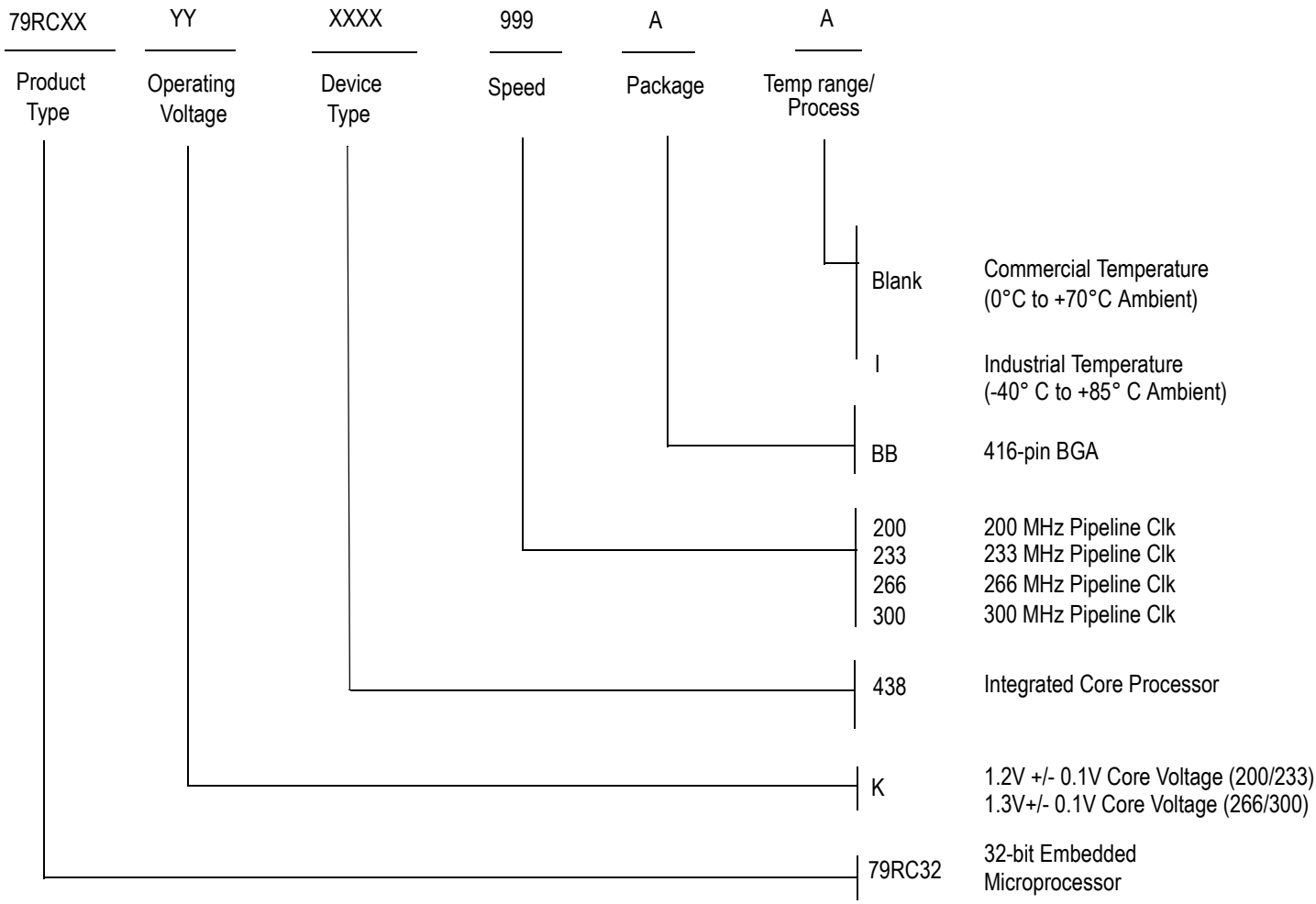
BOTTOM VIEW
(416 SOLDER BALLS)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 26 X 26.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
APPROVALS	DATE	TITLE	BB PACKAGE OUTLINE 27.0 X 27.0 mm BODY PBGA
DRAWN BK	08/06/01		
CHECKED		SIZE C	DRAWING No. PSC-4106 REV 00
DO NOT SCALE DRAWING			SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32K438 -200BB, 233BB, 266BB, 300BB	416-pin BGA package, Commercial Temperature
79RC32K438 -200BBI, 233BBI	416-pin BGA package, Industrial Temperature

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