# Renesas Electronics America Inc - 79RC32K438-266BBGI Datasheet

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 266MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 416-BGA |
| Supplier Device Package | 416-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-266bbgi |

- **DMA Controller**
  - *10 DMA channels: two channels for PCI (PCI to Memory and Memory to PCI), two for each Ethernet interface, two channels for memory to memory operations, two channels for external operations*
  - *Provides flexible descriptor based operation*
  - *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length.*
- **Two Ethernet Interfaces**
  - *10 and 100 Mb/s ISO/IEC 8802-3:1996 compliant*
  - *Two IEEE 802.3u compatible Media Independent Interfaces (MII) with serial management interface*
  - *MII supports IEEE 802.3u auto-negotiation speed selection*
  - *Supports 64 entry hash table based multicast address filtering*
  - *512 byte transmit and receive FIFOs*
  - *Supports flow control functions outlined in IEEE Std. 802.3x-1997*
- **Universal Asynchronous Receiver Transmitter (UART)**
  - *Compatible with the 16550 and 16450 UARTs*
  - *Two completely separate serial channels*
  - *Modem control functions (CTS, RTS, DSR, DTR, RI, DCD)*
  - *16-byte transmit and receive buffers*
  - *Programmable baud rate generator derived from the system clock*
  - *Fully programmable serial characteristics:*
    - *5, 6, 7, or 8 bit characters*
    - *Even, odd or no parity bit generation and detection*
    - *1, 1-1/2 or 2 stop bit generation*
  - *Line break generation and detection*
  - *False start bit detection*
  - *Internal loopback mode*
- **$I^2C$-Bus**
  - *Supports standard 100 Kbps mode as well as 400 Kbps fast mode*
  - *Supports 7-bit and 10-bit addressing*
  - *Supports four modes: master transmitter, master receiver, slave transmitter, slave receiver*
- **Additional General Purpose Peripherals**
  - *Two 16550-compatible serial ports*
  - *Interrupt controller*
  - *System integrity functions*
  - *General purpose I/O controller*
  - *Serial peripheral interface (SPI)*
- **On-chip Memory**
  - *4KB of high speed SRAM organized as 1K x 32 bits*
  - *Supports burst and non-burst byte, halfword, triple-byte, and word CPU, PCI, and DMA accesses*
- **Debug Support**
  - *Rev. 2.6 compliant EJTAG Interface*

# Device Overview

The RC32438 is a member of the IDT™ Interprise™ family of PCI integrated communications processors. It incorporates a high performance CPU core and a number of on-chip peripherals. The integrated processor is designed to transfer information from I/O modules to main memory with minimal CPU intervention using a highly sophisticated direct memory access (DMA) engine. All data transfers through the RC32438 are achieved by writing data from an on-chip I/O peripheral to main memory and then out to another I/O module.

## CPU Execution Core

The 32-bit CPU core is 100% compatible with the MIPS32 instruction set architecture (ISA).

Specifically, this device features the 4Kc CPU core developed by MIPS Technologies Inc. (www.mips.com). This core issues a single instruction per cycle, includes a five stage pipeline, and is optimized for applications that require integer arithmetic. The CPU core includes 16 KB instruction and 16 KB data caches. Both caches are 4-way set associative and can be locked on a per line basis, which allows the programmer control over this precious on-chip memory resource. The core also features a memory management unit (MMU). The CPU core also incorporates an enhanced joint test access group (EJTAG) interface that is used to interface to in-circuit emulator tools, providing access to internal registers and enabling the part to be controlled externally, simplifying the system debug process. The use of this core allows IDT's customers to leverage the broad range of software and development tools available for the MIPS architecture, including operating systems, compilers, and in-circuit emulators.

## Double Data Rate Memory Controller

The RC32438 incorporates a high performance double data rate (DDR) memory controller which supports both x16 and x32 memory configurations up to 2GB. This module provides all of the signals required to interface to both memory modules and discrete devices, including two chip selects, differential clocking outputs and data strobes.

## Memory and I/O Controller

The RC32438 uses a dedicated local memory/IO controller including a de-multiplexed 16-bit data and 26-bit address bus. It includes all of the signals required to interface directly to as many as six Intel or Motorola-style external peripherals, and the interface can be configured to support both 8-bit and 16-bit peripherals.

## DMA Controller

The DMA controller consists of 10 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

## PCI Interface

The PCI interface on the RC32438 is compatible with version 2.2 of the PCI specification. An on-chip arbiter supports up to six external bus masters, supporting both fixed priority and rotating priority arbitration schemes. The part can support both satellite and host PCI configurations, enabling the RC32438 to act as a slave controller for a PCI add-in

| Signal | Type | Name/Description |
|---|---|---|
| DDRVREF | I | **DDR Voltage Reference.** SSTL_2 DDR voltage reference generated by an external source. |
| DDRWEN | O | **DDR Write Enable.** DDR write enable is asserted during DDR write transactions. |
| **PCI Bus** | | |
| PCIAD[31:0] | I/O | **PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads. |
| PCICBEN[3:0] | I/O | **PCI Multiplexed Command/Byte Enable Bus**. PCI command is driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s). |
| PCICLK | I | **PCI Clock**. Clock used for all PCI bus transactions. |
| PCIDEVSELN | I/O | **PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces. |
| PCIFRAMEN | I/O | **PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data. |
| PCIGNTN[3:0] | I/O | **PCI Bus Grant**.<br>**In PCI host mode with internal arbiter:**<br>The assertion of these signals indicates to the agent that the internal RC32438 arbiter has granted the agent access to the PCI bus.<br>**In PCI host mode with external arbiter:**<br>PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted.<br>PCIGNTN[3:1]: unused and driven high.<br>**In PCI satellite mode:**<br>PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32438 that access to the PCI bus has been granted.<br>PCIGNTN[1]: this signal takes on the alternate function of PCIEECS and is used as a PCI Serial EEPROM chip select<br>PCIGNTN[3:2]: unused and driven high.<br>**Note**: When the GPIO register is programmed in the alternate function mode for bits GPIO [26] and [28], these bits become PCIGNTN [4] and [5] respectively. |
| PCIIRDYN | I/O | **PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete. |
| PCILOCKN | I/O | **PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring. |
| PCIPAR | I/O | **PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase. |
| PCIPERRN | I/O | **PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received. |

**Table 1 Pin Description (Part 3 of 9)**

| Signal | Type | Name/Description |
|---|---|---|
| GPIO[18] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: DMAFINN0<br>Alternate function: External DMA channel 0 finished output. |
| GPIO[19] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: DMAFINN1<br>Alternate function: External DMA channel 1 finished output. |
| GPIO[20] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin<br>Alternate function pin name: MADDR[22]<br>Alternate function: Memory and peripheral bus address output. |
| GPIO[21] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: MADDR[23]<br>Alternate function: Memory and peripheral bus address output. |
| GPIO[22] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: MADDR[24]<br>Alternate function: Memory and peripheral bus address output. |
| GPIO[23] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: MADDR[25]<br>Alternate function: Memory and peripheral bus address output. |
| GPIO[24] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PCIREQN[4]<br>Alternate function: PCI Request 4 input or output. |
| GPIO[25] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: AFSPARE1<br>Alternate function: *reserved.* |
| GPIO[26] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PCIGNTN[4]<br>Alternate function: PCI Grant 4 output. |
| GPIO[27] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PCIREQN[5]<br>Alternate function: PCI Request 5 input or output. |
| GPIO[28] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: PCIGNTN[5]<br>Alternate function: PCI Grant 5 output. |
| GPIO[29] | I/O | **General Purpose I/O.**<br>This pin can be configured as a general purpose I/O pin.<br>Alternate function pin name: Reserved<br>Alternate function: Reserved. |

**Table 1 Pin Description (Part 6 of 9)**

| Signal | Type | Name/Description |
|---|---|---|
| MII1CRS | I | **Ethernet 1 MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle. |
| MII1RXCLK | I | **Ethernet 1 MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data. |
| MII1RXD[3:0] | I | **Ethernet 1 MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY. |
| MII1RXDV | I | **Ethernet 1 MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus. |
| MII1RXER | I | **Ethernet 1 MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus. |
| MII1TXCLK | I | **Ethernet 1 MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data. |
| MII1TXD[3:0] | O | **Ethernet 1 MII Transmit Data.** This nibble wide data bus contains the data to be transmitted. |
| MII1TXENP | O | **Ethernet 1 MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission. |
| MII1TXER | O | **Ethernet 1 MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters. |
| MIIMDC | O | **MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface. |
| MIIMDIO | I/O | **MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY. |
| **JTAG / EJTAG** | | |
| EJTAG_TMS | I | **EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high. |
| JTAG_TCK | I | **JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle. |
| JTAG_TDI | I | **JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller. |
| JTAG_TDO | O | **JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated. |
| JTAG_TMS | I | **JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high. |

**Table 1 Pin Description (Part 8 of 9)**

| Signal | Name/Description |
|---|---|
| MDATA[7] | **Boot Device Width**. This field specifies the width of the boot device (i.e., Device 0).<br>0x0 - 8-bit boot device width<br>0x1 - 16-bit boot device width |
| MDATA[8] | **Reset Mode**. This bit specifies the length of time the RSTN signal is driven.<br>0x0 - Normal reset: RSTN driven for minimum of 4096 clock cycles<br>0x1 - reserved |
| MDATA[11:9] | **PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode.<br>0x0 - Disabled (EN initial value is zero)<br>0x1 - PCI satellite mode with PCI target not ready (EN initial value is one)<br>0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one)<br>0x3 - PCI host mode with external arbiter (EN initial value is zero)<br>0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero)<br>0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero)<br>0x6 - *reserved*<br>0x7 - *reserved* |
| MDATA[12] | **Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset.<br>0x0 - Watchdog timer enabled<br>0x1 - Watchdog timer disabled |
| MDATA[15:13] | **Reserved**. These pins must be driven low during boot configuration. |

**Table 3 Boot Configuration Encoding (Part 2 of 2)**

# AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

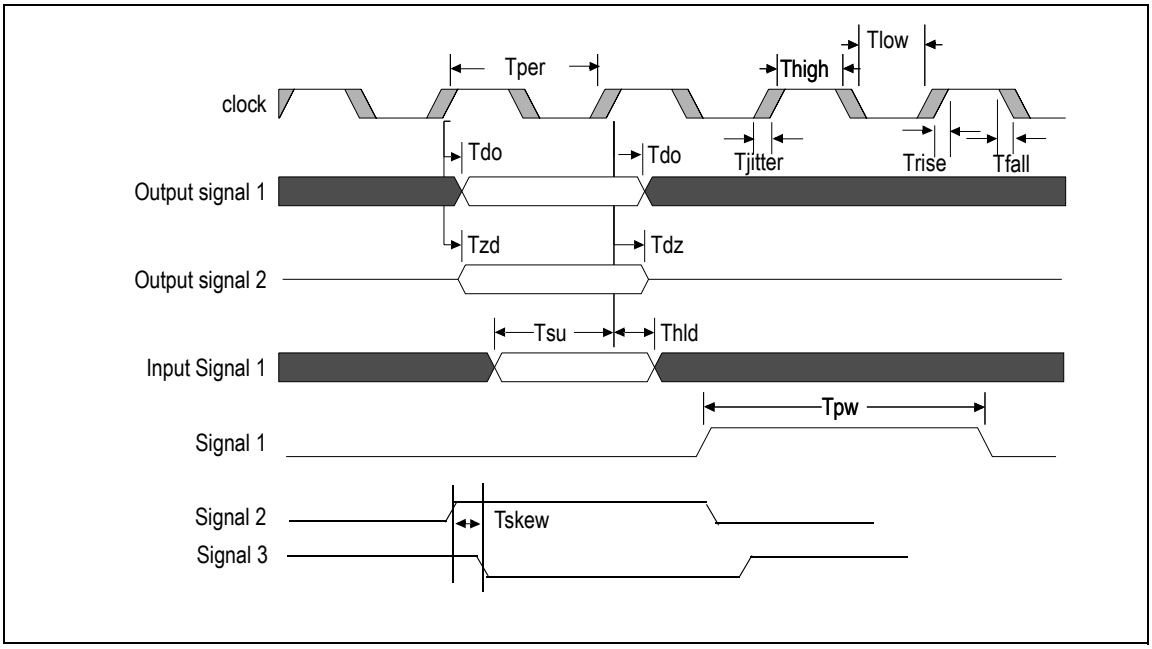
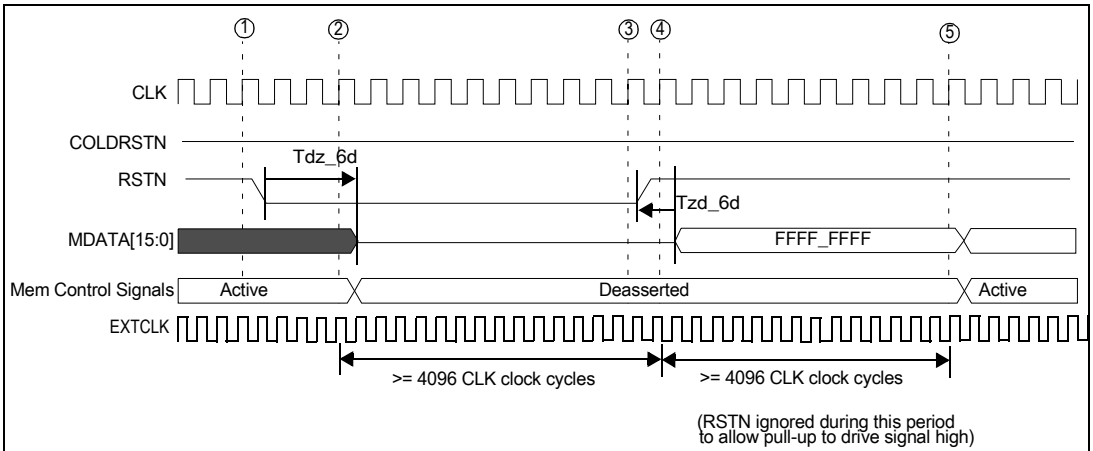



**Figure 2 AC Timing Definitions Waveform**

| Symbol | Definition |
|---|---|
| Tper | Clock period. |
| Tlow | Clock low. Amount of time the clock is low in one clock period. |
| Thigh | Clock high. Amount of time the clock is high in one clock period. |
| Trise | Rise time. Low to high transition time. |
| Tfall | Fall time. High to low transition time. |
| Tjitter | Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges. |
| Tdo | Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data. |
| Tzd | Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid. |
| Tdz | Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated. |
| Tsu | Input set-up. Amount of time before the reference clock edge that the input must be valid. |
| Thld | Input hold. Amount of time after the reference clock edge that the input must remain valid. |
| Tpw | Pulse width. Amount of time the input or output is active for asynchronous signals. |
| Tslew | Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high. |
| X(clock) | Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200. |
| Tskew | Skew. The amount of time two signal edges deviate from one another. |

**Table 4 AC Timing Definitions**




1. Warm reset caused by any of the conditions listed in the Warm Reset section of Chapter 3, Clocking and Initialization, in the RC32438 User Reference Manual.
2. The RC32438 tri-states the data bus, MDATA[15:0], and negates all memory control signals.
3. The RC32438 negates RSTN.
4. The RC32438 starts driving the data bus, MDATA[15:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

**Figure 5 Warm Reset AC Timing Waveform**

| Signal | Symbol[1] | Reference Edge | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **Memory Bus - DDR Access** | | | | | | | | | | | | | |
| DDRDATA[31:0] | Tskew_7g[2] | DDRDQSx | 0.0 | 0.9 | 0.0 | 0.9 | 0.0 | 0.9 | 0.0 | 0.8 | ns | | See Figures 6 and 7. |
| | Tdo_7k[3] | | 1.5 | 3.3 | 1.1 | 2.9 | 0.9 | 2.7 | 0.7 | 2.4 | ns | | |
| DDRDM[7:0] | Tdo_7l | DDRDQSx | 1.5 | 3.3 | 1.1 | 2.9 | 0.9 | 2.7 | 0.7 | 2.4 | ns | | |
| DDRDQS[3:0] | Tac | DDRCKPx | -0.75 | 0.75 | -0.75 | 0.75 | -0.75 | 0.75 | -0.75 | 0.75 | ns | | |
| DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN[1:0], DDROEN[3:0], DDRRASN, DDRWEN | Tdo_7m[4] | DDRCKPx | 1.1 | 4.5 | 1.1 | 4.5 | 1.1 | 4.5 | 1.1 | 4.5 | ns | | |

**Table 7 DDR SDRAM Timing Characteristics**

1. In the DDR data sheet: Tskew_7g = $t_{DQSQ;}$ Tdo_7k = $t_{DH}$, $t_{DS;}$ Tdo_7l = $t_{DH}$, $t_{DS;}$ Tac = $t_{AC;}$ Tdo_7m = $t_{IH}$, $t_{IS.}$

2. Meets DDR timing requirements for DDR 266 SDRAMs with 400 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32438 DDR layout guidelines are followed.

3. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.5ns, the $T_{IS}$ parameter is 7.5ns minus 4.5ns = 3ns. The DDR spec for this parameter is 1ns, so there is 2ns of slack left over for board propagation. Calculations for $T_{DS}$ are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 2.7ns, we have 3.75ns minus 2.7ns = 1.05ns for $T_{DS}$. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 0.55ns slack for board propagation delays.

| Signal | Symbol | Reference Edge | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| MDATA[15:0] | Tsu_8c | EXTCLK rising | 7.0 | — | 7.0 | — | 7.0 | — | 7.0 | — | ns | | See Figures 8 and 9 (cont.) |
| | Thld_8c | | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns | | |
| | Tdo_8c | | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | ns | | |
| | Tdz_8c[2] | | 0.0 | 0.1 | 0.0 | 0.1 | 0.0 | 0.1 | 0.0 | 0.1 | ns | | |
| | Tzd_8c[2] | | 0.5 | 2.2 | 0.5 | 2.2 | 0.5 | 2.2 | 0.5 | 2.2 | ns | | |
| EXTCLK[3] | Tper_8d | none | 10.0 | — | 8.33 | — | 7.5 | — | 6.66 | — | ns | | |
| BDIRN | Tdo_8e | EXTCLK rising | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns | | |
| | Tdz_8e[2] | | -1.0 | -0.1 | -1.0 | -0.1 | -1.0 | -0.1 | -1.0 | -0.1 | ns | | |
| | Tzd_8e[2] | | 0.4 | 1.0 | 0.4 | 1.0 | 0.4 | 1.0 | 0.4 | 1.0 | ns | | |
| BOEN | Tdo_8f | EXTCLK rising | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns | | |
| | Tdz_8f[2] | | 0.1 | 0.4 | 0.1 | 0.4 | 0.1 | 0.4 | 0.1 | 0.4 | ns | | |
| | Tzd_8f[2] | | 1.1 | 2.0 | 1.1 | 2.0 | 1.1 | 2.0 | 1.1 | 2.0 | ns | | |
| BRN | Tsu_8g | EXTCLK rising | 5.5 | — | 5.5 | — | 5.5 | — | 5.5 | — | ns | | |
| | Thld_8g | | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns | | |
| BGN | Tdo_8h | EXTCLK rising | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns | | |
| WAITACKN[4] | Tsu_8h | EXTCLK rising | 5.8 | — | 5.8 | — | 5.8 | — | 5.8 | — | ns | | |
| | Thld_8h | | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns | | |
| | Tpw_8h[2] | none | 2(EXT-CLK) | — | 2(EXT-CLK) | — | 2(EXT-CLK) | — | 2(EXT-CLK) | — | ns | | |
| CSN[5:0] | Tdo_8i | EXTCLK rising | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | ns | | |
| | Tdz_8i[2] | | 0.1 | 0.4 | 0.1 | 0.4 | 0.1 | 0.4 | 0.1 | 0.4 | ns | | |
| | Tzd_8i[2] | | 0.6 | 2.2 | 0.6 | 2.2 | 0.6 | 2.2 | 0.6 | 2.2 | ns | | |
| RWN | Tdo_8j | EXTCLK rising | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | ns | | |
| | Tdz_8j[2] | | -0.7 | 0.1 | -0.7 | 0.1 | -0.7 | 0.1 | -0.7 | 0.1 | ns | | |
| | Tzd_8j[2] | | 0.6 | 1.1 | 0.6 | 1.1 | 0.6 | 1.1 | 0.6 | 1.1 | ns | | |
| OEN | Tdo_8k | EXTCLK rising | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | ns | | |
| | Tdz_8k[2] | | -0.4 | 0.2 | -0.4 | 0.2 | -0.4 | 0.2 | -0.4 | 0.2 | ns | | |
| | Tzd_8k[2] | | 0.8 | 1.5 | 0.8 | 1.5 | 0.8 | 1.5 | 0.8 | 1.5 | ns | | |
| BWEN[1:0] | Tdo_8l | EXTCLK rising | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | 0.0 | 4.0 | ns | | |
| | Tdz_8l[2] | | 0 | 0.2 | 0 | 0.2 | 0 | 0.2 | 0 | 0.2 | ns | | |
| | Tzd_8l[2] | | 0.8 | 1.7 | 0.8 | 1.7 | 0.8 | 1.7 | 0.8 | 1.7 | ns | | |

**Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 3)**

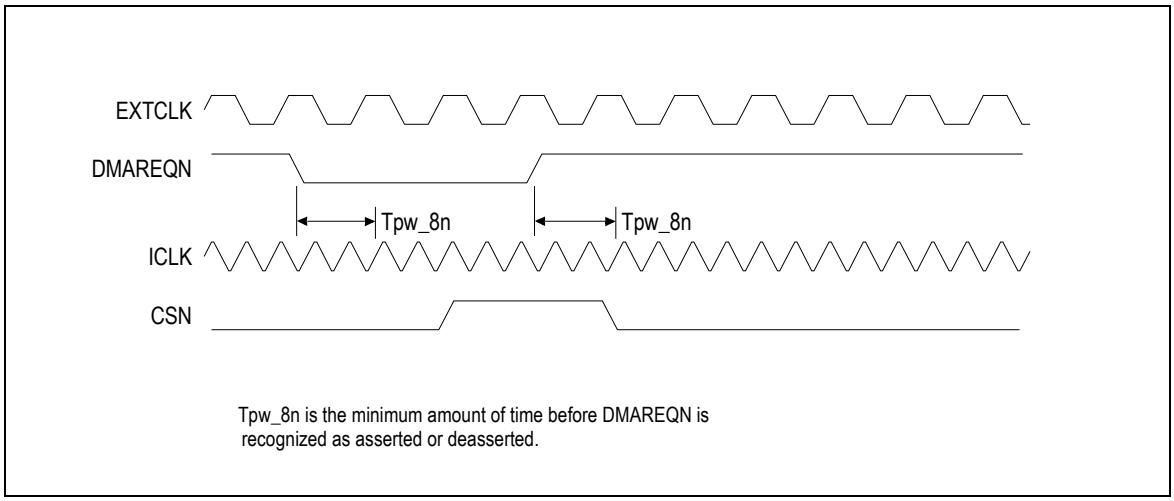



**Figure 11 DMAREQN AC Timing Waveform**

| Signal | Symbol | Reference Edge | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **Ethernet**[1] | | | | | | | | | | | | | |
| MIIMDC | Tper_9a | None | 40.0 | — | 33.3 | — | 30.0 | — | 30.0 | — | ns | | See Figure 12. |
| | Thigh_9a, Tlow_9a | | 16.0 | — | 13.0 | — | 12.0 | — | 12.0 | — | ns | | |
| MIIMDIO | Tsu_9b | MIIMDC rising | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| | Thld_9b | | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns | | |
| | Tdo_9b[2] | | 10 | 300 | 10 | 300 | 10 | 300 | 10 | 300 | ns | | |
| MIIxRXCLK, MIIxTXCLK[3] | Tper_9c | None | 399.96 | 400.4 | 399.96 | 400.4 | 399.96 | 400.4 | 399.96 | 400.4 | ns | 10 Mbps | |
| | Thigh_9c, Tlow_9c | | 140 | 260 | 140 | 260 | 140 | 260 | 140 | 260 | ns | | |
| | Trise_9c, Tfall_9c | | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | ns | | |
| MIIxRXCLK, MIIxTXCLK[3] | Tper_9d | None | 39.9 | 40.0 | 39.9 | 40.0 | 39.9 | 40.0 | 39.9 | 40.0 | ns | 100 Mbps | |
| | Thigh_9d, Tlow_9d | | 14.0 | 26.0 | 14.0 | 26.0 | 14.0 | 26.0 | 14.0 | 26.0 | ns | | |
| | Trise_9d, Tfall_9d | | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | ns | | |
| MIIxRXD[3:0], MIIxRXDV, MIIxRXER | Tsu_9e | MIIxRXCLK rising | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| | Thld_9e | | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| MIIxTXD[3:0], MIIxTXENP, MIIxTXER | Tdo_9f | MIIxTXCLK rising | 0.0 | 25.0 | 0.0 | 25.0 | 0.0 | 25.0 | 0.0 | 25.0 | ns | | |

**Table 9 Ethernet AC Timing Characteristics**

1. There are two MII interfaces and the timing is the same for each. "X" represents interface 0 or 1.

2. The values for this symbol were determined by calculation, not by testing.

| Signal | Symbol | Reference Edge | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **PCI**[1] | | | | | | | | | | | | | |
| PCICLK[2] | Tper_10a | none | 15.0 | 30.0 | 15.0 | 30.0 | 15.0 | 30.0 | 15.0 | 30.0 | ns | 66 MHz PCI | See Figure 13. |
| | Thigh_10a, Tlow_10a | | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns | | |
| | Tslew_10a | | 1.5 | 4.0 | 1.5 | 4.0 | 1.5 | 4.0 | 1.5 | 4.0 | V/ns | | |
| PCIAD[31:0], PCIBEN[3:0], PCIDEVSELN, PCIFRAMEN,PCIIRDYN, PCILOCKN, PCIPAR, PCIPERRN, PCISTOPN, PCITRDY | Tsu_10b | PCICLK rising | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns | | |
| | Thld_10b | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | See Figure 13 (cont.) |
| | Tdo_10b | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| | Tdz_10b[3] | | — | 14.0 | — | 14.0 | — | 14.0 | — | 14.0 | ns | | |
| | Tzd_10b[3] | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | | |
| PCIGNTN[3:0], PCIREQN[3:0] | Tsu_10c | PCICLK rising | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | ns | | |
| | Thld_10c | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_10c | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| PCIRSTN (output)[4] | Tpw_10d[3] | None | 4000 (CLK) | — | 4000 (CLK) | — | 4000 (CLK) | — | 4000 (CLK) | — | ns | | See Figures 15 and 16 |
| PCIRSTN (input)[4,5] | Tpw_10e[3] | None | 2(CLK) | — | 2(CLK) | — | 2(CLK) | — | 2(CLK) | — | ns | | |
| | Tdz_10e[3] | PCIRSTN falling | 6(CLK) | — | 6(CLK) | — | 6(CLK) | — | 6(CLK) | — | ns | | |
| PCISERRN[6] | Tsu_10f | PCICLK rising | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns | | See Figure 13 |
| | Thld_10f | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_10f | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| PCIMUINTN[6] | Tdo_10g | PCICLK rising | 4.7 | 11.1 | 4.7 | 11.1 | 4.7 | 11.1 | 4.7 | 11.1 | ns | | |

**Table 10 PCI AC Timing Characteristics**

1. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2.

2. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66MHz.

3. The values for this symbol were determined by calculation, not by testing.

4. PCIRSTN is an output in host mode and an input in satellite mode.

5. To meet the PCI delay specification from reset asserted to outputs floating, the PCI reset should be logically combined with the COLDRSTN input, instead of input on PCIRSTN.

6. PCISERRN and PCIMUINTN use open collector I/O types.

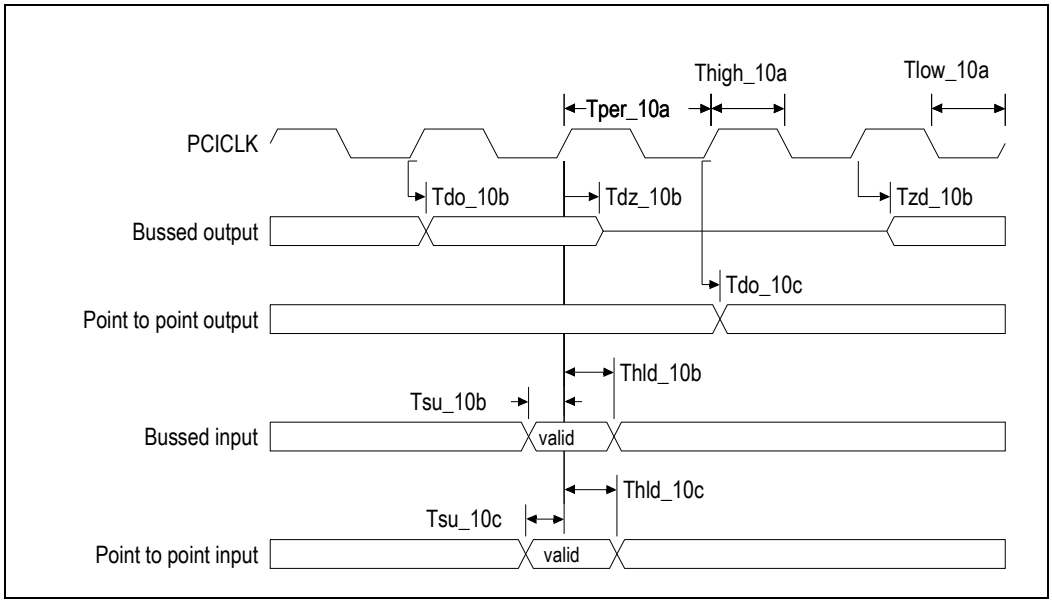



**Figure 13 PCI AC Timing Waveform**

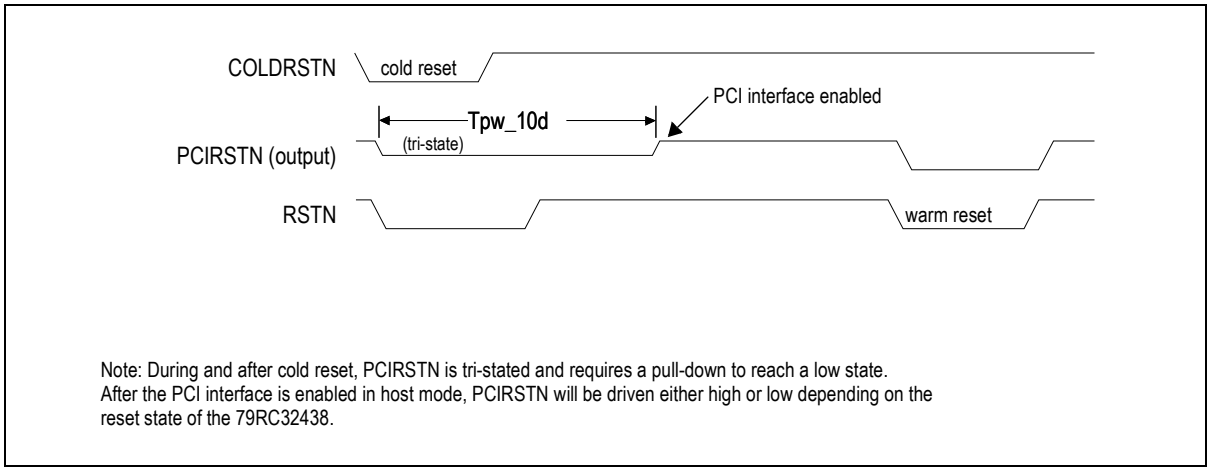



**Figure 14 PCI AC Timing Waveform — PCI Reset in Host Mode**

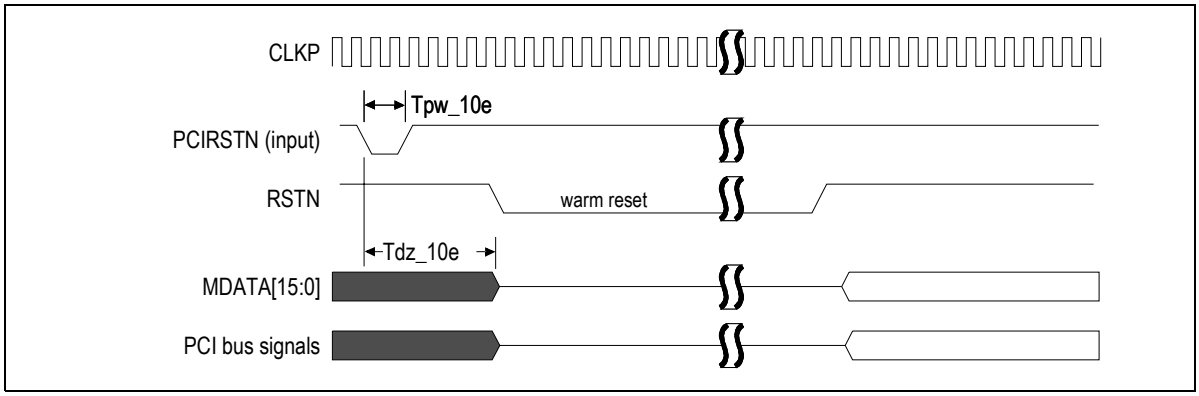



**Figure 15 PCI AC Timing Waveform — PCI Reset in Satellite Mode**

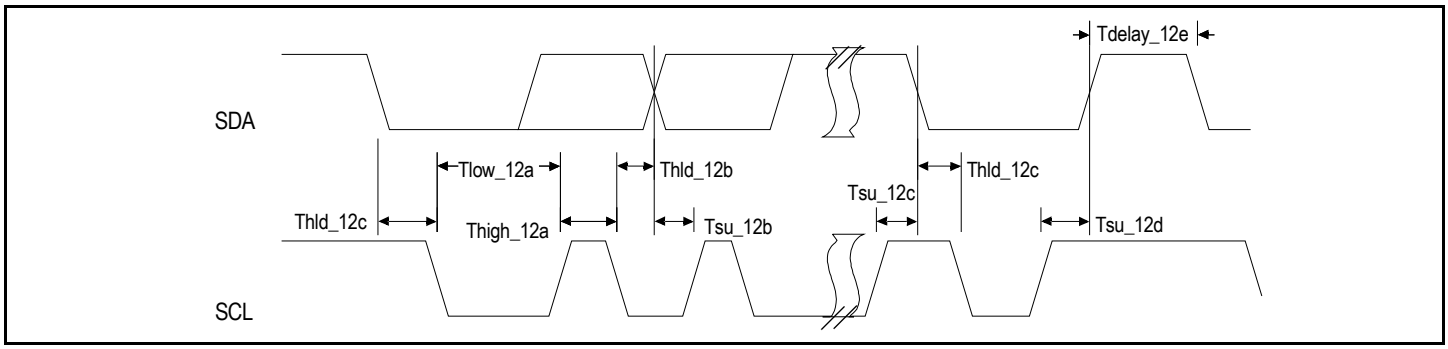



**Figure 16 I²C AC Timing Waveform**

| Signal | Symbol | Reference Edge | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **GPIO** | | | | | | | | | | | | | |
| GPIO[31:0][1] | Tpw_13b[2] | None | 2(ICLK) | — | 2(ICLK) | — | 2(ICLK) | — | 2(ICLK) | — | ns | | See Figure 17. |

**Table 12 GPIO AC Timing Characteristics**

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

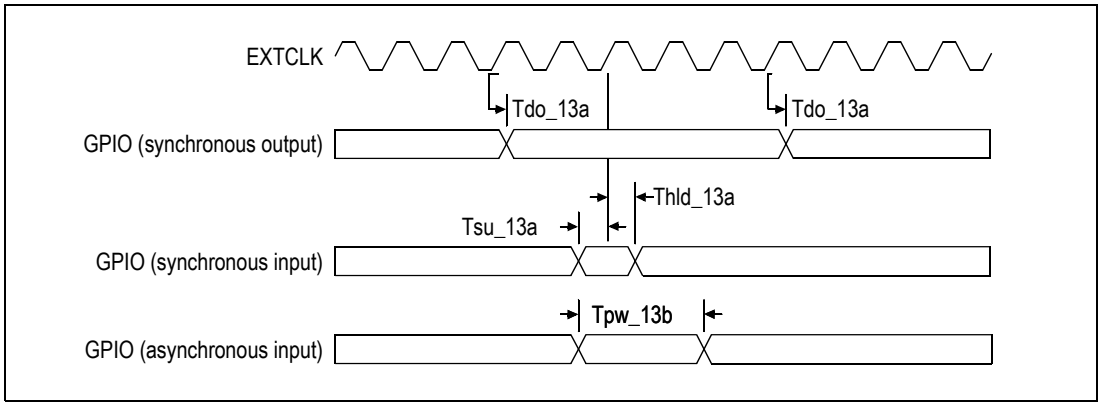



**Figure 17 GPIO AC Timing Waveform**

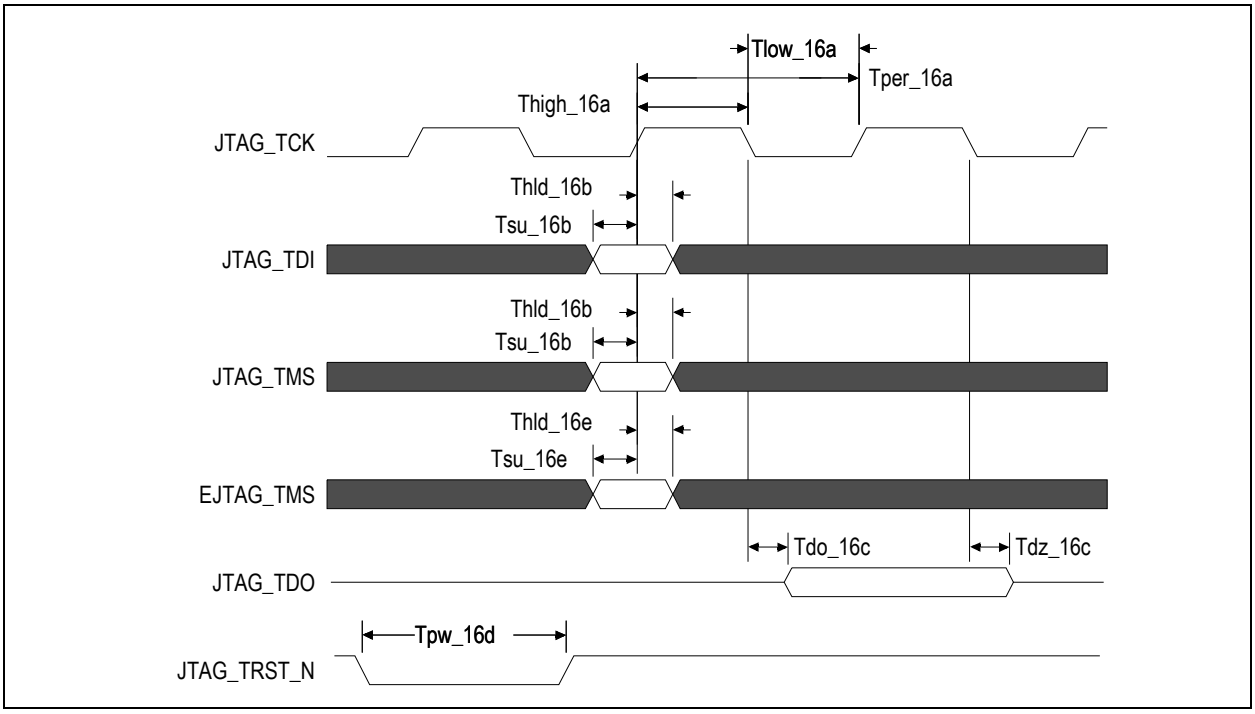



**Figure 22 JTAG AC Timing Waveform**

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32438 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 23 shows the electrical connection of the EJTAG probe target system connector.

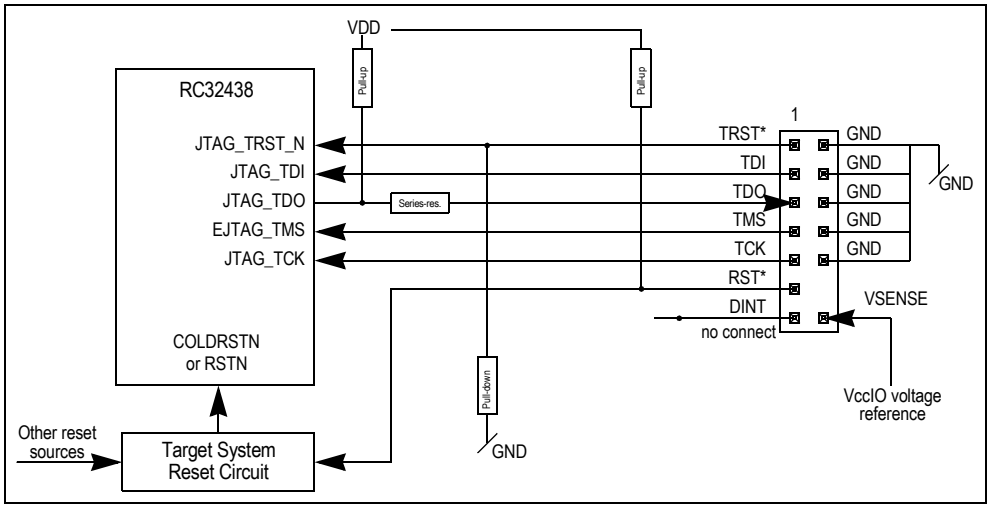



**Figure 23 Target System Electrical EJTAG Connection**

### Using the EJTAG Probe

In Figure 23, the pull-up resistors for JTAG_TDO and RST*, the pull-down resistor for JTAG_TRST_N, and the series resistor for JTAG_TDO must be adjusted to the specific design. However, the recommended pull-up/down resistor is 1.0 kΩ because a low value reduces crosstalk on the cable to the connector, allowing higher JTAG_TCK frequencies. A typical value for the series resistor is 33 Ω. Recommended resistor values have ± 5% tolerance.

If a probe is used, the pull-up resistor on JTAG_TDO must ensure that the JTAG_TDO level is high when no probe is connected and the JTAG_TDO output is tri-stated. This requirement allows reliable connection of the probe if it is hooked-up when the power is already on (hot plug). The pull-up resistor value of around 47 kΩ should be sufficient. Optional diodes to protect against overshoot and undershoot voltage can be added on the signals of the chip with EJTAG.

If a probe is used, the RST* signal must have a pull-up resistor because it is controlled by an open-collector (OC) driver in the probe, and thus is actively pulled low only. The pull-up resistor is responsible for the high value when not driven by the probe of 25pF. The input on the target system reset circuit must be able to accept the rise time when the pull-up resistor charges the capacitance to a high logical level. Vcc I/O must connect to a voltage reference that drops rapidly to below 0.5V when the target system loses power, even with a capacitive load of 25pF. The probe can thus detect the lost power condition.

For additional information on EJTAG, refer to Chapter 20 of the RC32438 User Reference Manual.

### Voltage Sense Signal Timing

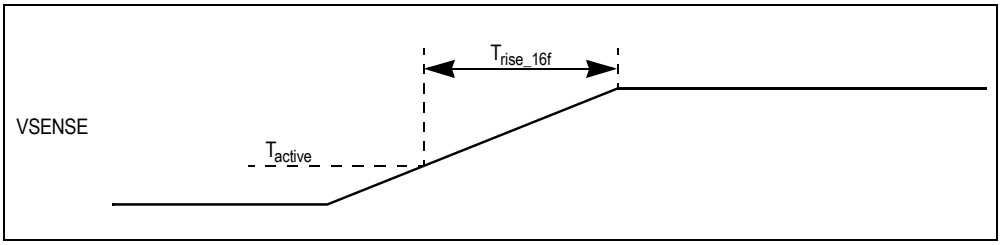



**Figure 24 Voltage Sense Signal Timing**

The target system must ensure that $T_{rise}$ is obeyed after the system reaches 0.5V ($T_{active}$), so the probe can use this value to determine when the target has powered-up. The probe is allowed to measure the $T_{rise}$ time from a higher value than $T_{active}$ (but lower than Vcc I/O minimum) because the stable indication in this case comes later than the time when target power is guaranteed to be stable. If JTAG_TRST_N is asserted by a pulse at power-up, this reset must be completed after $T_{rise}$. If JTAG_TRST_N is asserted by a pull-down resistor, the probe will control JTAG_TRST_N. At power-down, no power is indicated to the probe when Vcc I/O drops under the $T_{active}$ value, which the probe uses to stop driving the input signals, except for the probe RST*.

## Phase-Locked Loop (PLL)

The phase-locked loop (PLL) multiplies the external oscillator input (pin CLK) according to the parameter provided by the boot configuration vector to create the processor clock (PCLK). Inherently, PLL circuits are only capable of generating clock frequencies within a limited range.

### PLL Filters

It is recommended that the system designer provide a filter network of passive components for the PLL analog and digital power supplies.

The PLL circuit power and PLL circuit ground should be isolated from power and ground with a filter circuit such as the one shown in Figure 25.

Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

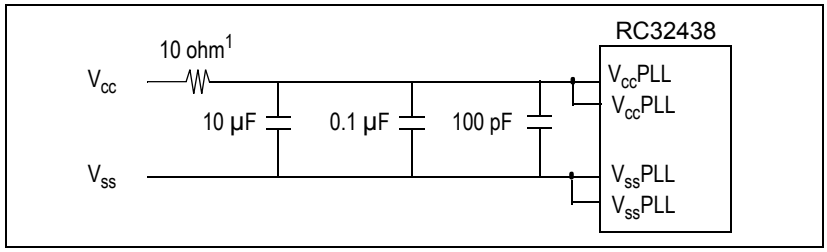



**Figure 25 PLL Filter Circuit for Noisy Environments**

# Recommended Operating Supply Voltages

| Symbol | Parameter | Clock Speed | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{ss}$ | Common ground | All speeds | 0 | 0 | 0 | V |
| $V_{ss}$PLL | PLL ground | | | | | |
| $V_{cc}$I/O | I/O supply except for SSTL_2[1] | | 3.0 | 3.3 | 3.6 | V |
| $V_{cc}$SI/O | I/O supply for SSTL_2[1] | | 2.3 | 2.5 | 2.7 | V |
| $V_{cc}$PLL | PLL supply | 200MHz, 233MHz | 1.1 | 1.2 | 1.3 | V |
| | | 266MHz, 300MHz | 1.2 | 1.3 | 1.4 | V |
| $V_{cc}$Core | Internal logic supply | 200MHz, 233MHz | 1.1 | 1.2 | 1.3 | V |
| | | 266MHz, 300MHz | 1.2 | 1.3 | 1.4 | V |
| DDRVREF[2] | SSTL_2 input reference voltage | All speeds | 0.5(VccSI/O) | 0.5(VccSI/O) | 0.5(VccSI/O) | V |
| $V_{TT}$[3] | SSTL_2 termination voltage | | DDRVREF - 0.04 | DDRVREF | DDRVREF + 0.04 | V |

**Table 15 RC32438 Operating Voltages**

1. SSTL_2 I/Os are used to connect to DDR SDRAM.

2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).

3. $V_{TT}$ of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

# Recommended Operating Temperatures

| Grade | Temperature |
|---|---|
| Commercial | 0°C to +70°C Ambient |
| Industrial | -40°C to +85°C Ambient |

**Table 16 RC32438 Operating Temperatures**

# Capacitive Load Deration

Refer to the 79RC32438 IBIS Model on the IDT web site (www.idt.com).

# Power Consumption

| Parameter | | 200MHz | | 233MHz | | 266MHz | | 300MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | | |
| $I_{cc}$ I/O | | 130 | 150 | 180 | 200 | 220 | 250 | 260 | 300 | mA | $C_L$ = 35 pF<br>$T_{ambient}$ = 25°C<br>Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. |
| $I_{cc}$ SI/O | | 100 | 120 | 150 | 170 | 200 | 220 | 250 | 270 | mA | |
| $I_{cc}$ Core, $I_{cc}$ PLL | Normal mode | 460 | 500 | 510 | 550 | 610 | 650 | 680 | 730 | mA | |
| Power Dissipation | Normal mode | 1.2 | 1.6 | 1.6 | 1.9 | 2.0 | 2.4 | 2.4 | 2.7 | W | |

**Table 17 RC32438 Power Consumption**

# DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

**Note:** See Table 2, Pin Characteristics, for a complete I/O listing.

| I/O Type | Parameter | Min. | Typical | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| LOW Drive Output | $I_{OL}$ | — | 14.0 | — | mA | $V_{OL}$ = 0.4V |
| | $I_{OH}$ | — | -12.0 | — | mA | $V_{OH}$ = 1.5V |
| HIGH Drive Output | $I_{OL}$ | — | 24.0 | — | mA | $V_{OL}$ = 0.4V |
| | $I_{OH}$ | — | -42.0 | — | mA | $V_{OH}$ = 1.5V |
| Schmitt Trigger Input (STI) | $V_{IL}$ | -0.3 | — | 0.8 | V | — |
| | $V_{IH}$ | 2.0 | — | $V_{cc}$I/O + 0.5 | V | — |
| SSTL_2 (for DDR SDRAM) | $I_{OL}$ | 7.6 | — | — | mA | $V_{OL}$ = 0.5V |
| | $I_{OH}$ | -7.6 | — | — | mA | $V_{OH}$ = 1.76V |
| | $V_{IL}$ | -0.3 | — | 0.5($V_{cc}$SI/O) - 0.18 | V | |
| | $V_{IH}$ | 0.5($V_{cc}$SI/O) + 0.18 | — | $V_{cc}$SI/O + 0.3 | V | |

**Table 18 DC Electrical Characteristics (Part 1 of 2)**

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|
| B9 | MDATA[11] | | G3 | MII0TXCLK | | V3 | GPIO[05] | 1 | AD25 | DDROEN[02] | |
| B10 | MDATA[03] | | G4 | $V_{ss}$ | | V4 | $V_{ss}$ | | AD26 | DDROEN[01] | |
| B11 | MDATA[08] | | G23 | $V_{ss}$ | | V23 | $V_{ss}$ | | AE1 | N/C | |
| B12 | MDATA[02] | | G24 | DDRCKP[00] | | V24 | DDRADDR[08] | | AE2 | GPIO[13] | 1 |
| B13 | GPIO[23] | 1 | G25 | DDRDATA[16] | | V25 | DDRRASN | | AE3 | GPIO[18] | 1 |
| B14 | MADDR[20] | | G26 | DDRDATA[13] | | V26 | DDRCASN | | AE4 | GPIO[24] | 1 |
| B15 | GPIO[20] | 1 | H1 | MII1CRS | | W1 | GPIO[04] | 1 | AE5 | GPIO[26] | 1 |
| B16 | MADDR[17] | | H2 | MII1CL | | W2 | SCK | | AE6 | PCIAD[31] | |
| B17 | MADDR[14] | | H3 | MII1RXCLK | | W3 | CLK | | AE7 | PCIAD[28] | |
| B18 | MADDR[12] | | H4 | $V_{ss}$ | | W4 | $V_{ss}$ | | AE8 | PCIAD[25] | |
| B19 | MADDR[09] | | H23 | $V_{ss}$ | | W23 | $V_{ss}$ | | AE9 | GPIO[30] | 1 |
| B20 | MADDR[06] | | H24 | DDRCKN[00] | | W24 | DDRADDR[07] | | AE10 | PCIAD[22] | |
| B21 | MADDR[03] | | H25 | DDRDATA[18] | | W25 | DDRADDR[06] | | AE11 | PCIAD[19] | |
| B22 | MADDR[00] | | H26 | DDRVREF | | W26 | DDRBA[01] | | AE12 | PCIAD[16] | |
| B23 | DDRDATA[01] | | J1 | MII1RXD[01] | | Y1 | GPIO[06] | 1 | AE13 | PCIRSTN | |
| B24 | DDRDQS[00] | | J2 | MII1RXD[00] | | Y2 | $V_{cc}$ PLL | | AE14 | PCIREQN[02] | |
| B25 | DDRDM[00] | | J3 | MII1RXD[03] | | Y3 | GPIO[08] | 1 | AE15 | PCIFRAMEN | |
| B26 | DDRDATA[06] | | J4 | $V_{ss}$ | | Y4 | $V_{ss}$ | | AE16 | PCIDEVSELN | |
| C1 | MII0RXD[00] | | J23 | $V_{ss}$ | | Y23 | $V_{ss}$ | | AE17 | PCILOCKN | |
| C2 | MII0RXCLK | | J24 | DDRDATA[17] | | Y24 | DDRCKN[01] | | AE18 | PCICBEN[01] | |
| C3 | EXTCLK | | J25 | DDRDATA[21] | | Y25 | DDRBA[00] | | AE19 | PCIAD[13] | |
| C4 | COLDRSTN | | J26 | DDRDATA[19] | | Y26 | DDRADDR[05] | | AE20 | PCIAD[10] | |
| C5 | OEN | | K1 | MII1RXDV | | AA1 | $V_{ss}$ PLL | | AE21 | PCICBEN[00] | |
| C6 | CSN[03] | | K2 | MII1RXD[02] | | AA2 | GPIO[07] | 1 | AE22 | PCIAD[05] | |
| C7 | CSN[00] | | K3 | MII1TXCLK | | AA3 | $V_{cc}$ PLL | | AE23 | PCIAD[02] | |
| C8 | BRN | | K4 | $V_{cc}$ Core | | AA4 | $V_{ss}$ | | AE24 | PCIGNTN[01] | |
| C9 | BDIRN | | K23 | $V_{ss}$ | | AA23 | $V_{ss}$ | | AE25 | DDRDM[07] | |
| C10 | MDATA[12] | | K24 | DDRDATA[20] | | AA24 | DDRCKP[01] | | AE26 | DDRDM[04] | |
| C11 | MDATA[09] | | K25 | DDRDQS[02] | | AA25 | DDRADDR[03] | | AF1 | GPIO[16] | 1 |
| C12 | MDATA[01] | | K26 | DDRCKE | | AA26 | DDRADDR[04] | | AF2 | GPIO[17] | 1 |
| C13 | MDATA[05] | | L1 | MII1TXD[00] | | AB1 | GPIO[09] | 1 | AF3 | GPIO[19] | 1 |
| C14 | MDATA[04] | | L2 | MII1RXER | | AB2 | GPIO[14] | 1 | AF4 | SCL | |
| C15 | MDATA[00] | | L3 | MII1TXD[03] | | AB3 | GPIO[11] | 1 | AF5 | GPIO[28] | 1 |
| C16 | GPIO[21] | 1 | L4 | $V_{cc}$ Core | | AB4 | $V_{ss}$ | | AF6 | PCIAD[29] | |
| C17 | MADDR[18] | | L23 | $V_{cc}$ Core | | AB23 | $V_{ss}$ | | AF7 | PCIAD[27] | |
| C18 | MADDR[15] | | L24 | DDRDM[02] | | AB24 | $V_{cc}$ SI/O | | AF8 | PCIAD[24] | |
| C19 | MADDR[11] | | L25 | DDRDATA[24] | | AB25 | DDRADDR[01] | | AF9 | PCIAD[23] | |

**Table 20 RC32438 416-pin Signal Pin-Out (Part 2 of 3)**

# RC32438 Alternate Signal Functions

| Pin | GPIO | Alternate | Pin | GPIO | Alternate | Pin | GPIO | Alternate |
|---|---|---|---|---|---|---|---|---|
| A14 | GPIO[22] | MADDR[24] | Y1 | GPIO[06] | U0RTSN | AE2 | GPIO[13] | U1CTSN |
| B13 | GPIO[23] | MADDR[25] | Y3 | GPIO[08] | U1SOUT | AE3 | GPIO[18] | DMAFINN[0] |
| B15 | GPIO[20] | MADDR[22] | AA2 | GPIO[07] | U0CTSN | AE4 | GPIO[24] | PCIREQN[4] |
| C16 | GPIO[21] | MADDR[23] | AB1 | GPIO[09] | U1SINP | AE5 | GPIO[26] | PCIGNTN[4] |
| N3 | GPIO[01] | U0SINP | AB2 | GPIO[14] | DMAREQN[0] | AE9 | GPIO[30] | PCIMUINTN |
| P1 | GPIO[00] | U0SOUT | AB3 | GPIO[11] | U1DSRN | AF1 | GPIO[16] | DMADONE[0] |
| P3 | GPIO[02] | U0RIN | AC2 | GPIO[10] | U1DTRN | AF2 | GPIO[17] | DMADONE[1] |
| T2 | GPIO[03] | U0DCDN | AC3 | GPIO[12] | U1RTSN | AF3 | GPIO[19] | DMAFINN[1] |
| V3 | GPIO[05] | U0DSRN | AD3 | GPIO[15] | DMAREQN[1] | AF5 | GPIO[28] | PCIGNTN[5] |
| W1 | GPIO[04] | U0DTRN | AD5 | GPIO[27] | PCIREQN[5] | | | |

**Table 23 RC32438 Alternate Signal Functions**

# RC32438 Signals Listed Alphabetically

The following table lists the RC32438 pins in alphabetical order.

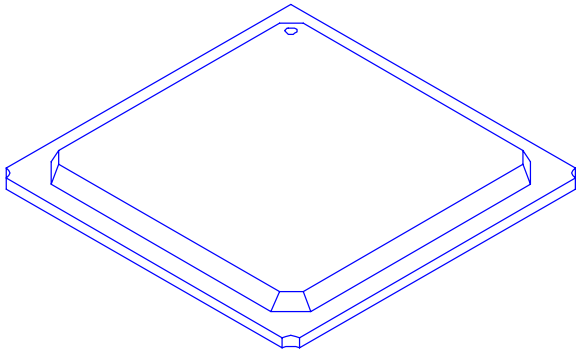
| Signal Name | I/O Type | Location | Signal Category |
|---|---|---|---|
| BDIRN | O | C9 | Memory and Peripheral Bus |
| BGN | O | B7 | Memory and Peripheral Bus |
| BOEN | O | A7 | Memory and Peripheral Bus |
| BRN | I | C8 | Memory and Peripheral Bus |
| BWEN[00] | O | B6 | Memory and Peripheral Bus |
| BWEN[01] | O | A6 | Memory and Peripheral Bus |
| CLK | I | W3 | System |
| COLDRSTN | I | C4 | System |
| CPU | O | T3 | Debug |
| CSN[00] | O | C7 | Memory and Peripheral Bus |
| CSN[01] | O | B5 | |
| CSN[02] | O | A5 | |
| CSN[03] | O | C6 | |
| CSN[04] | O | B4 | |
| CSN[05] | O | A4 | |

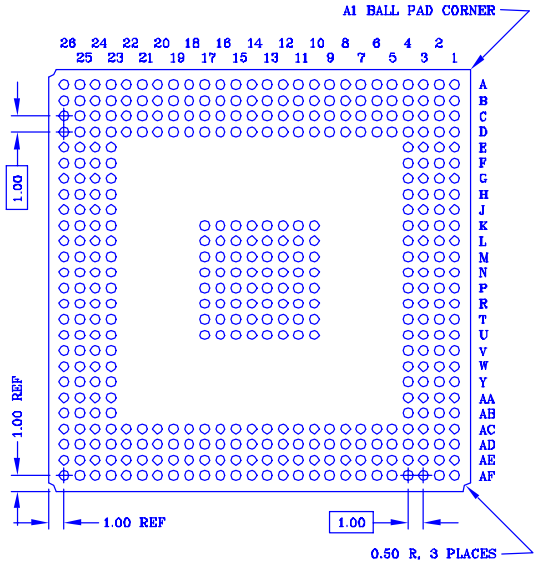
**Table 24 RC32438 Alphabetical Signal List (Part 1 of 9)**

| Signal Name | I/O Type | Location | Signal Category |
|---|---|---|---|
| GPIO[28] | I/O | AF5 | General Purpose Input/Output |
| GPIO[29] | I/O | A13 | |
| GPIO[30] | I/O | AE9 | |
| GPIO[31] | I/O | A3 | |
| INST | O | R1 | Debug |
| JTAG_TCK | I | U2 | EJTAG/ICE |
| JTAG_TDI | I | U1 | |
| JTAG_TDO | O | U3 | |
| JTAG_TMS | I | AD2 | |
| JTAG_TRST_N | I | AD1 | |
| MADDR[00] | O | B22 | Memory and Peripheral Bus |
| MADDR[01] | O | C22 | |
| MADDR[02] | O | A22 | |
| MADDR[03] | O | B21 | |
| MADDR[04] | O | C21 | |
| MADDR[05] | O | A21 | |
| MADDR[06] | O | B20 | |
| MADDR[07] | O | A20 | |
| MADDR[08] | O | C20 | |
| MADDR[09] | O | B19 | |
| MADDR[10] | O | A19 | |
| MADDR[11] | O | C19 | |
| MADDR[12] | O | B18 | |
| MADDR[13] | O | A18 | |
| MADDR[14] | O | B17 | |
| MADDR[15] | O | C18 | |
| MADDR[16] | O | A17 | |
| MADDR[17] | O | B16 | |
| MADDR[18] | O | C17 | |
| MADDR[19] | O | A16 | |
| MADDR[20] | O | B14 | |
| MADDR[21] | O | A15 | |
| MDATA[00] | I/O | C15 | |
| MDATA[01] | I/O | C12 | |

**Table 24 RC32438 Alphabetical Signal List (Part 5 of 9)**

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| | 00 | INITIAL RELEASE | 04/01/02 | |






BOTTOM VIEW
(416 SOLDER BALLS)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 26 X 26.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | Integrated Device Technology, Inc.<br>2975 Stender Way, Santa Clara, CA 95054<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 TWX: 910-338-2070 | | |
| APPROVALS | DATE | TITLE | BB PACKAGE OUTLINE<br>27.0 X 27.0 mm BODY<br>PBGA |
| DRAWN BK | 08/06/01 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4106 REV 00 |
| DO NOT SCALE DRAWING | | | SHEET 2 OF 2 |