Renesas Electronics America Inc - 79RC32K438-266BBI Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	416-BGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-266bbi

Signal	Type	Name/Description
GPIO[18]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAFINN0 Alternate function: External DMA channel 0 finished output.
GPIO[19]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAFINN1 Alternate function: External DMA channel 1 finished output.
GPIO[20]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address output.
GPIO[21]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address output.
GPIO[22]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address output.
GPIO[23]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address output.
GPIO[24]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4 input or output.
GPIO[25]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: AFSPARE1 Alternate function: *reserved.*
GPIO[26]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4 output.
GPIO[27]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5 input or output.
GPIO[28]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5 output.
GPIO[29]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: Reserved Alternate function: Reserved.

Table 1 Pin Description (Part 6 of 9)

Signal	Type	Name/Description
MII1CRS	I	**Ethernet 1 MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII1RXCLK	I	**Ethernet 1 MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MII1RXD[3:0]	I	**Ethernet 1 MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MII1RXDV	I	**Ethernet 1 MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII1RXER	I	**Ethernet 1 MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII1TXCLK	I	**Ethernet 1 MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII1TXD[3:0]	O	**Ethernet 1 MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MII1TXENP	O	**Ethernet 1 MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MII1TXER	O	**Ethernet 1 MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
JTAG / EJTAG		
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 8 of 9)

Signal	Type	Name/Description
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
Debug		
CPU	O	**CPU Transaction.** This signal is asserted during all CPU instruction fetches and data transfers to/from the DDR and devices on the memory and peripheral bus. The signal is negated during PCI and DMA transactions to/from the DDR and devices on the memory and peripheral bus.
INST	O	**Instruction or Data.** This signal is driven high during CPU instruction fetches on the memory and peripheral bus memory or DDR bus.

Table 1 Pin Description (Part 9 of 9)

Pin Characteristics

Note: Some input pads of the RC32438 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32438's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BGN	O	LVTTL	Low Drive		
	BOEN	O	LVTTL	High Drive		
	BRN	I	LVTTL	STI[2]	pull-up	
	BWEN[1:0]	O	LVTTL	High Drive		
	CSN[5:0]	O	LVTTL	High Drive		
	MADDR[21:0]	O	LVTTL	High Drive		
	MDATA[15:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	

Table 2 Pin Characteristics (Part 1 of 4)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Miscellaneous	CLK	I	LVTTL	STI		
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 4 of 4)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.
2. Schmidt Trigger Input (STI).
3. The PCI pins have internal pull-ups but they are too weak to guarantee system validity. Therefore, board pull-ups are mandatory where indicated. GPIO alternate function pins for PCI must also have board pull-ups.
4. PCIMUINTN is an alternate function of GPIO[30]. When configured as an alternate function, this pin is tri-stated when not asserted (i.e., it acts as an open collector output).
5. Use a 2.2K pull-up resistor for I2C pins.

Boot Configuration Vector

The boot configuration vector is read by the RC32438 during a cold reset. The vector defines essential RC32438 parameters that are required once the cold reset completes.

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32438 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MDATA[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.1 in the RC32438 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 6 0x4 - Multiply by 8 0x5 - reserved 0x6 - reserved 0x7 - reserved 0x8 - reserved 0xD - reserved 0xE - reserved 0xF - reserved
MDATA[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MDATA[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian

Table 3 Boot Configuration Encoding (Part 1 of 2)

Signal	Name/Description
MDATA[7]	**Boot Device Width**. This field specifies the width of the boot device (i.e., Device 0). 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width
MDATA[8]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4096 clock cycles 0x1 - reserved
MDATA[11:9]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*
MDATA[12]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MDATA[15:13]	**Reserved**. These pins must be driven low during boot configuration.

Table 3 Boot Configuration Encoding (Part 2 of 2)

Logic Diagram — RC32438

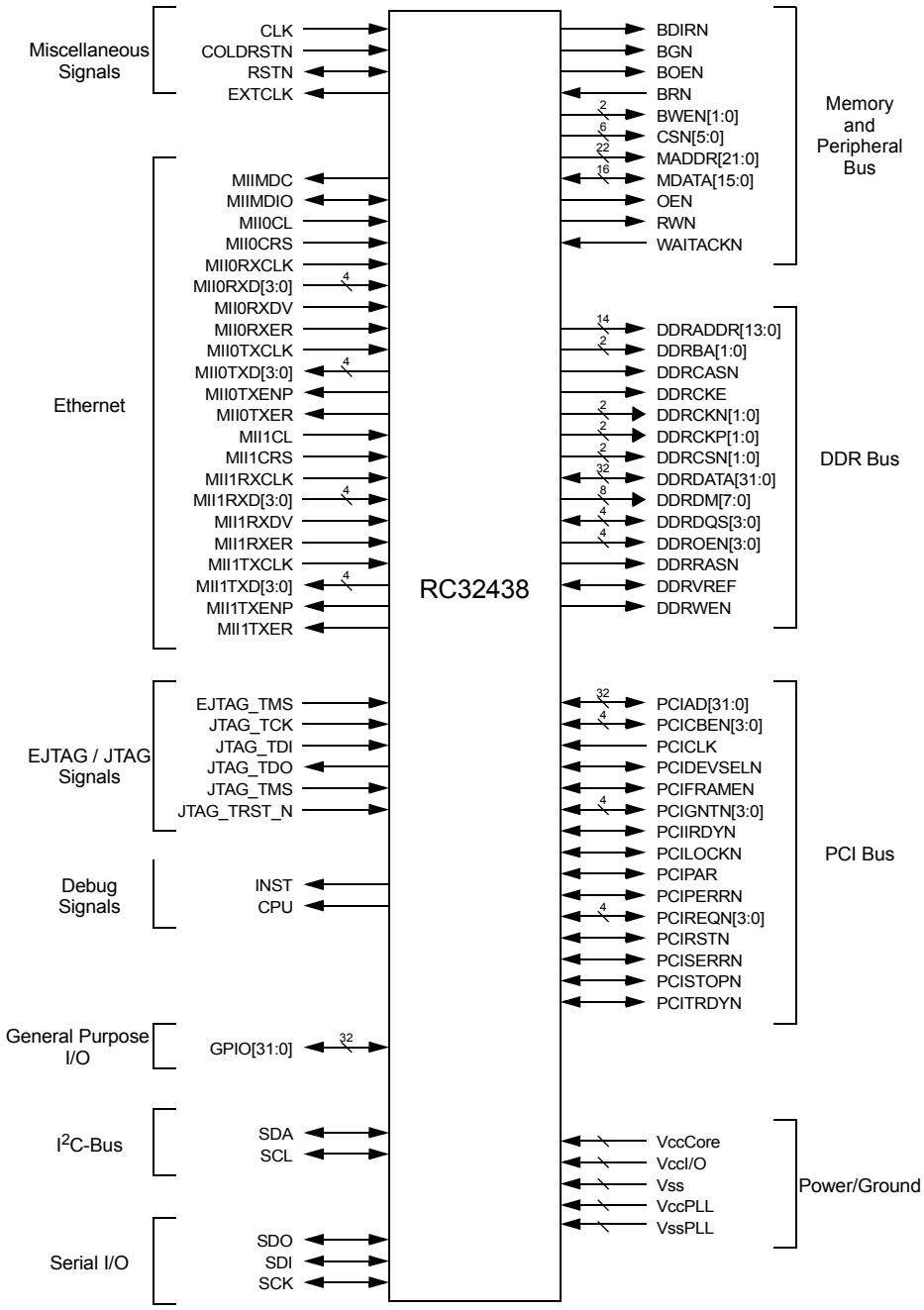
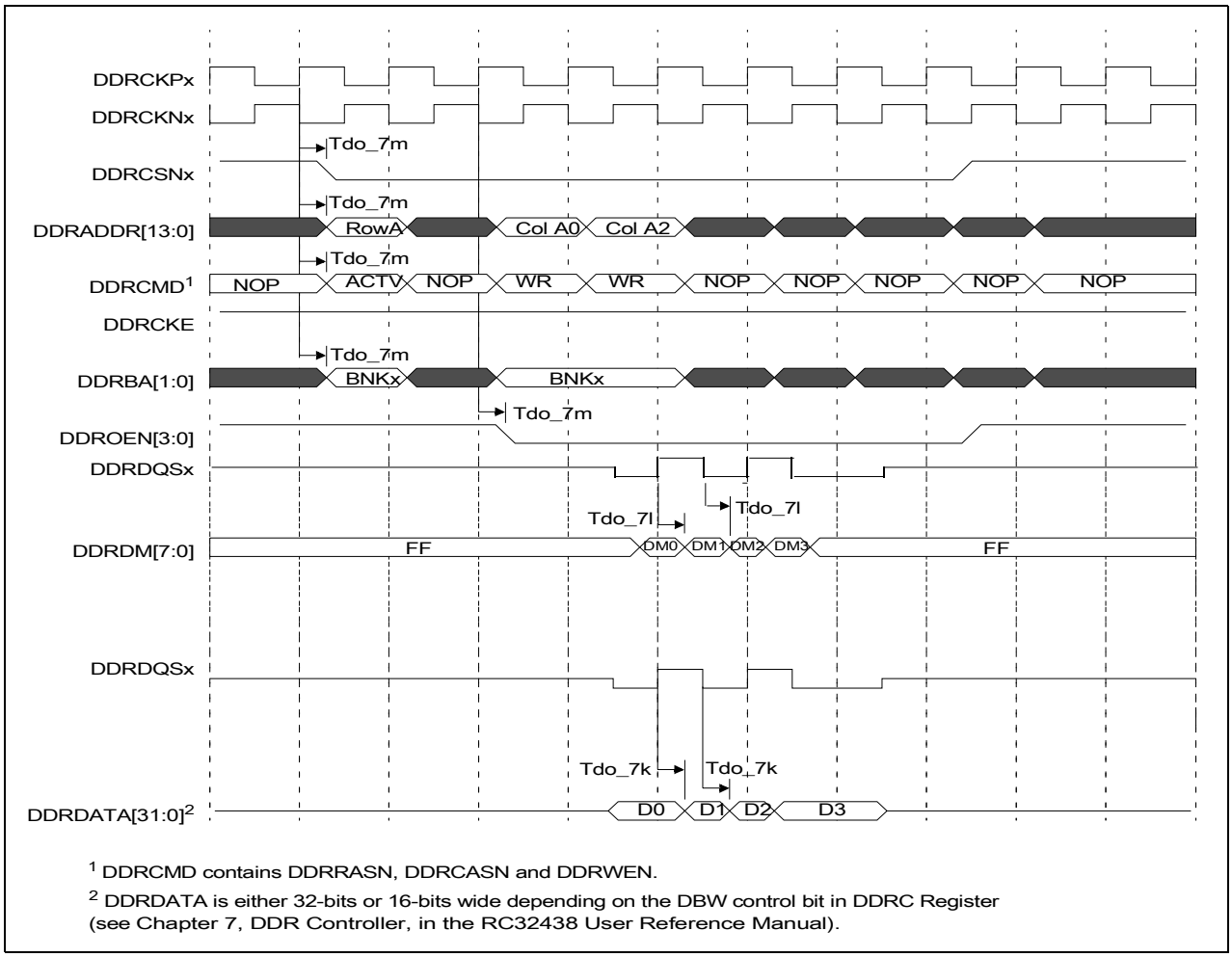


Figure 1 Logic Diagram



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32438 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns		
	Tdz_8a[2]		0.0	0.1	0.0	0.1	0.0	0.1	0.0	0.1	ns		
	Tzd_8a[2]		0.5	2.3	0.5	2.3	0.5	2.3	0.5	2.3	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.0	6.5	0.0	6.5	0.0	6.5	0.0	6.5	ns		
	Tdz_8b[2]		0.7	1.5	0.7	1.5	0.7	1.5	0.7	1.5	ns		
	Tzd_8b[2]		1.2	3.3	1.2	3.3	1.2	3.3	1.2	3.3	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 3)

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[15:0]	Tsu_8c	EXTCLK rising	7.0	—	7.0	—	7.0	—	7.0	—	ns		See Figures 8 and 9 (cont.)
	Thld_8c		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_8c		0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8c[2]		0.0	0.1	0.0	0.1	0.0	0.1	0.0	0.1	ns		
	Tzd_8c[2]		0.5	2.2	0.5	2.2	0.5	2.2	0.5	2.2	ns		
EXTCLK[3]	Tper_8d	none	10.0	—	8.33	—	7.5	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
	Tdz_8e[2]		-1.0	-0.1	-1.0	-0.1	-1.0	-0.1	-1.0	-0.1	ns		
	Tzd_8e[2]		0.4	1.0	0.4	1.0	0.4	1.0	0.4	1.0	ns		
BOEN	Tdo_8f	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
	Tdz_8f[2]		0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	ns		
	Tzd_8f[2]		1.1	2.0	1.1	2.0	1.1	2.0	1.1	2.0	ns		
BRN	Tsu_8g	EXTCLK rising	5.5	—	5.5	—	5.5	—	5.5	—	ns		
	Thld_8g		0.0	—	0.0	—	0.0	—	0.0	—	ns		
BGN	Tdo_8h	EXTCLK rising	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	5.8	—	5.8	—	5.8	—	5.8	—	ns		
	Thld_8h		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tpw_8h[2]	none	2(EXT-CLK)	—	2(EXT-CLK)	—	2(EXT-CLK)	—	2(EXT-CLK)	—	ns		
CSN[5:0]	Tdo_8i	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8i[2]		0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	ns		
	Tzd_8i[2]		0.6	2.2	0.6	2.2	0.6	2.2	0.6	2.2	ns		
RWN	Tdo_8j	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8j[2]		-0.7	0.1	-0.7	0.1	-0.7	0.1	-0.7	0.1	ns		
	Tzd_8j[2]		0.6	1.1	0.6	1.1	0.6	1.1	0.6	1.1	ns		
OEN	Tdo_8k	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8k[2]		-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	ns		
	Tzd_8k[2]		0.8	1.5	0.8	1.5	0.8	1.5	0.8	1.5	ns		
BWEN[1:0]	Tdo_8l	EXTCLK rising	0.0	4.0	0.0	4.0	0.0	4.0	0.0	4.0	ns		
	Tdz_8l[2]		0	0.2	0	0.2	0	0.2	0	0.2	ns		
	Tzd_8l[2]		0.8	1.7	0.8	1.7	0.8	1.7	0.8	1.7	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 3)

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
DMAREQN[1:0]	Tpw_8n[2]	None	2(ICLK)	—	2(ICLK)		2(ICLK)	—	2(ICLK)	—	ns		See Figures 10 and 11.
DMADONEN[1:0]	Tsu_8o	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		
	Thld_8o		1.0	—	1.0	—	1.0	—	1.0	—	ns		
DMAFINN[1:0]	Tdo_8p	EXTCLK rising	1.5	6.0	1.5	6.0	1.5	6.0	1.5	6.0	ns		
CPU, INST	Tdo_8m	EXTCLK rising	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns		See Figures 8 and 9.

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 3 of 3)

1. The RC32438 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32438 are both driving. See Chapter 6, Device Controller, in the RC32438 User Reference Manual.
2. The values for this symbol were determined by calculation, not by testing.
3. The frequency of EXTCLK is programmable. See the External Clock Divider description in Table 3 of this data sheet.
4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

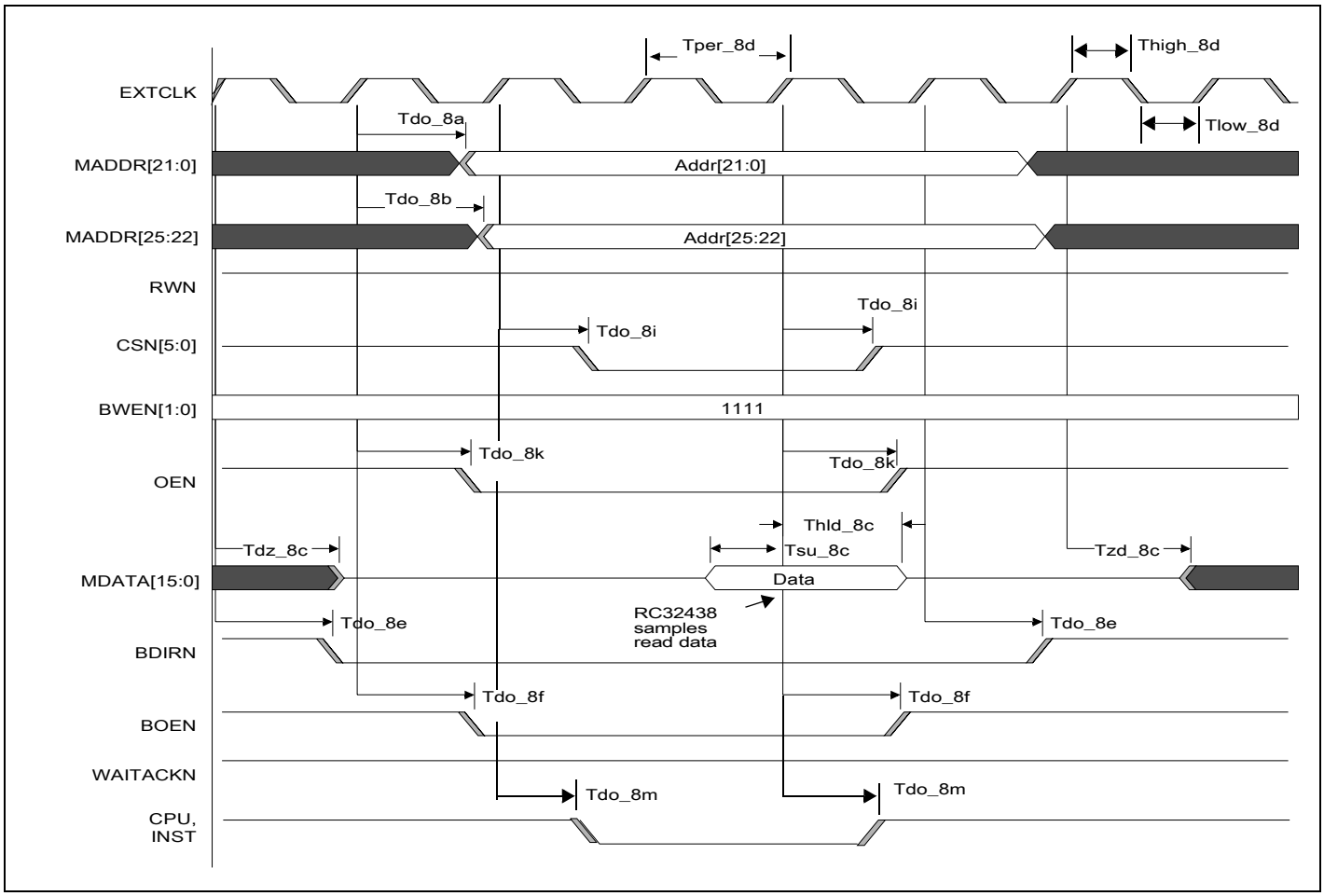


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

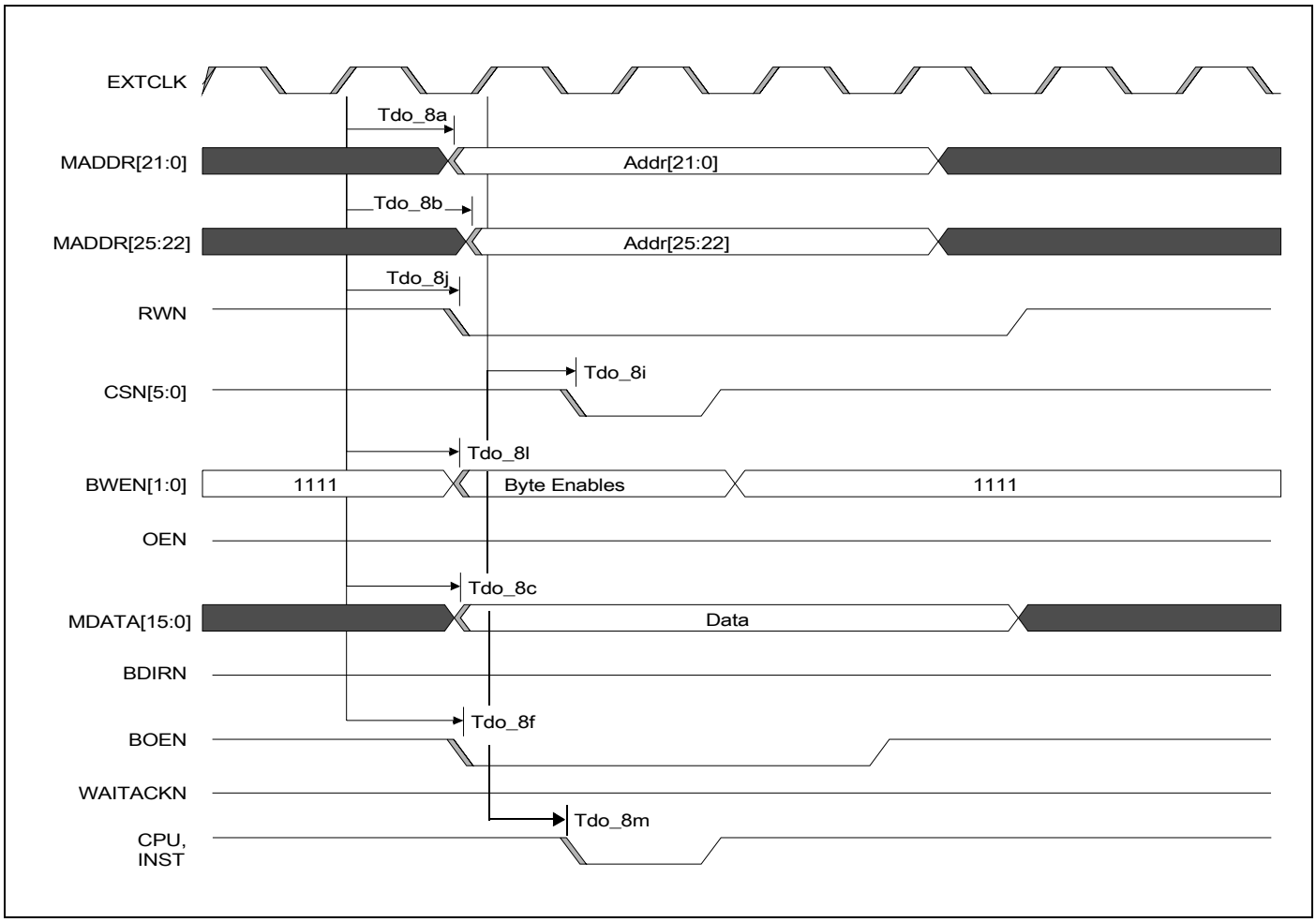


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

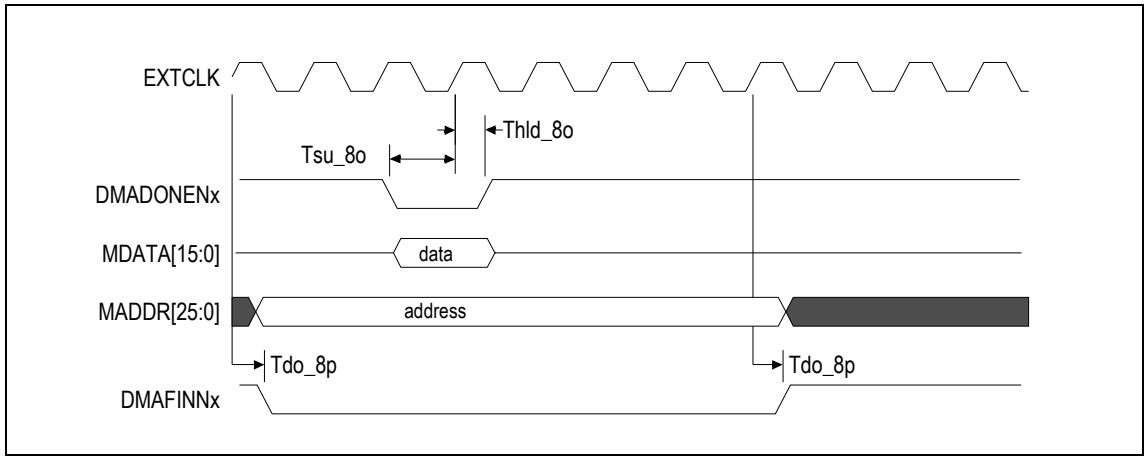


Figure 10 DMADONEN and DMAFINN AC Timing Waveform

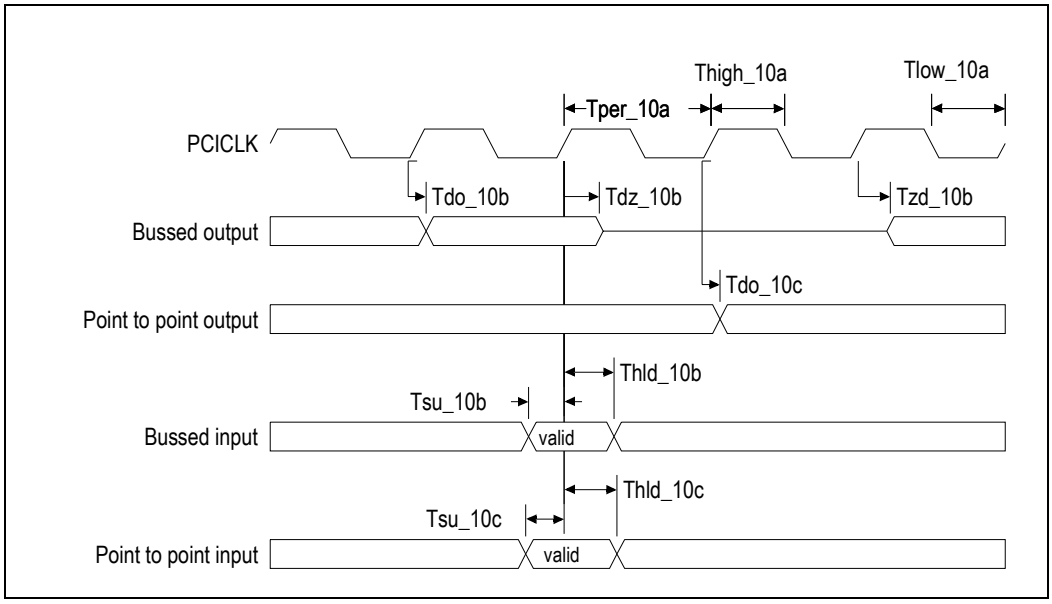


Figure 13 PCI AC Timing Waveform

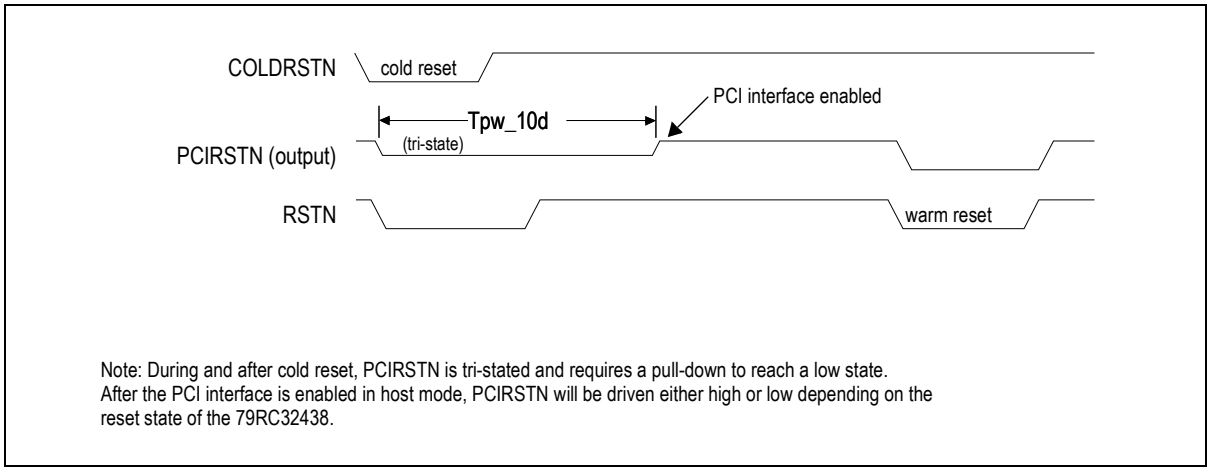


Figure 14 PCI AC Timing Waveform — PCI Reset in Host Mode

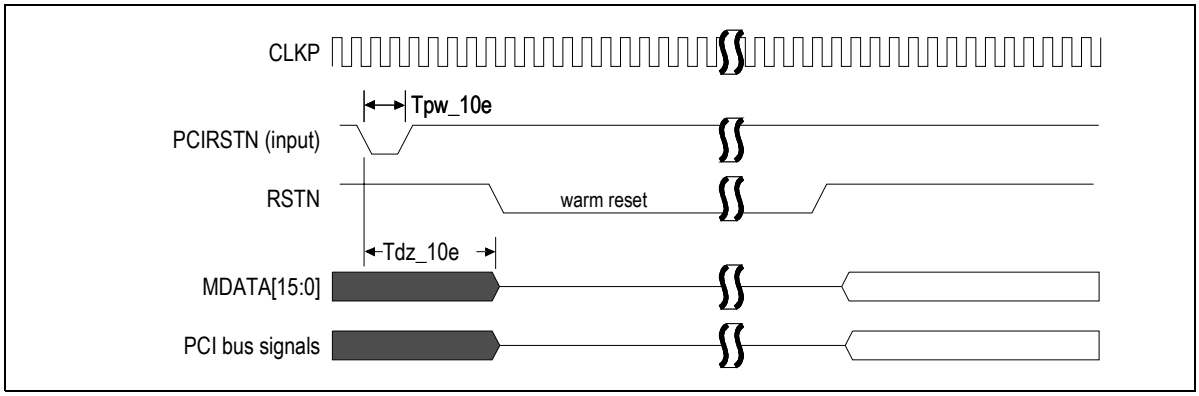


Figure 15 PCI AC Timing Waveform — PCI Reset in Satellite Mode

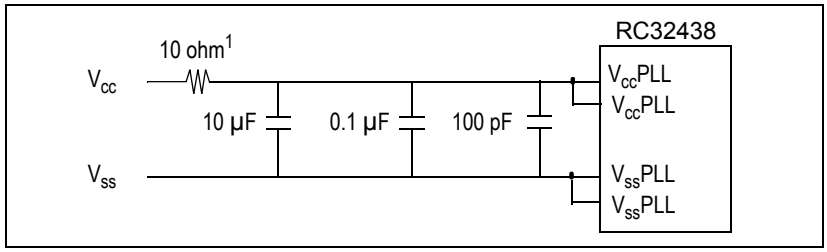


Figure 25 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Clock Speed	Minimum	Typical	Maximum	Unit
V_{ss}	Common ground	All speeds	0	0	0	V
V_{ss}PLL	PLL ground					
V_{cc}I/O	I/O supply except for SSTL_2[1]		3.0	3.3	3.6	V
V_{cc}SI/O	I/O supply for SSTL_2[1]		2.3	2.5	2.7	V
V_{cc}PLL	PLL supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
V_{cc}Core	Internal logic supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
DDRVREF[2]	SSTL_2 input reference voltage	All speeds	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage		DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32438 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.

2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).

3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32438 Operating Temperatures

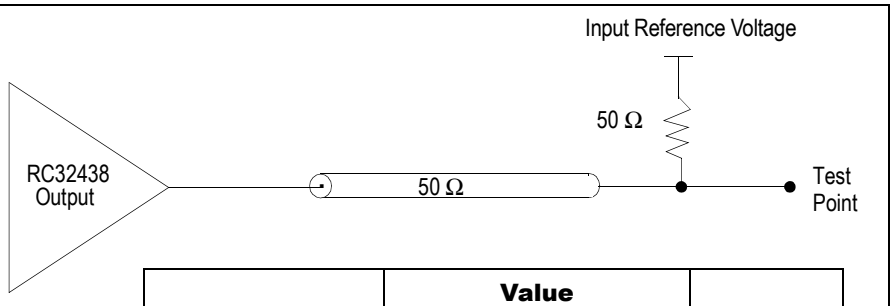
Capacitive Load Deration

Refer to the 79RC32438 IBIS Model on the IDT web site (www.idt.com).

I/O Type	Parameter	Min.	Typical	Max.	Unit	Conditions
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—		mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—		mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	8.0	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs	—	—	± 10	µA	Vcc (max)
	I/O_{LEAK} with Pull-ups/downs	—	—	± 80	µA	Vcc (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

AC Test Conditions



Parameter	Value		Units
	SSTL I/O	Other I/O	
Input pulse levels	0 to 2.5	0 to 3.3	V
Input rise/fall	0.8	1.0	ns
Input reference level	0.5(VccSI/O)	0.5(VccI/O)	V
Output reference levels	1.25	1.5	V
AC test load	35	35	pF

Figure 26 AC Test Conditions

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B9	MDATA[11]		G3	MII0TXCLK		V3	GPIO[05]	1	AD25	DDROEN[02]	
B10	MDATA[03]		G4	V_{ss}		V4	V_{ss}		AD26	DDROEN[01]	
B11	MDATA[08]		G23	V_{ss}		V23	V_{ss}		AE1	N/C	
B12	MDATA[02]		G24	DDRCKP[00]		V24	DDRADDR[08]		AE2	GPIO[13]	1
B13	GPIO[23]	1	G25	DDRDATA[16]		V25	DDRRASN		AE3	GPIO[18]	1
B14	MADDR[20]		G26	DDRDATA[13]		V26	DDRCASN		AE4	GPIO[24]	1
B15	GPIO[20]	1	H1	MII1CRS		W1	GPIO[04]	1	AE5	GPIO[26]	1
B16	MADDR[17]		H2	MII1CL		W2	SCK		AE6	PCIAD[31]	
B17	MADDR[14]		H3	MII1RXCLK		W3	CLK		AE7	PCIAD[28]	
B18	MADDR[12]		H4	V_{ss}		W4	V_{ss}		AE8	PCIAD[25]	
B19	MADDR[09]		H23	V_{ss}		W23	V_{ss}		AE9	GPIO[30]	1
B20	MADDR[06]		H24	DDRCKN[00]		W24	DDRADDR[07]		AE10	PCIAD[22]	
B21	MADDR[03]		H25	DDRDATA[18]		W25	DDRADDR[06]		AE11	PCIAD[19]	
B22	MADDR[00]		H26	DDRVREF		W26	DDRBA[01]		AE12	PCIAD[16]	
B23	DDRDATA[01]		J1	MII1RXD[01]		Y1	GPIO[06]	1	AE13	PCIRSTN	
B24	DDRDQS[00]		J2	MII1RXD[00]		Y2	V_{cc} PLL		AE14	PCIREQN[02]	
B25	DDRDM[00]		J3	MII1RXD[03]		Y3	GPIO[08]	1	AE15	PCIFRAMEN	
B26	DDRDATA[06]		J4	V_{ss}		Y4	V_{ss}		AE16	PCIDEVSELN	
C1	MII0RXD[00]		J23	V_{ss}		Y23	V_{ss}		AE17	PCILOCKN	
C2	MII0RXCLK		J24	DDRDATA[17]		Y24	DDRCKN[01]		AE18	PCICBEN[01]	
C3	EXTCLK		J25	DDRDATA[21]		Y25	DDRBA[00]		AE19	PCIAD[13]	
C4	COLDRSTN		J26	DDRDATA[19]		Y26	DDRADDR[05]		AE20	PCIAD[10]	
C5	OEN		K1	MII1RXDV		AA1	V_{ss} PLL		AE21	PCICBEN[00]	
C6	CSN[03]		K2	MII1RXD[02]		AA2	GPIO[07]	1	AE22	PCIAD[05]	
C7	CSN[00]		K3	MII1TXCLK		AA3	V_{cc} PLL		AE23	PCIAD[02]	
C8	BRN		K4	V_{cc} Core		AA4	V_{ss}		AE24	PCIGNTN[01]	
C9	BDIRN		K23	V_{ss}		AA23	V_{ss}		AE25	DDRDM[07]	
C10	MDATA[12]		K24	DDRDATA[20]		AA24	DDRCKP[01]		AE26	DDRDM[04]	
C11	MDATA[09]		K25	DDRDQS[02]		AA25	DDRADDR[03]		AF1	GPIO[16]	1
C12	MDATA[01]		K26	DDRCKE		AA26	DDRADDR[04]		AF2	GPIO[17]	1
C13	MDATA[05]		L1	MII1TXD[00]		AB1	GPIO[09]	1	AF3	GPIO[19]	1
C14	MDATA[04]		L2	MII1RXER		AB2	GPIO[14]	1	AF4	SCL	
C15	MDATA[00]		L3	MII1TXD[03]		AB3	GPIO[11]	1	AF5	GPIO[28]	1
C16	GPIO[21]	1	L4	V_{cc} Core		AB4	V_{ss}		AF6	PCIAD[29]	
C17	MADDR[18]		L23	V_{cc} Core		AB23	V_{ss}		AF7	PCIAD[27]	
C18	MADDR[15]		L24	DDRDM[02]		AB24	V_{cc} SI/O		AF8	PCIAD[24]	
C19	MADDR[11]		L25	DDRDATA[24]		AB25	DDRADDR[01]		AF9	PCIAD[23]	

Table 20 RC32438 416-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C20	MADDR[08]		L26	DDRDATA[22]		AB26	DDRADDR[02]		AF10	PCIAD[20]	
C21	MADDR[04]		M1	MII1TXD[02]		AC1	V_{ss} PLL		AF11	PCIAD[17]	
C22	MADDR[01]		M2	MII1TXD[01]		AC2	GPIO[10]	1	AF12	PCIREQN[03]	
C23	DDRDATA[00]		M3	MIIMDC		AC3	GPIO[12]	1	AF13	PCIREQN[00]	
C24	DDRDATA[03]		M4	V_{cc} Core		AC4	V_{ss}		AF14	PCICBEN[02]	
C25	DDRDATA[08]		M23	V_{cc} Core		AC5	V_{ss}		AF15	PCITRDYN	
C26	DDRDATA[07]		M24	DDRDATA[23]		AC6	V_{ss}		AF16	PCISERRN	
D1	MII0RXD[03]		M25	DDRDATA[27]		AC7	V_{cc} I/O		AF17	PCIPAR	
D2	MII0RXD[01]		M26	DDRDATA[25]		AC8	V_{cc} I/O		AF18	PCIAD[14]	
D3	MII0RXD[02]		N1	MII1TXER		AC9	V_{cc} I/O		AF19	PCIAD[12]	
D4	V_{ss}		N2	MII1TXENP		AC10	V_{ss}		AF20	PCIAD[09]	
D5	V_{ss}		N3	GPIO[01]	1	AC11	V_{ss}		AF21	PCIAD[07]	
D6	V_{ss}		N4	V_{cc} Core		AC12	V_{ss}		AF22	PCIAD[03]	
D7	V_{cc} I/O		N23	V_{cc} Core		AC13	V_{cc} Core		AF23	PCIAD[01]	
D8	V_{cc} I/O		N24	DDRDATA[26]		AC14	V_{cc} Core		AF24	PCIGNTN[02]	
D9	V_{cc} I/O		N25	DDRDATA[28]		AC15	V_{cc} Core		AF25	DDRDM[06]	
D10	V_{ss}		N26	DDRDQS[03]		AC16	V_{ss}		AF26	DDROEN[03]	

Table 20 RC32438 416-pin Signal Pin-Out (Part 3 of 3)

RC32438 Power Pins

V_{cc} I/O	V_{cc} SI/O	V_{cc} Core	V_{cc} PLL
D7	D21	D13	Y2, AA3
D8	D22	D14	
D9	D23	D15	
D20	D24	K4	
P4	E23	L4	
R4	F23	L23	
T4	R23	M4	
U4	T23	M23	
AC7	AB24	N4	
AC8	AC23	N23	
AC9	AC24	P23	
AC20		AC13	
AC21		AC14	
AC22		AC15	

Table 21 RC32438 Power Pins

RC32438 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate	Pin	GPIO	Alternate
A14	GPIO[22]	MADDR[24]	Y1	GPIO[06]	U0RTSN	AE2	GPIO[13]	U1CTSN
B13	GPIO[23]	MADDR[25]	Y3	GPIO[08]	U1SOUT	AE3	GPIO[18]	DMAFINN[0]
B15	GPIO[20]	MADDR[22]	AA2	GPIO[07]	U0CTSN	AE4	GPIO[24]	PCIREQN[4]
C16	GPIO[21]	MADDR[23]	AB1	GPIO[09]	U1SINP	AE5	GPIO[26]	PCIGNTN[4]
N3	GPIO[01]	U0SINP	AB2	GPIO[14]	DMAREQN[0]	AE9	GPIO[30]	PCIMUINTN
P1	GPIO[00]	U0SOUT	AB3	GPIO[11]	U1DSRN	AF1	GPIO[16]	DMADONE[0]
P3	GPIO[02]	U0RIN	AC2	GPIO[10]	U1DTRN	AF2	GPIO[17]	DMADONE[1]
T2	GPIO[03]	U0DCDN	AC3	GPIO[12]	U1RTSN	AF3	GPIO[19]	DMAFINN[1]
V3	GPIO[05]	U0DSRN	AD3	GPIO[15]	DMAREQN[1]	AF5	GPIO[28]	PCIGNTN[5]
W1	GPIO[04]	U0DTRN	AD5	GPIO[27]	PCIREQN[5]			

Table 23 RC32438 Alternate Signal Functions

RC32438 Signals Listed Alphabetically

The following table lists the RC32438 pins in alphabetical order.

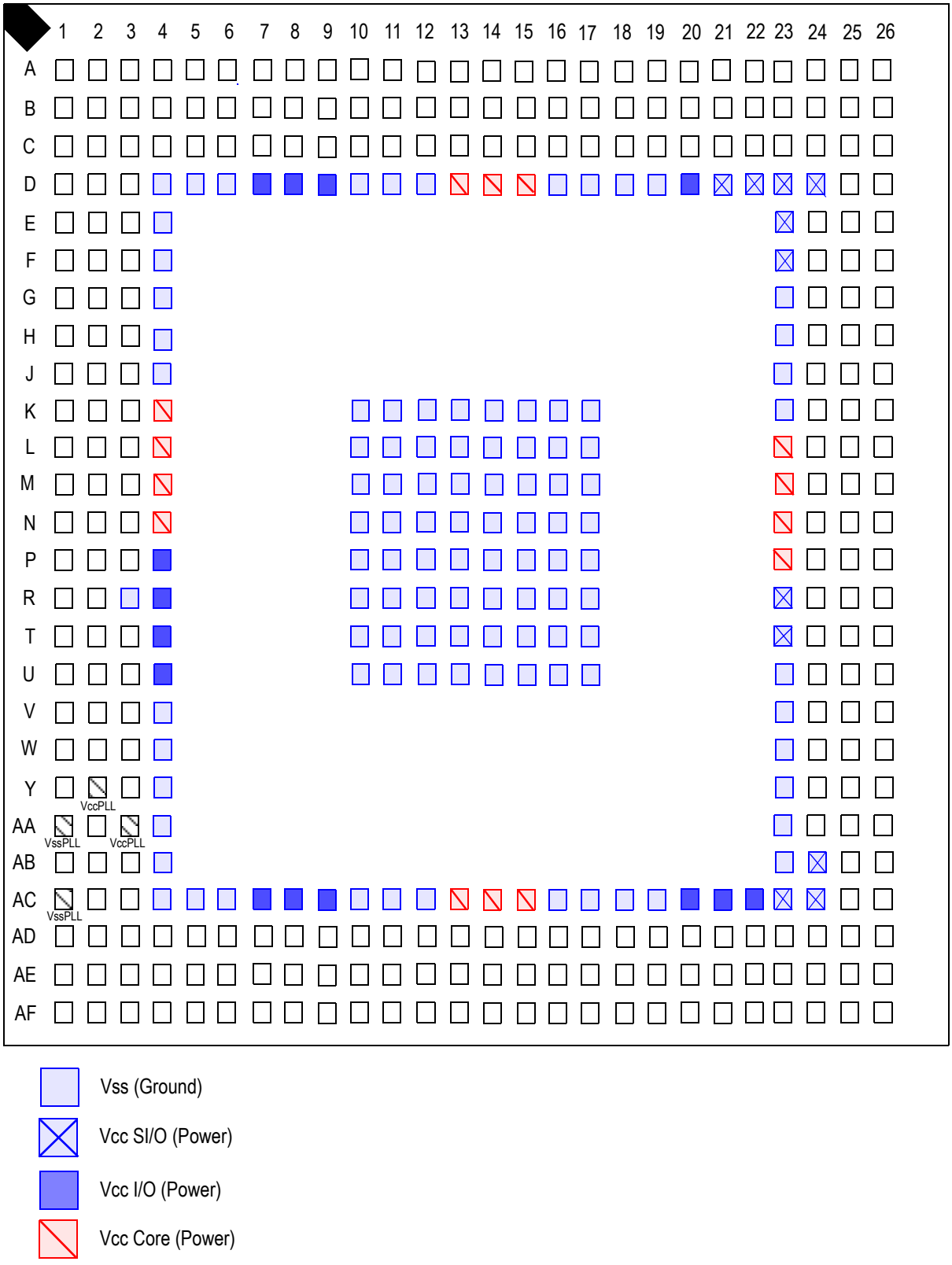
Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C9	Memory and Peripheral Bus
BGN	O	B7	Memory and Peripheral Bus
BOEN	O	A7	Memory and Peripheral Bus
BRN	I	C8	Memory and Peripheral Bus
BWEN[00]	O	B6	Memory and Peripheral Bus
BWEN[01]	O	A6	Memory and Peripheral Bus
CLK	I	W3	System
COLDRSTN	I	C4	System
CPU	O	T3	Debug
CSN[00]	O	C7	Memory and Peripheral Bus
CSN[01]	O	B5	
CSN[02]	O	A5	
CSN[03]	O	C6	
CSN[04]	O	B4	
CSN[05]	O	A4	

Table 24 RC32438 Alphabetical Signal List (Part 1 of 9)

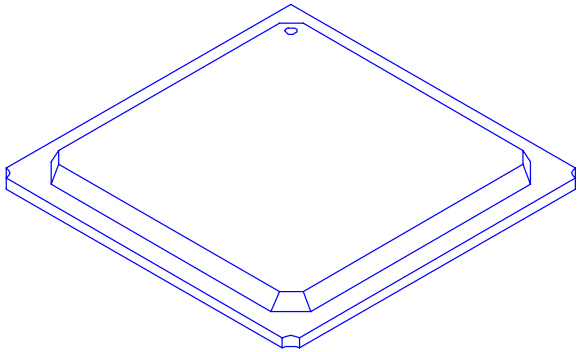
Signal Name	I/O Type	Location	Signal Category
PCIAD[21]	I/O	AD9	PCI Bus
PCIAD[22]	I/O	AE10	
PCIAD[23]	I/O	AF9	
PCIAD[24]	I/O	AF8	
PCIAD[25]	I/O	AE8	
PCIAD[26]	I/O	AD7	
PCIAD[27]	I/O	AF7	
PCIAD[28]	I/O	AE7	
PCIAD[29]	I/O	AF6	
PCIAD[30]	I/O	AD6	
PCIAD[31]	I/O	AE6	
PCICBEN[00]	I/O	AE21	
PCICBEN[01]	I/O	AE18	
PCICBEN[02]	I/O	AF14	
PCICBEN[03]	I/O	AD8	
PCICLK	I	AD12	
PCIDEVSELN	I/O	AE16	
PCIFRAMEN	I/O	AE15	
PCIGNTN[00]	I/O	AD13	
PCIGNTN[01]	I/O	AE24	
PCIGNTN[02]	I/O	AF24	
PCIGNTN[03]	I/O	AD21	
PCIIRDYN	I/O	AD14	
PCILOCKN	I/O	AE17	
PCIPAR	I/O	AF17	
PCIPERRN	I/O	AD16	
PCIREQN[00]	I/O	AF13	
PCIREQN[01]	I/O	AD11	
PCIREQN[02]	I/O	AE14	
PCIREQN[03]	I/O	AF12	
PCIRSTN	I/O	AE13	
PCISERRN	I/O	AF16	
PCISTOPN	I/O	AD15	
PCITRDYN	I/O	AF15	
RSTN	I/O	A23	System
RWN	O	B3	Memory and Peripheral Bus

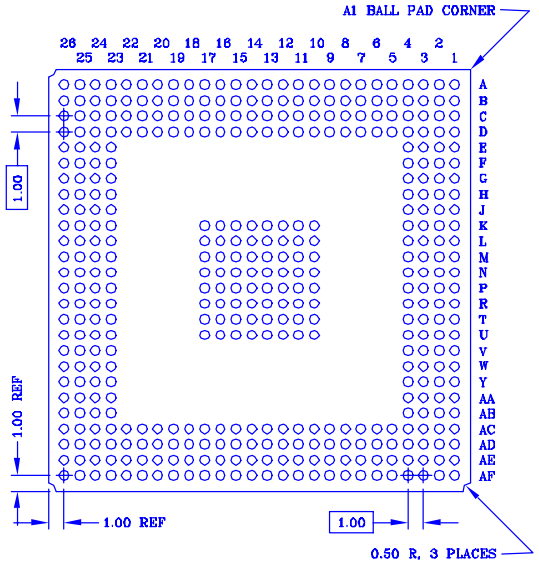
Table 24 RC32438 Alphabetical Signal List (Part 8 of 9)

RC32438 Pinout — Top View



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	04/01/02	





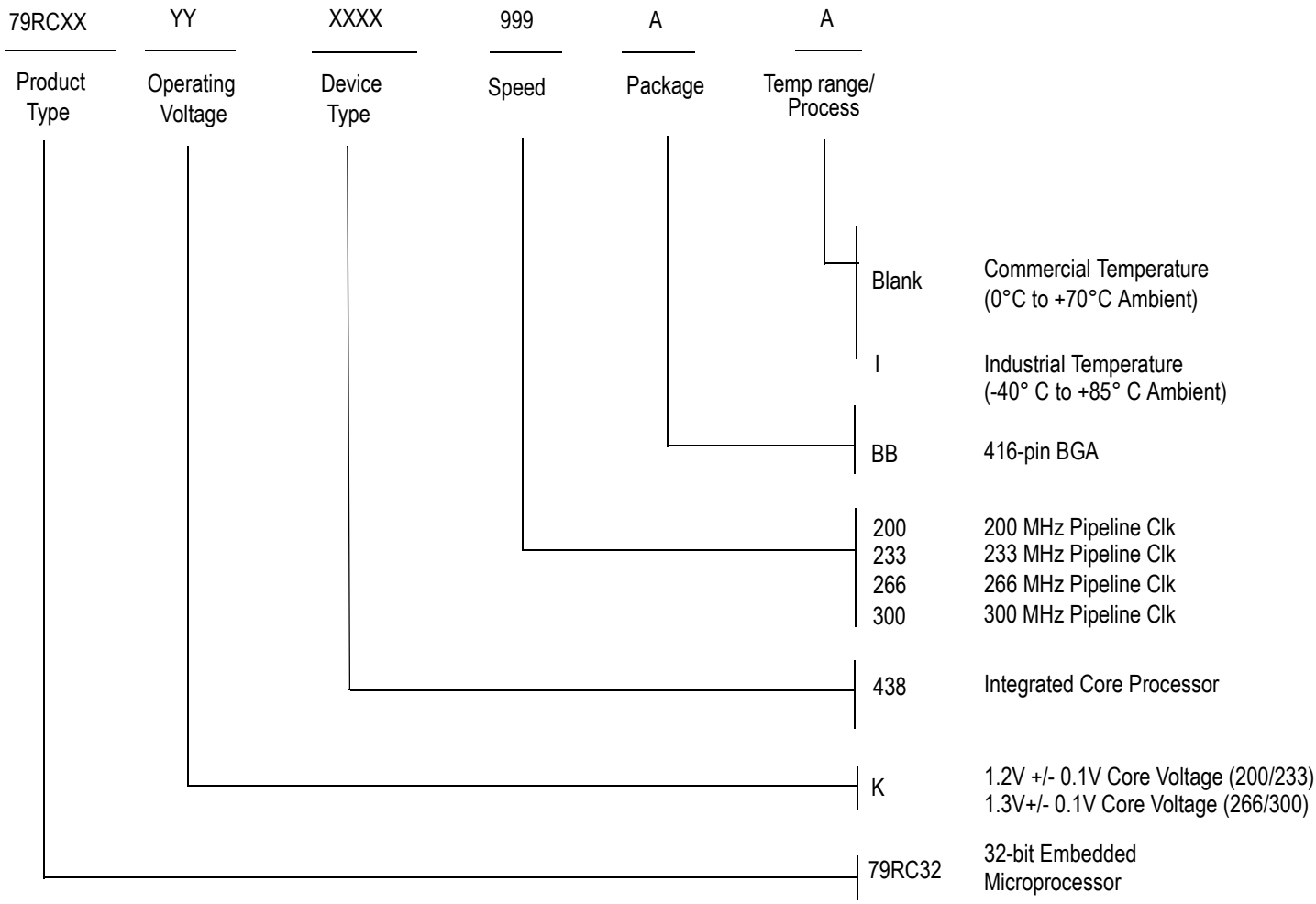
BOTTOM VIEW
(416 SOLDER BALLS)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 26 X 26.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
APPROVALS	DATE	TITLE	BB PACKAGE OUTLINE 27.0 X 27.0 mm BODY PBGA
DRAWN BK	08/06/01		
CHECKED		SIZE C	DRAWING No. PSC-4106 REV 00
DO NOT SCALE DRAWING			SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32K438 -200BB, 233BB, 266BB, 300BB	416-pin BGA package, Commercial Temperature
79RC32K438 -200BBI, 233BBI	416-pin BGA package, Industrial Temperature

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