Renesas Electronics America Inc - 79RC32K438-300BB Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	416-BGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-300bb

- **DMA Controller**
  - *10 DMA channels: two channels for PCI (PCI to Memory and Memory to PCI), two for each Ethernet interface, two channels for memory to memory operations, two channels for external operations*
  - *Provides flexible descriptor based operation*
  - *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length.*
- **Two Ethernet Interfaces**
  - *10 and 100 Mb/s ISO/IEC 8802-3:1996 compliant*
  - *Two IEEE 802.3u compatible Media Independent Interfaces (MII) with serial management interface*
  - *MII supports IEEE 802.3u auto-negotiation speed selection*
  - *Supports 64 entry hash table based multicast address filtering*
  - *512 byte transmit and receive FIFOs*
  - *Supports flow control functions outlined in IEEE Std. 802.3x-1997*
- **Universal Asynchronous Receiver Transmitter (UART)**
  - *Compatible with the 16550 and 16450 UARTs*
  - *Two completely separate serial channels*
  - *Modem control functions (CTS, RTS, DSR, DTR, RI, DCD)*
  - *16-byte transmit and receive buffers*
  - *Programmable baud rate generator derived from the system clock*
  - *Fully programmable serial characteristics:*
    - *5, 6, 7, or 8 bit characters*
    - *Even, odd or no parity bit generation and detection*
    - *1, 1-1/2 or 2 stop bit generation*
  - *Line break generation and detection*
  - *False start bit detection*
  - *Internal loopback mode*
- **I^2C-Bus**
  - *Supports standard 100 Kbps mode as well as 400 Kbps fast mode*
  - *Supports 7-bit and 10-bit addressing*
  - *Supports four modes: master transmitter, master receiver, slave transmitter, slave receiver*
- **Additional General Purpose Peripherals**
  - *Two 16550-compatible serial ports*
  - *Interrupt controller*
  - *System integrity functions*
  - *General purpose I/O controller*
  - *Serial peripheral interface (SPI)*
- **On-chip Memory**
  - *4KB of high speed SRAM organized as 1K x 32 bits*
  - *Supports burst and non-burst byte, halfword, triple-byte, and word CPU, PCI, and DMA accesses*
- **Debug Support**
  - *Rev. 2.6 compliant EJTAG Interface*

Device Overview

The RC32438 is a member of the IDT™ Interprise™ family of PCI integrated communications processors. It incorporates a high performance CPU core and a number of on-chip peripherals. The integrated processor is designed to transfer information from I/O modules to main memory with minimal CPU intervention using a highly sophisticated direct memory access (DMA) engine. All data transfers through the RC32438 are achieved by writing data from an on-chip I/O peripheral to main memory and then out to another I/O module.

CPU Execution Core

The 32-bit CPU core is 100% compatible with the MIPS32 instruction set architecture (ISA).

Specifically, this device features the 4Kc CPU core developed by MIPS Technologies Inc. (www.mips.com). This core issues a single instruction per cycle, includes a five stage pipeline, and is optimized for applications that require integer arithmetic. The CPU core includes 16 KB instruction and 16 KB data caches. Both caches are 4-way set associative and can be locked on a per line basis, which allows the programmer control over this precious on-chip memory resource. The core also features a memory management unit (MMU). The CPU core also incorporates an enhanced joint test access group (EJTAG) interface that is used to interface to in-circuit emulator tools, providing access to internal registers and enabling the part to be controlled externally, simplifying the system debug process. The use of this core allows IDT's customers to leverage the broad range of software and development tools available for the MIPS architecture, including operating systems, compilers, and in-circuit emulators.

Double Data Rate Memory Controller

The RC32438 incorporates a high performance double data rate (DDR) memory controller which supports both x16 and x32 memory configurations up to 2GB. This module provides all of the signals required to interface to both memory modules and discrete devices, including two chip selects, differential clocking outputs and data strobes.

Memory and I/O Controller

The RC32438 uses a dedicated local memory/IO controller including a de-multiplexed 16-bit data and 26-bit address bus. It includes all of the signals required to interface directly to as many as six Intel or Motorola-style external peripherals, and the interface can be configured to support both 8-bit and 16-bit peripherals.

DMA Controller

The DMA controller consists of 10 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

PCI Interface

The PCI interface on the RC32438 is compatible with version 2.2 of the PCI specification. An on-chip arbiter supports up to six external bus masters, supporting both fixed priority and rotating priority arbitration schemes. The part can support both satellite and host PCI configurations, enabling the RC32438 to act as a slave controller for a PCI add-in

Signal	Type	Name/Description
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
Debug		
CPU	O	**CPU Transaction.** This signal is asserted during all CPU instruction fetches and data transfers to/from the DDR and devices on the memory and peripheral bus. The signal is negated during PCI and DMA transactions to/from the DDR and devices on the memory and peripheral bus.
INST	O	**Instruction or Data.** This signal is driven high during CPU instruction fetches on the memory and peripheral bus memory or DDR bus.

Table 1 Pin Description (Part 9 of 9)

Pin Characteristics

Note: Some input pads of the RC32438 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32438's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BGN	O	LVTTL	Low Drive		
	BOEN	O	LVTTL	High Drive		
	BRN	I	LVTTL	STI[2]	pull-up	
	BWEN[1:0]	O	LVTTL	High Drive		
	CSN[5:0]	O	LVTTL	High Drive		
	MADDR[21:0]	O	LVTTL	High Drive		
	MDATA[15:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	

Table 2 Pin Characteristics (Part 1 of 4)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Serial Interface	SCK	I/O	LVTTL	Low Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	Low Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	Low Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[5]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[5]
Ethernet Interfaces	MII0CL	I	LVTTL	STI	pull-down	
	MII0CRS	I	LVTTL	STI	pull-down	
	MII0RXCLK	I	LVTTL	STI	pull-up	
	MII0RXD[3:0]	I	LVTTL	STI	pull-up	
	MII0RXDV	I	LVTTL	STI	pull-down	
	MII0RXER	I	LVTTL	STI	pull-down	
	MII0TXCLK	I	LVTTL	STI	pull-up	
	MII0TXD[3:0]	O	LVTTL	Low Drive		
	MII0TXENP	O	LVTTL	Low Drive		
	MII0TXER	O	LVTTL	Low Drive		
	MII1CL	I	LVTTL	STI	pull-down	
	MII1CRS	I	LVTTL	STI	pull-down	
	MII1RXCLK	I	LVTTL	STI	pull-up	
	MII1RXD[3:0]	I	LVTTL	STI	pull-up	
	MII1RXDV	I	LVTTL	STI	pull-down	
	MII1RXER	I	LVTTL	STI	pull-down	
	MII1TXCLK	I	LVTTL	STI	pull-up	
	MII1TXD[3:0]	O	LVTTL	Low Drive		
	MII1TXENP	O	LVTTL	Low Drive		
	MII1TXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / ICE	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
Debug	CPU	O	LVTTL	Low Drive		
	INST	O	LVTTL	Low Drive		

Table 2 Pin Characteristics (Part 3 of 4)

Logic Diagram — RC32438

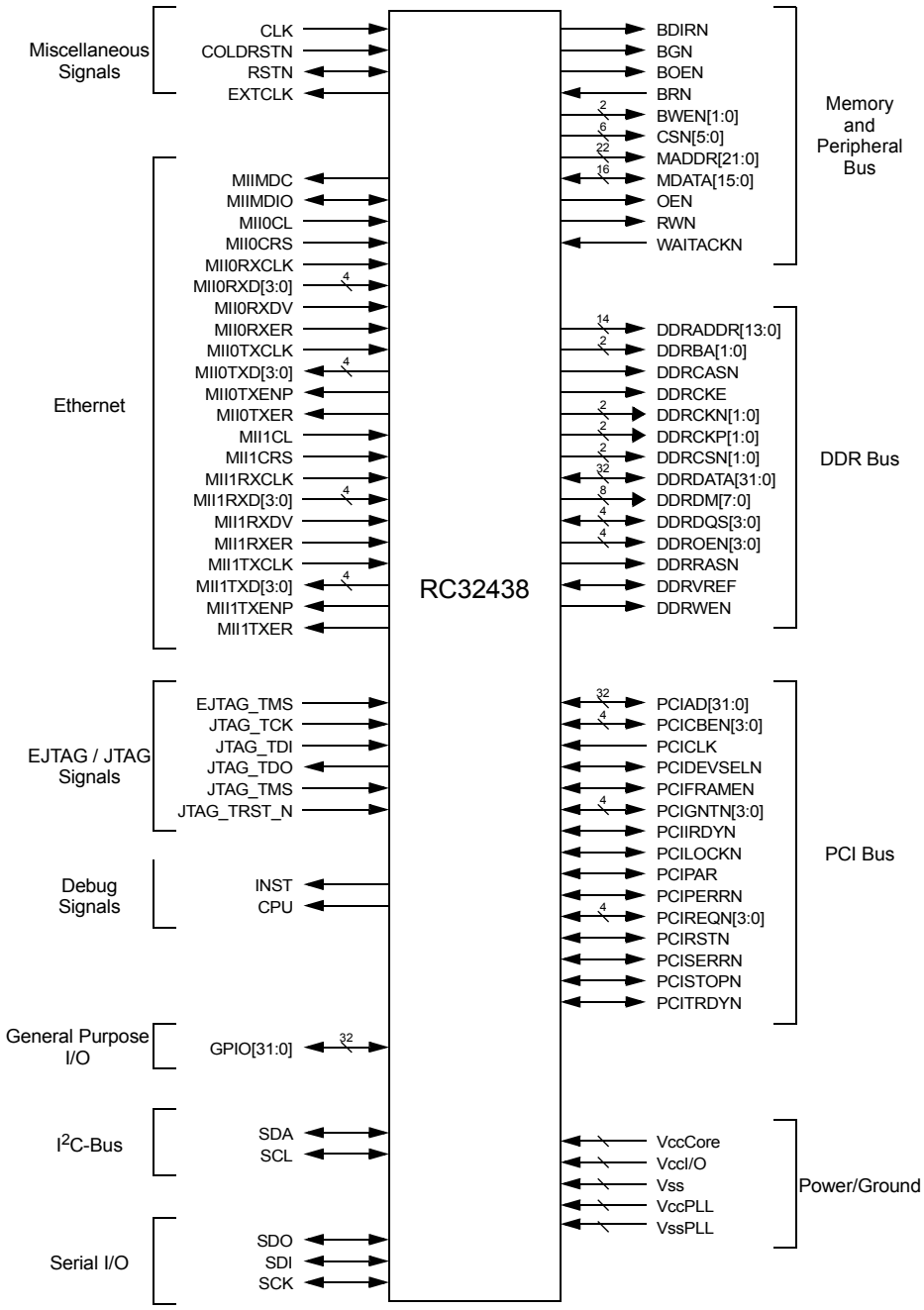


Figure 1 Logic Diagram

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

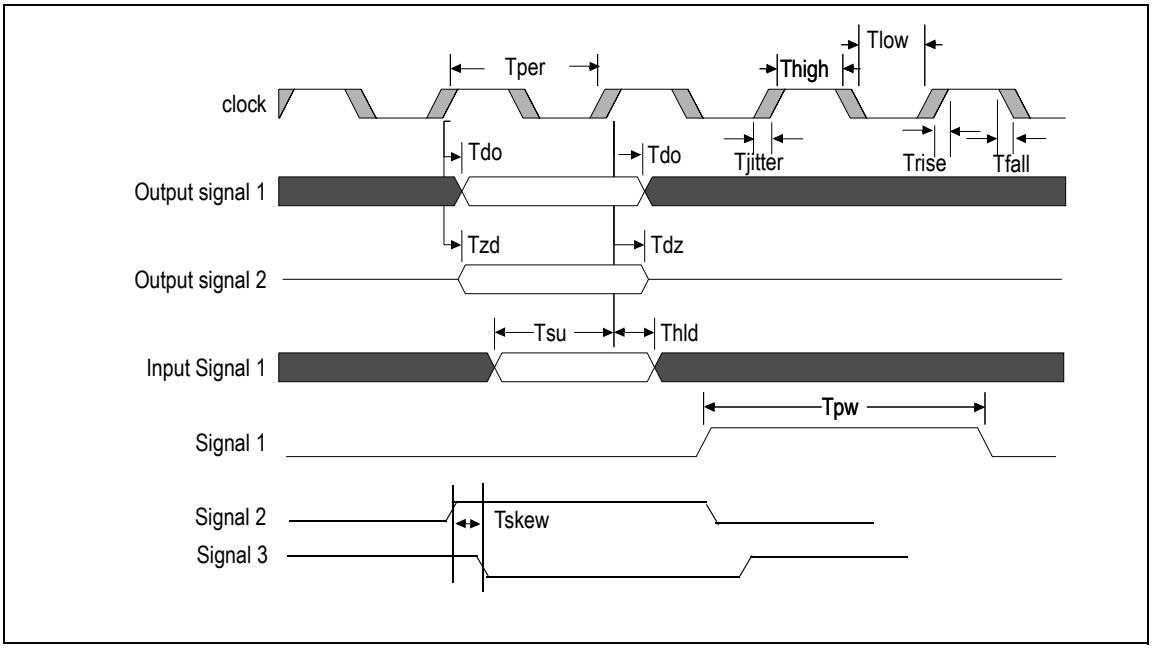
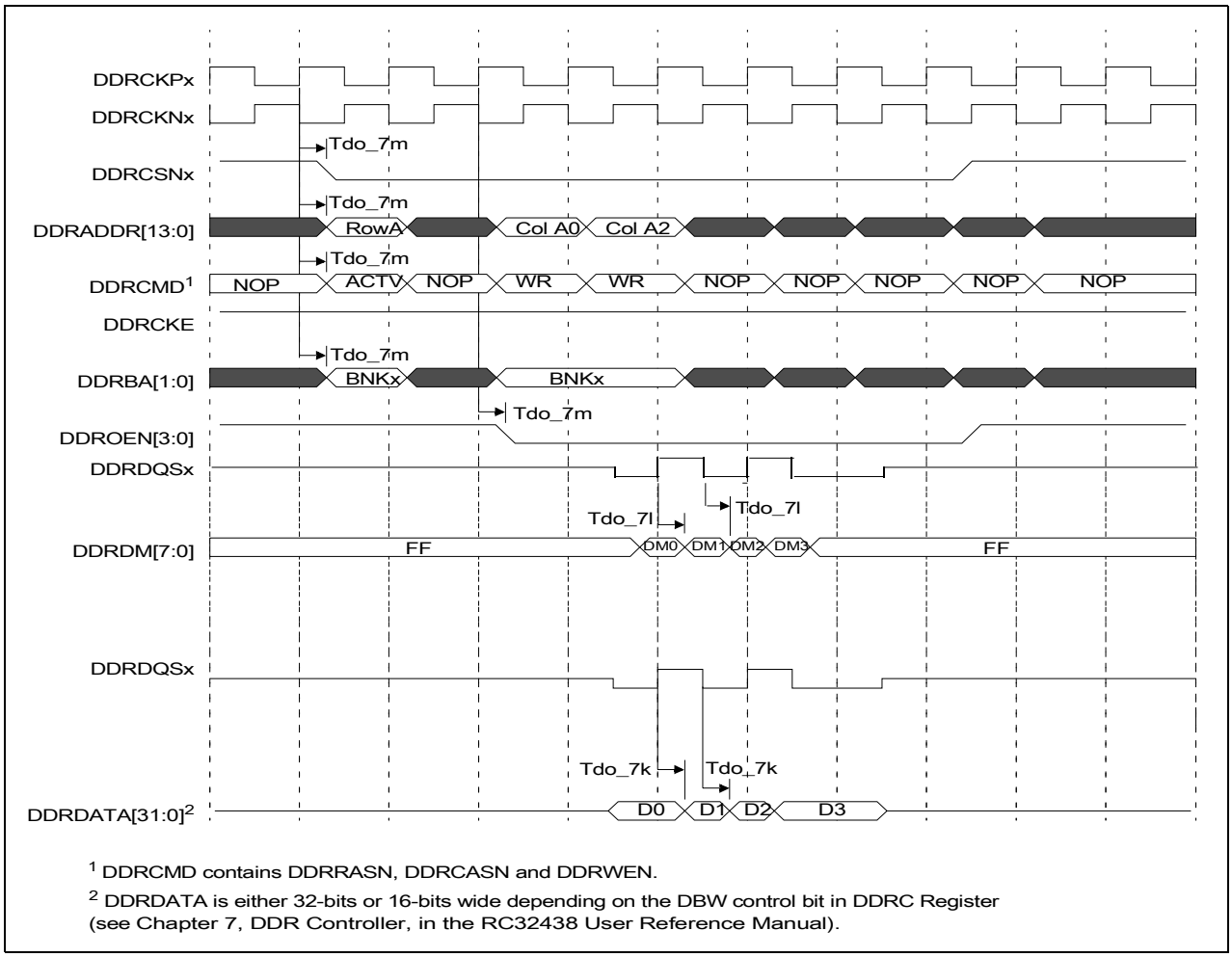


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

Table 4 AC Timing Definitions



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32438 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns		
	Tdz_8a[2]		0.0	0.1	0.0	0.1	0.0	0.1	0.0	0.1	ns		
	Tzd_8a[2]		0.5	2.3	0.5	2.3	0.5	2.3	0.5	2.3	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.0	6.5	0.0	6.5	0.0	6.5	0.0	6.5	ns		
	Tdz_8b[2]		0.7	1.5	0.7	1.5	0.7	1.5	0.7	1.5	ns		
	Tzd_8b[2]		1.2	3.3	1.2	3.3	1.2	3.3	1.2	3.3	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 3)

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
DMAREQN[1:0]	Tpw_8n[2]	None	2(ICLK)	—	2(ICLK)		2(ICLK)	—	2(ICLK)	—	ns		See Figures 10 and 11.
DMADONEN[1:0]	Tsu_8o	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		
	Thld_8o		1.0	—	1.0	—	1.0	—	1.0	—	ns		
DMAFINN[1:0]	Tdo_8p	EXTCLK rising	1.5	6.0	1.5	6.0	1.5	6.0	1.5	6.0	ns		
CPU, INST	Tdo_8m	EXTCLK rising	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns		See Figures 8 and 9.

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 3 of 3)

1. The RC32438 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32438 are both driving. See Chapter 6, Device Controller, in the RC32438 User Reference Manual.
2. The values for this symbol were determined by calculation, not by testing.
3. The frequency of EXTCLK is programmable. See the External Clock Divider description in Table 3 of this data sheet.
4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

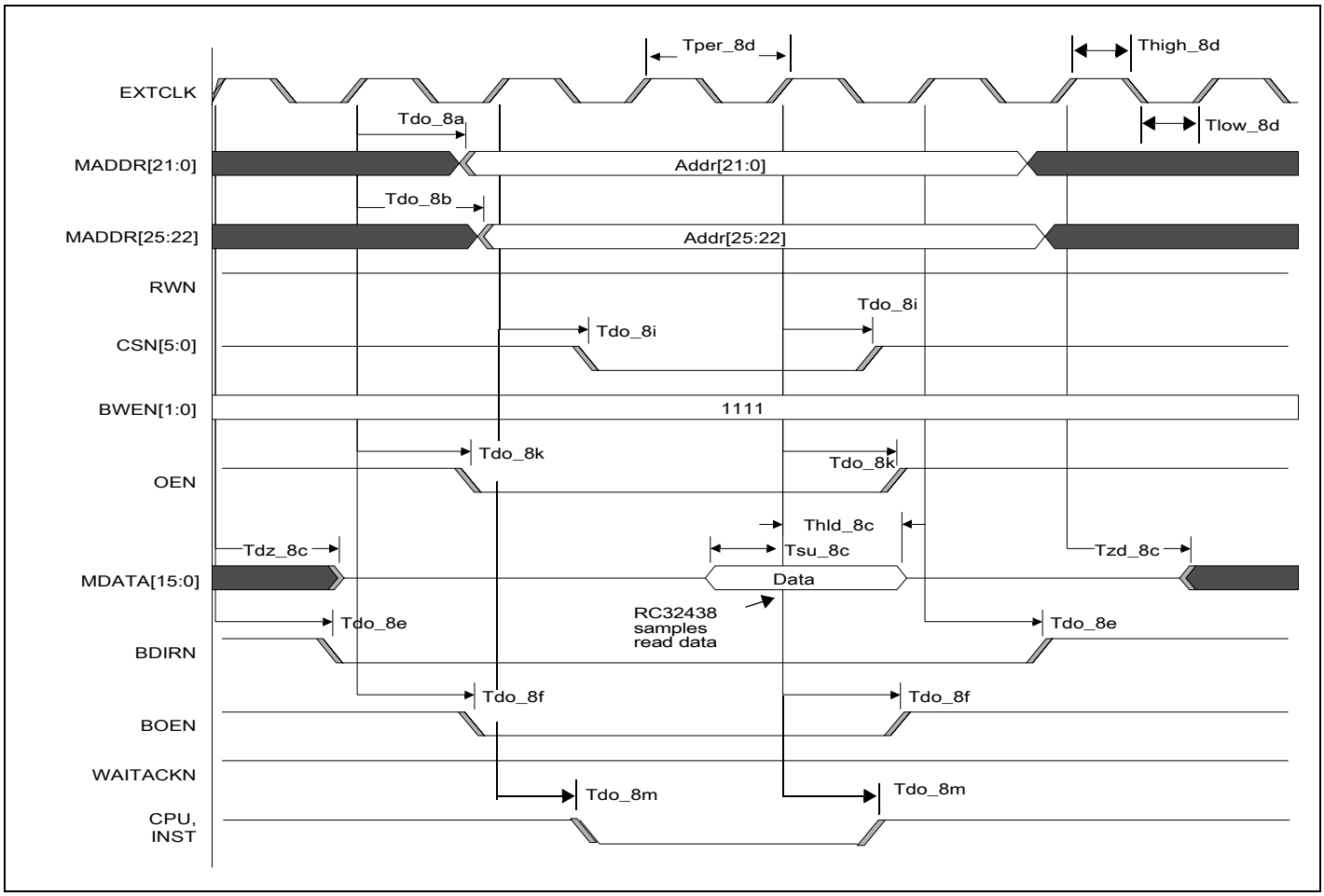


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

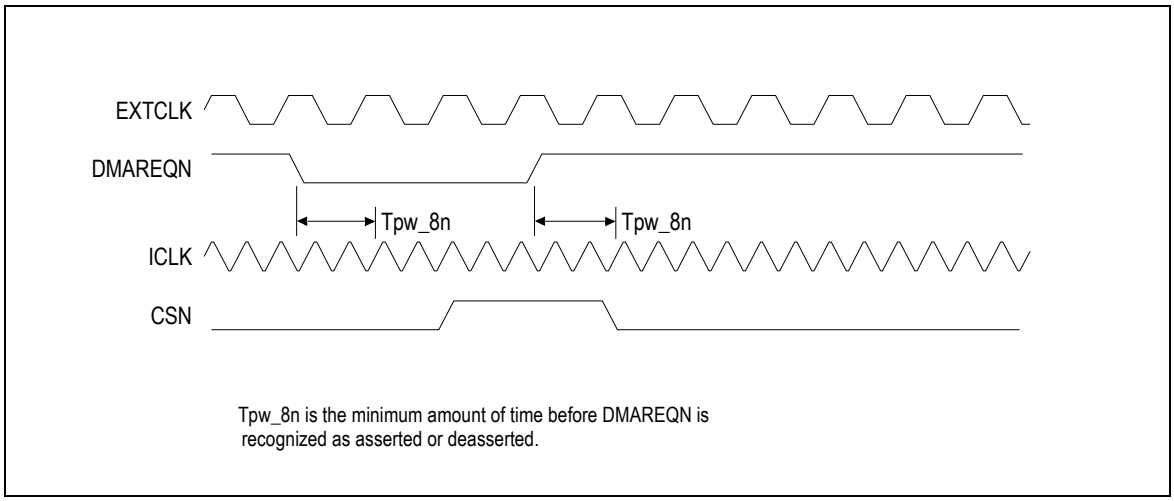


Figure 11 DMAREQN AC Timing Waveform

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Ethernet[1]													
MIIMDC	Tper_9a	None	40.0	—	33.3	—	30.0	—	30.0	—	ns		See Figure 12.
	Thigh_9a, Tlow_9a		16.0	—	13.0	—	12.0	—	12.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9b		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_9b[2]		10	300	10	300	10	300	10	300	ns		
MIIxRXCLK, MIIxTXCLK[3]	Tper_9c	None	399.96	400.4	399.96	400.4	399.96	400.4	399.96	400.4	ns	10 Mbps	
	Thigh_9c, Tlow_9c		140	260	140	260	140	260	140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	—	3.0	—	3.0	—	3.0	ns		
MIIxRXCLK, MIIxTXCLK[3]	Tper_9d	None	39.9	40.0	39.9	40.0	39.9	40.0	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	14.0	26.0	14.0	26.0	14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	—	2.0	—	2.0	—	2.0	ns		
MIIxRXD[3:0], MIIxRXDV, MIIxRXER	Tsu_9e	MIIxRXCLK rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9e		10.0	—	10.0	—	10.0	—	10.0	—	ns		
MIIxTXD[3:0], MIIxTXENP, MIIxTXER	Tdo_9f	MIIxTXCLK rising	0.0	25.0	0.0	25.0	0.0	25.0	0.0	25.0	ns		

Table 9 Ethernet AC Timing Characteristics

1. There are two MII interfaces and the timing is the same for each. "X" represents interface 0 or 1.

2. The values for this symbol were determined by calculation, not by testing.

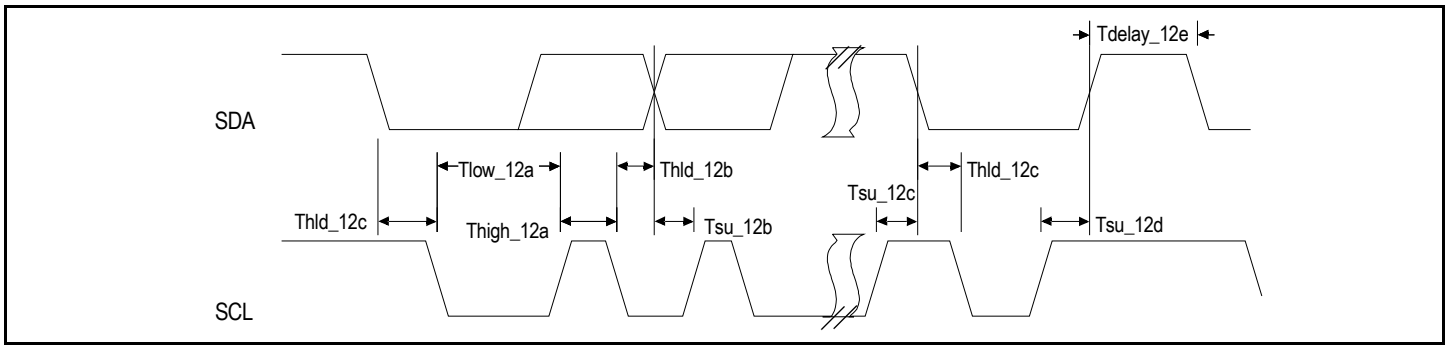


Figure 16 I²C AC Timing Waveform

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[31:0][1]	Tpw_13b[2]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 17.

Table 12 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

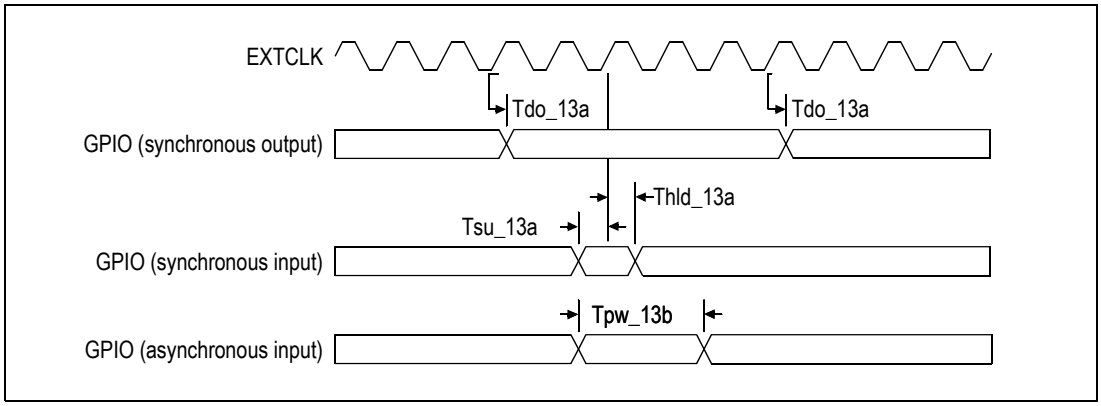


Figure 17 GPIO AC Timing Waveform

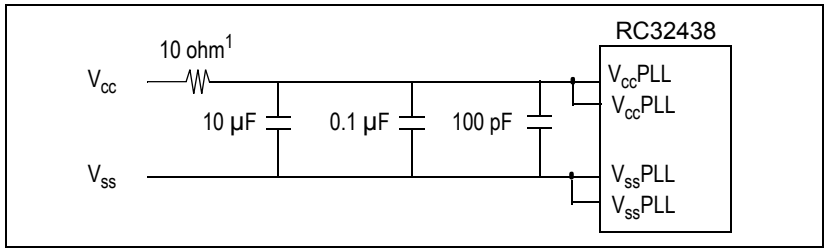


Figure 25 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Clock Speed	Minimum	Typical	Maximum	Unit
V_{ss}	Common ground	All speeds	0	0	0	V
V_{ss}PLL	PLL ground					
V_{cc}I/O	I/O supply except for SSTL_2[1]		3.0	3.3	3.6	V
V_{cc}SI/O	I/O supply for SSTL_2[1]		2.3	2.5	2.7	V
V_{cc}PLL	PLL supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
V_{cc}Core	Internal logic supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
DDRVREF[2]	SSTL_2 input reference voltage	All speeds	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage		DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32438 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.

2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).

3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32438 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32438 IBIS Model on the IDT web site (www.idt.com).

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O	I/O supply for SSTL_2[2]	-0.6	3.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply	-0.6	2.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B9	MDATA[11]		G3	MII0TXCLK		V3	GPIO[05]	1	AD25	DDROEN[02]	
B10	MDATA[03]		G4	V_{ss}		V4	V_{ss}		AD26	DDROEN[01]	
B11	MDATA[08]		G23	V_{ss}		V23	V_{ss}		AE1	N/C	
B12	MDATA[02]		G24	DDRCKP[00]		V24	DDRADDR[08]		AE2	GPIO[13]	1
B13	GPIO[23]	1	G25	DDRDATA[16]		V25	DDRRASN		AE3	GPIO[18]	1
B14	MADDR[20]		G26	DDRDATA[13]		V26	DDRCASN		AE4	GPIO[24]	1
B15	GPIO[20]	1	H1	MII1CRS		W1	GPIO[04]	1	AE5	GPIO[26]	1
B16	MADDR[17]		H2	MII1CL		W2	SCK		AE6	PCIAD[31]	
B17	MADDR[14]		H3	MII1RXCLK		W3	CLK		AE7	PCIAD[28]	
B18	MADDR[12]		H4	V_{ss}		W4	V_{ss}		AE8	PCIAD[25]	
B19	MADDR[09]		H23	V_{ss}		W23	V_{ss}		AE9	GPIO[30]	1
B20	MADDR[06]		H24	DDRCKN[00]		W24	DDRADDR[07]		AE10	PCIAD[22]	
B21	MADDR[03]		H25	DDRDATA[18]		W25	DDRADDR[06]		AE11	PCIAD[19]	
B22	MADDR[00]		H26	DDRVREF		W26	DDRBA[01]		AE12	PCIAD[16]	
B23	DDRDATA[01]		J1	MII1RXD[01]		Y1	GPIO[06]	1	AE13	PCIRSTN	
B24	DDRDQS[00]		J2	MII1RXD[00]		Y2	V_{cc} PLL		AE14	PCIREQN[02]	
B25	DDRDM[00]		J3	MII1RXD[03]		Y3	GPIO[08]	1	AE15	PCIFRAMEN	
B26	DDRDATA[06]		J4	V_{ss}		Y4	V_{ss}		AE16	PCIDEVSELN	
C1	MII0RXD[00]		J23	V_{ss}		Y23	V_{ss}		AE17	PCILOCKN	
C2	MII0RXCLK		J24	DDRDATA[17]		Y24	DDRCKN[01]		AE18	PCICBEN[01]	
C3	EXTCLK		J25	DDRDATA[21]		Y25	DDRBA[00]		AE19	PCIAD[13]	
C4	COLDRSTN		J26	DDRDATA[19]		Y26	DDRADDR[05]		AE20	PCIAD[10]	
C5	OEN		K1	MII1RXDV		AA1	V_{ss} PLL		AE21	PCICBEN[00]	
C6	CSN[03]		K2	MII1RXD[02]		AA2	GPIO[07]	1	AE22	PCIAD[05]	
C7	CSN[00]		K3	MII1TXCLK		AA3	V_{cc} PLL		AE23	PCIAD[02]	
C8	BRN		K4	V_{cc} Core		AA4	V_{ss}		AE24	PCIGNTN[01]	
C9	BDIRN		K23	V_{ss}		AA23	V_{ss}		AE25	DDRDM[07]	
C10	MDATA[12]		K24	DDRDATA[20]		AA24	DDRCKP[01]		AE26	DDRDM[04]	
C11	MDATA[09]		K25	DDRDQS[02]		AA25	DDRADDR[03]		AF1	GPIO[16]	1
C12	MDATA[01]		K26	DDRCKE		AA26	DDRADDR[04]		AF2	GPIO[17]	1
C13	MDATA[05]		L1	MII1TXD[00]		AB1	GPIO[09]	1	AF3	GPIO[19]	1
C14	MDATA[04]		L2	MII1RXER		AB2	GPIO[14]	1	AF4	SCL	
C15	MDATA[00]		L3	MII1TXD[03]		AB3	GPIO[11]	1	AF5	GPIO[28]	1
C16	GPIO[21]	1	L4	V_{cc} Core		AB4	V_{ss}		AF6	PCIAD[29]	
C17	MADDR[18]		L23	V_{cc} Core		AB23	V_{ss}		AF7	PCIAD[27]	
C18	MADDR[15]		L24	DDRDM[02]		AB24	V_{cc} SI/O		AF8	PCIAD[24]	
C19	MADDR[11]		L25	DDRDATA[24]		AB25	DDRADDR[01]		AF9	PCIAD[23]	

Table 20 RC32438 416-pin Signal Pin-Out (Part 2 of 3)

Signal Name	I/O Type	Location	Signal Category
DDRADDR[00]	O	AC26	DDR Bus
DDRADDR[01]	O	AB25	
DDRADDR[02]	O	AB26	
DDRADDR[03]	O	AA25	
DDRADDR[04]	O	AA26	
DDRADDR[05]	O	Y26	
DDRADDR[06]	O	W25	
DDRADDR[07]	O	W24	
DDRADDR[08]	O	V24	
DDRADDR[09]	O	U26	
DDRADDR[10]	O	T25	
DDRADDR[11]	O	U24	
DDRADDR[12]	O	T26	
DDRADDR[13]	O	R25	
DDRBA[00]	O	Y25	
DDRBA[01]	O	W26	
DDRCASN	O	V26	
DDRCKE	O	K26	
DDRCKN[00]	O	H24	
DDRCKN[01]	O	Y24	
DDRCKP[00]	O	G24	
DDRCKP[01]	O	AA24	
DDRCSN[00]	O	T24	
DDRCSN[01]	O	R26	
DDRDATA[00]	I/O	C23	
DDRDATA[01]	I/O	B23	
DDRDATA[02]	I/O	A24	
DDRDATA[03]	I/O	C24	
DDRDATA[04]	I/O	A25	
DDRDATA[05]	I/O	A26	
DDRDATA[06]	I/O	B26	
DDRDATA[07]	I/O	C26	
DDRDATA[08]	I/O	C25	
DDRDATA[09]	I/O	E24	
DDRDATA[10]	I/O	D26	

Table 24 RC32438 Alphabetical Signal List (Part 2 of 9)

Signal Name	I/O Type	Location	Signal Category
DDRDATA[11]	I/O	D25	DDR Bus
DDRDATA[12]	I/O	E25	
DDRDATA[13]	I/O	G26	
DDRDATA[14]	I/O	F26	
DDRDATA[15]	I/O	F25	
DDRDATA[16]	I/O	G25	
DDRDATA[17]	I/O	J24	
DDRDATA[18]	I/O	H25	
DDRDATA[19]	I/O	J26	
DDRDATA[20]	I/O	K24	
DDRDATA[21]	I/O	J25	
DDRDATA[22]	I/O	L26	
DDRDATA[23]	I/O	M24	
DDRDATA[24]	I/O	L25	
DDRDATA[25]	I/O	M26	
DDRDATA[26]	I/O	N24	
DDRDATA[27]	I/O	M25	
DDRDATA[28]	I/O	N25	
DDRDATA[29]	I/O	R24	
DDRDATA[30]	I/O	P26	
DDRDATA[31]	I/O	P25	
DDRDM[00]	O	B25	
DDRDM[01]	O	E26	
DDRDM[02]	O	L24	
DDRDM[03]	O	P24	
DDRDM[04]	O	AE26	
DDRDM[05]	O	AD24	
DDRDM[06]	O	AF25	
DDRDM[07]	O	AE25	
DDRDQS[00]	I/O	B24	
DDRDQS[01]	I/O	F24	
DDRDQS[02]	I/O	K25	
DDRDQS[03]	I/O	N26	
DDROEN[00]	O	AC25	
DDROEN[01]	O	AD26	

Table 24 RC32438 Alphabetical Signal List (Part 3 of 9)

Signal Name	I/O Type	Location	Signal Category
DDROEN[02]	O	AD25	DDR Bus
DDROEN[03]	O	AF26	
DDRRASN	O	V25	
DDRVREF	I	H26	
DDRWEN	O	U25	
EJTAG_TMS	I	R2	EJTAG/ICE
EXTCLK	O	C3	System
GPIO[00]	I/O	P1	General Purpose Input/Output
GPIO[01]	I/O	N3	
GPIO[02]	I/O	P3	
GPIO[03]	I/O	T2	
GPIO[04]	I/O	W1	
GPIO[05]	I/O	V3	
GPIO[06]	I/O	Y1	
GPIO[07]	I/O	AA2	
GPIO[08]	I/O	Y3	
GPIO[09]	I/O	AB1	
GPIO[10]	I/O	AC2	
GPIO[11]	I/O	AB3	
GPIO[12]	I/O	AC3	
GPIO[13]	I/O	AE2	
GPIO[14]	I/O	AB2	
GPIO[15]	I/O	AD3	
GPIO[16]	I/O	AF1	
GPIO[17]	I/O	AF2	
GPIO[18]	I/O	AE3	
GPIO[19]	I/O	AF3	
GPIO[20]	I/O	B15	
GPIO[21]	I/O	C16	
GPIO[22]	I/O	A14	
GPIO[23]	I/O	B13	
GPIO[24]	I/O	AE4	
GPIO[25]	I/O	A2	
GPIO[26]	I/O	AE5	
GPIO[27]	I/O	AD5	

Table 24 RC32438 Alphabetical Signal List (Part 4 of 9)

Signal Name	I/O Type	Location	Signal Category
GPIO[28]	I/O	AF5	General Purpose Input/Output
GPIO[29]	I/O	A13	
GPIO[30]	I/O	AE9	
GPIO[31]	I/O	A3	
INST	O	R1	Debug
JTAG_TCK	I	U2	EJTAG/ICE
JTAG_TDI	I	U1	
JTAG_TDO	O	U3	
JTAG_TMS	I	AD2	
JTAG_TRST_N	I	AD1	
MADDR[00]	O	B22	Memory and Peripheral Bus
MADDR[01]	O	C22	
MADDR[02]	O	A22	
MADDR[03]	O	B21	
MADDR[04]	O	C21	
MADDR[05]	O	A21	
MADDR[06]	O	B20	
MADDR[07]	O	A20	
MADDR[08]	O	C20	
MADDR[09]	O	B19	
MADDR[10]	O	A19	
MADDR[11]	O	C19	
MADDR[12]	O	B18	
MADDR[13]	O	A18	
MADDR[14]	O	B17	
MADDR[15]	O	C18	
MADDR[16]	O	A17	
MADDR[17]	O	B16	
MADDR[18]	O	C17	
MADDR[19]	O	A16	
MADDR[20]	O	B14	
MADDR[21]	O	A15	
MDATA[00]	I/O	C15	
MDATA[01]	I/O	C12	

Table 24 RC32438 Alphabetical Signal List (Part 5 of 9)

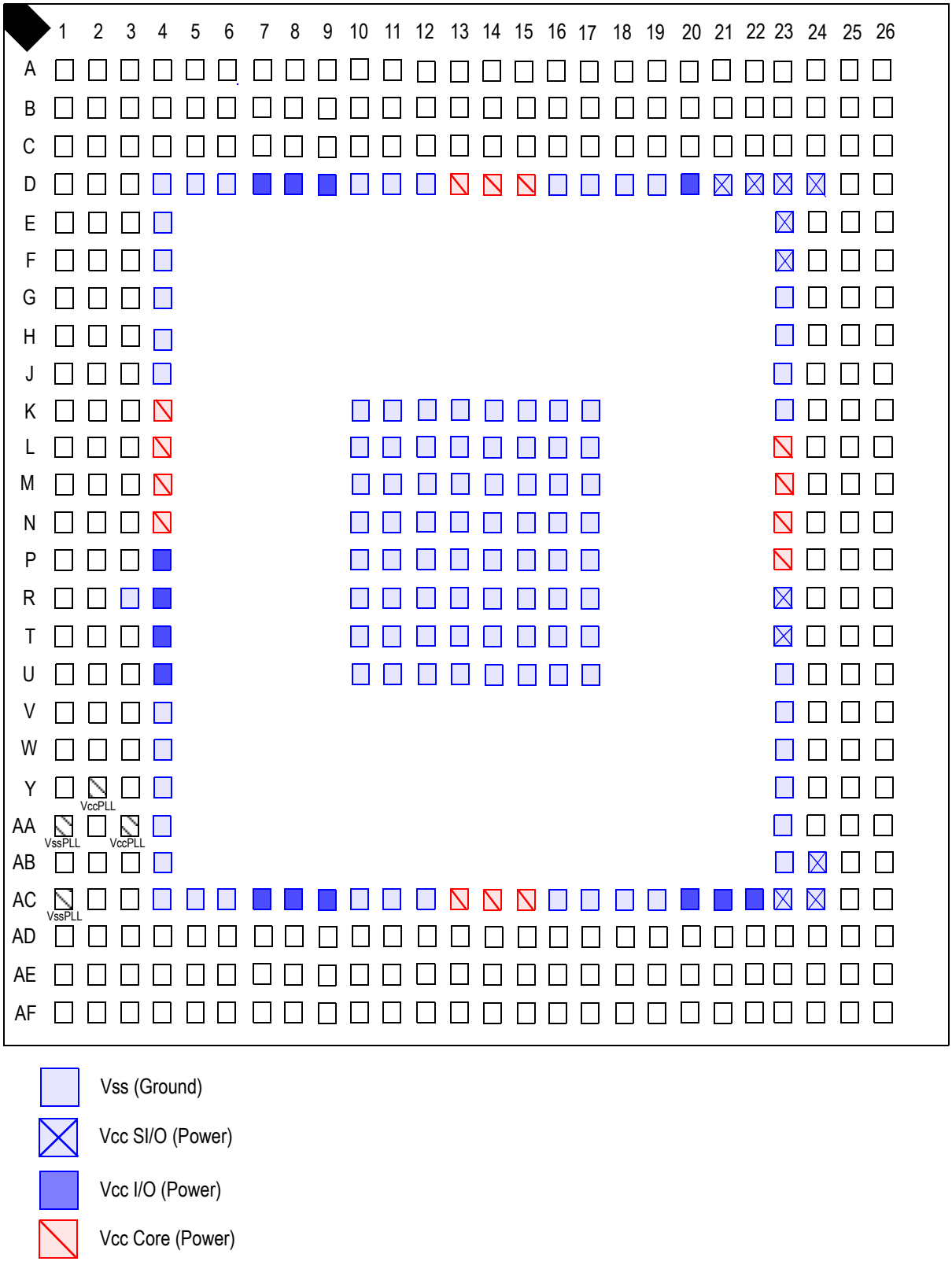
Signal Name	I/O Type	Location	Signal Category
MII1RXD[02]	I	K2	Ethernet Interfaces
MII1RXD[03]	I	J3	
MII1RXDV	I	K1	
MII1RXER	I	L2	
MII1TXCLK	I	K3	
MII1TXD[00]	O	L1	
MII1TXD[01]	O	M2	
MII1TXD[02]	O	M1	
MII1TXD[03]	O	L3	
MII1TXENP	O	N2	
MII1TXER	O	N1	
MIIMDC	O	M3	
MIIMDIO	I/O	P2	
OEN	O	C5	Memory and Peripheral Bus
PCIAD[00]	I/O	AD22	PCI Bus
PCIAD[01]	I/O	AF23	
PCIAD[02]	I/O	AE23	
PCIAD[03]	I/O	AF22	
PCIAD[04]	I/O	AD23	
PCIAD[05]	I/O	AE22	
PCIAD[06]	I/O	AD20	
PCIAD[07]	I/O	AF21	
PCIAD[08]	I/O	AD19	
PCIAD[09]	I/O	AF20	
PCIAD[10]	I/O	AE20	
PCIAD[11]	I/O	AD18	
PCIAD[12]	I/O	AF19	
PCIAD[13]	I/O	AE19	
PCIAD[14]	I/O	AF18	
PCIAD[15]	I/O	AD17	
PCIAD[16]	I/O	AE12	
PCIAD[17]	I/O	AF11	
PCIAD[18]	I/O	AD10	
PCIAD[19]	I/O	AE11	
PCIAD[20]	I/O	AF10	

Table 24 RC32438 Alphabetical Signal List (Part 7 of 9)

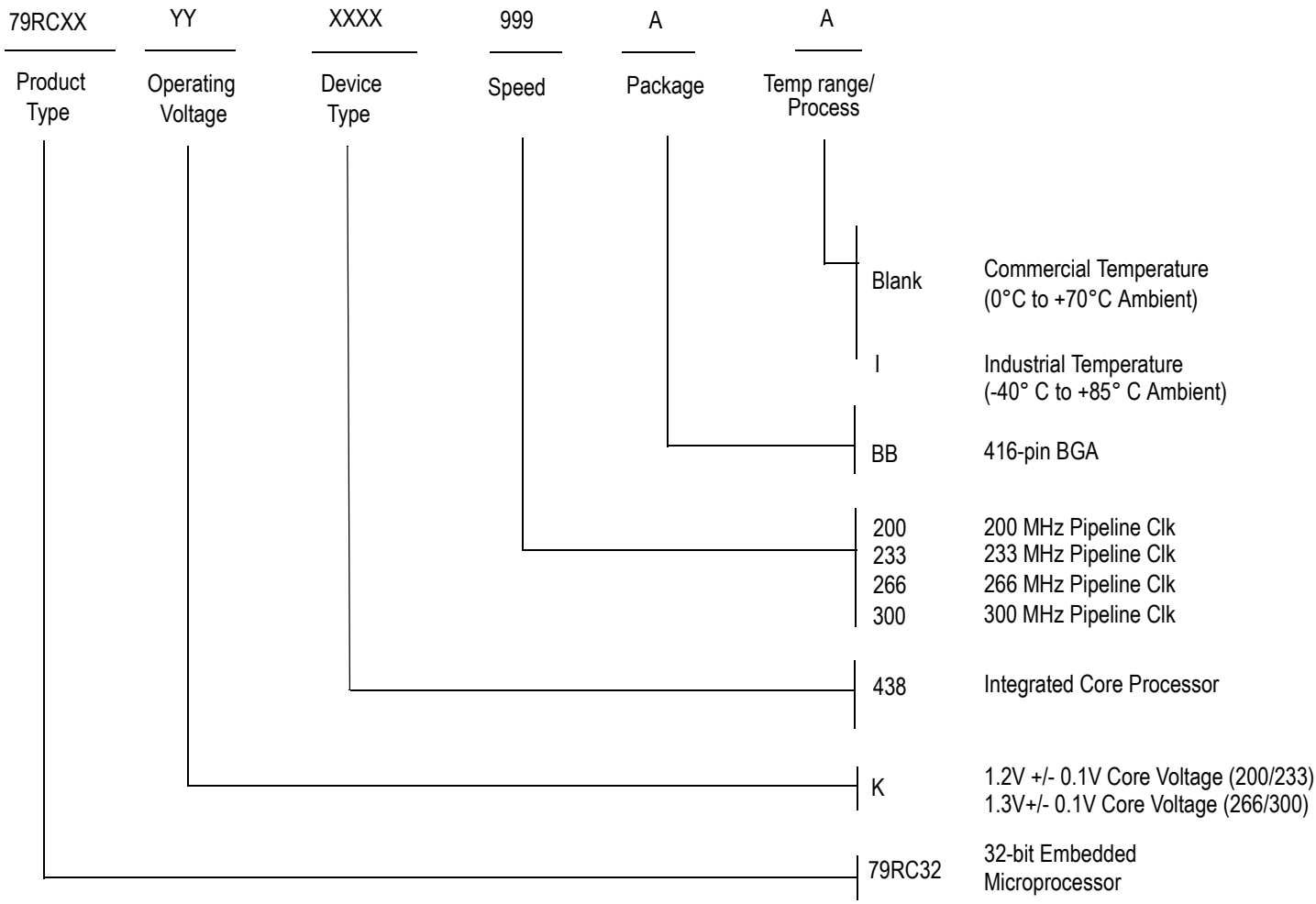
Signal Name	I/O Type	Location	Signal Category
PCIAD[21]	I/O	AD9	PCI Bus
PCIAD[22]	I/O	AE10	
PCIAD[23]	I/O	AF9	
PCIAD[24]	I/O	AF8	
PCIAD[25]	I/O	AE8	
PCIAD[26]	I/O	AD7	
PCIAD[27]	I/O	AF7	
PCIAD[28]	I/O	AE7	
PCIAD[29]	I/O	AF6	
PCIAD[30]	I/O	AD6	
PCIAD[31]	I/O	AE6	
PCICBEN[00]	I/O	AE21	
PCICBEN[01]	I/O	AE18	
PCICBEN[02]	I/O	AF14	
PCICBEN[03]	I/O	AD8	
PCICLK	I	AD12	
PCIDEVSELN	I/O	AE16	
PCIFRAMEN	I/O	AE15	
PCIGNTN[00]	I/O	AD13	
PCIGNTN[01]	I/O	AE24	
PCIGNTN[02]	I/O	AF24	
PCIGNTN[03]	I/O	AD21	
PCIIRDYN	I/O	AD14	
PCILOCKN	I/O	AE17	
PCIPAR	I/O	AF17	
PCIPERRN	I/O	AD16	
PCIREQN[00]	I/O	AF13	
PCIREQN[01]	I/O	AD11	
PCIREQN[02]	I/O	AE14	
PCIREQN[03]	I/O	AF12	
PCIRSTN	I/O	AE13	
PCISERRN	I/O	AF16	
PCISTOPN	I/O	AD15	
PCITRDYN	I/O	AF15	
RSTN	I/O	A23	System
RWN	O	B3	Memory and Peripheral Bus

Table 24 RC32438 Alphabetical Signal List (Part 8 of 9)

RC32438 Pinout — Top View



Ordering Information



Valid Combinations

79RC32K438 -200BB, 233BB, 266BB, 300BB	416-pin BGA package, Commercial Temperature
79RC32K438 -200BBI, 233BBI	416-pin BGA package, Industrial Temperature

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