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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	416-BGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32k438-300bbg

card application, or as the primary PCI controller in the system. The PCI interface can be operated synchronously or asynchronously to the other I/O interfaces on the RC32438 device.

Ethernet Interface

The RC32438 has two Ethernet Channels supporting 10Mbps and 100Mbps speeds to provide a standard media independent interface (MII) off-chip, allowing a wide range of external devices to be connected efficiently.

UART Interface

The RC32438 contains two completely separate serial channels (UARTs) that are compatible with the industry standard 16550 UART.

System Integrity Functions

The RC32438 contains a programmable watchdog timer that generates NMI when the counter expires and an address space monitor that reports errors in response to accesses to undecoded address regions.

General Purpose I/O Controller

The RC32438 contains 32 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

I^2C Interface

The standard I2C interface allows the RC32438 to connect to a number of standard external peripherals for a more complete system solution. The RC32438 supports both master and slave operations.

Debug Support

The RC32438 supports the industry standard Rev. 2.6 EJTAG interface.

Thermal Considerations

The RC32438 consumes less than 2.7 W peak power. It is guaranteed in a ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

November 7, 2002: Initial publication. Preliminary Information.

November 15, 2002: Added footnotes to Tables 5, 9, and 10.

December 12, 2002: Added Clock Speed parameter to PLL and Core supply in Table 16.

December 19, 2002: Release version.

January 13, 2003: Changed Thermal Considerations to read less than 2.7W instead of 2.5W, added values to CLK parameter in Table 5, and revised EJTAG description.

February 4, 2003: Revised description for EJTAG/JTAG pins in Table 1. Changed DDRDM[7:0] from input/output to output only in Tables 1 and 2 and Logic Diagram. Added new section, Voltage Sense Signal Timing, as part of EJTAG description.

March 4, 2003: In Table 2, removed “pull-up” from PCI pin category and from GPIO [24] and GPIO[30-26]. In Table 20, changed max. values for VccSI/O, VccCore, and VccPLL.

July 9, 2003: In Table 7: changed values for DDRDATA, DDRDM, and DDRADDR—WEN signals, and deleted old footnote #3 and changed values in new footnote #3. In Table 8, changed Tdo values. Changed Figure 7. Changed values in Table 18, Power Consumption. Removed IPBus Monitor feature which included changes to Tables 1, 2, 21, 24, and 25. Deleted Table 13 which resulted in a re-ordering of subsequent tables.

March 8, 2004: Added 300MHz speed grade.

May 25, 2004: In Table 9, signals MIIxRXCLK and MIIxTXCLK, the Min and Max values for Thigh/Tlow_9c were changed to 140 and 260 respectively and the Min and Max values for Thigh/Tlow_9d were changed to 14.0 and 26.0 respectively.

Signal	Type	Name/Description
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send output.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send input.
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1SOUT Alternate function: UART channel 1 serial output.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1SINP Alternate function: UART channel 1 serial input.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1DTRN Alternate function: UART channel 1 data terminal ready output.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1DSRN Alternate function: UART channel 1 data set ready input.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1RTSN Alternate function: UART channel 1 request to send output.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U1CTSN Alternate function: UART channel 1 clear to send input.
GPIO[14]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAREQN0 Alternate function: External DMA channel 0 request input.
GPIO[15]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMAREQN1 Alternate function: External DMA channel 1 request input.
GPIO[16]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMADONEN0 Alternate function: External DMA channel 0 done input.
GPIO[17]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: DMADONEN1 Alternate function: External DMA channel 1 done input.

Table 1 Pin Description (Part 5 of 9)

Signal	Type	Name/Description
GPIO[30]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
GPIO[31]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output in SPI mode and in PCI satellite mode with suspended CPU execution during PCI serial EEPROM loading. This pin may be configured as a GPIO pin.
SDI	I/O	**Serial Data Input**. This signal is used to shift in serial data in SPI mode and in PCI satellite mode with suspended CPU execution during PCI serial EEPROM loading. This pin may be configured as a GPIO pin.
SDO	I/O	**Serial Data Output**. This signal is used shift out serial data in SPI mode and in PCI satellite mode with suspended CPU execution during PCI serial EEPROM loading. This pin may be configured as a GPIO pin.
I^2C Bus Interface		
SCL	I/O	**I^2C Clock.** I^2C-bus clock.
SDA	I/O	**I^2C Data Bus.** I^2C-bus data bus.
Ethernet Interfaces		
MII0CL	I	**Ethernet 0 MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.
MII0CRS	I	**Ethernet 0 MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII0RXCLK	I	**Ethernet 0 MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MII0RXD[3:0]	I	**Ethernet 0 MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MII0RXDV	I	**Ethernet 0 MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII0RXER	I	**Ethernet 0 MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII0TXCLK	I	**Ethernet 0 MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII0TXD[3:0]	O	**Ethernet 0 MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MII0TXENP	O	**Ethernet 0 MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MII0TXER	O	**Ethernet 0 MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MII1CL	I	**Ethernet 1 MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.

Table 1 Pin Description (Part 7 of 9)

Signal	Type	Name/Description
MII1CRS	I	**Ethernet 1 MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII1RXCLK	I	**Ethernet 1 MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MII1RXD[3:0]	I	**Ethernet 1 MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MII1RXDV	I	**Ethernet 1 MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII1RXER	I	**Ethernet 1 MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII1TXCLK	I	**Ethernet 1 MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII1TXD[3:0]	O	**Ethernet 1 MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MII1TXENP	O	**Ethernet 1 MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MII1TXER	O	**Ethernet 1 MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
JTAG / EJTAG		
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 8 of 9)

Signal	Name/Description
MDATA[7]	**Boot Device Width**. This field specifies the width of the boot device (i.e., Device 0). 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width
MDATA[8]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4096 clock cycles 0x1 - reserved
MDATA[11:9]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*
MDATA[12]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MDATA[15:13]	**Reserved**. These pins must be driven low during boot configuration.

Table 3 Boot Configuration Encoding (Part 2 of 2)

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.

Parameter	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	200	200	233	200	266	200	300	MHz	See Figure 3.
	Tper		5.0	5.0	4.2	5.0	3.8	5.0	3.3	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	100	100	116.5	100	133	100	150	MHz	
	Tper		10.0	10.0	10.0	8.5	10.0	7.5	6.7	10.0	ns	
CLK[5]	Frequency	none	25	66.6	25	77.6	25	88.6	25	100	MHz	
	Tper_5a		15.0	40.0	12.9	40.0	11.2	40.0	10	40	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3).
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

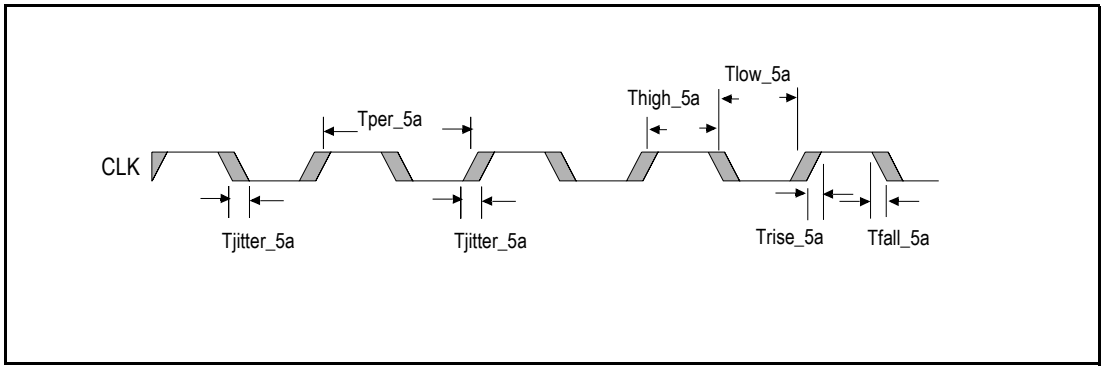
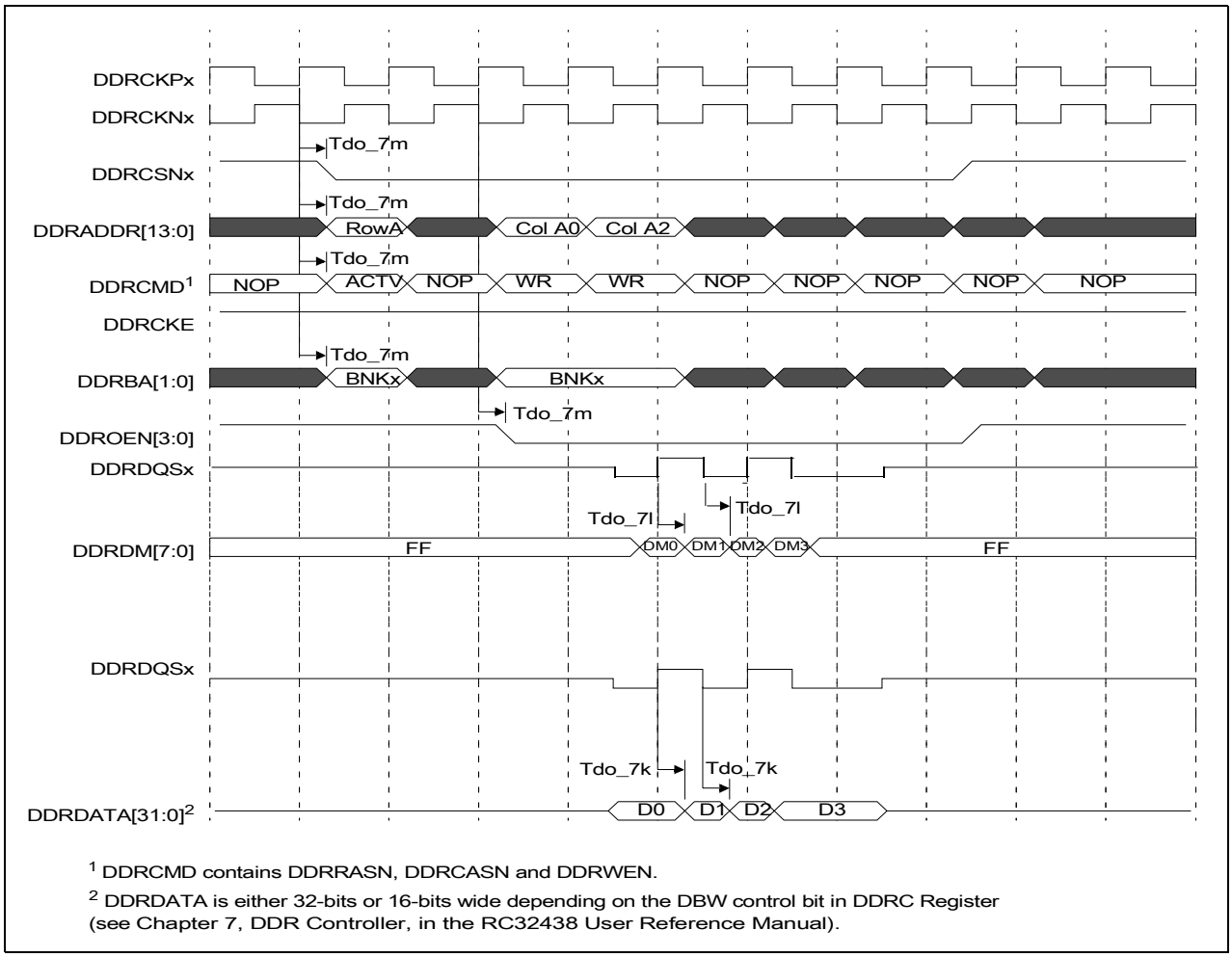


Figure 3 Clock Parameters Waveform



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32438 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns		
	Tdz_8a[2]		0.0	0.1	0.0	0.1	0.0	0.1	0.0	0.1	ns		
	Tzd_8a[2]		0.5	2.3	0.5	2.3	0.5	2.3	0.5	2.3	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.0	6.5	0.0	6.5	0.0	6.5	0.0	6.5	ns		
	Tdz_8b[2]		0.7	1.5	0.7	1.5	0.7	1.5	0.7	1.5	ns		
	Tzd_8b[2]		1.2	3.3	1.2	3.3	1.2	3.3	1.2	3.3	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 3)

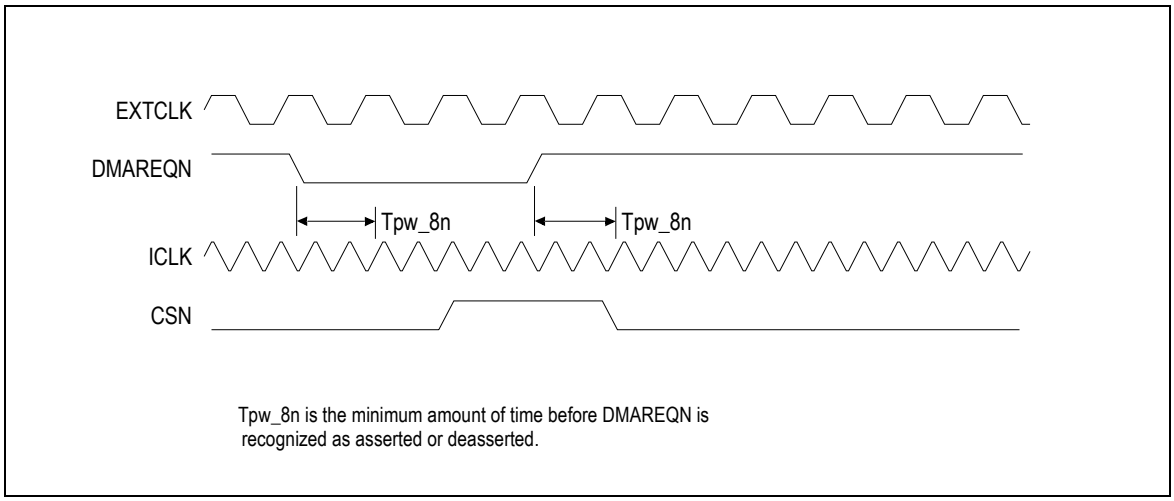


Figure 11 DMAREQN AC Timing Waveform

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Ethernet[1]													
MIIMDC	Tper_9a	None	40.0	—	33.3	—	30.0	—	30.0	—	ns		See Figure 12.
	Thigh_9a, Tlow_9a		16.0	—	13.0	—	12.0	—	12.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9b		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_9b[2]		10	300	10	300	10	300	10	300	ns		
MIIxRXCLK, MIIxTXCLK[3]	Tper_9c	None	399.96	400.4	399.96	400.4	399.96	400.4	399.96	400.4	ns	10 Mbps	
	Thigh_9c, Tlow_9c		140	260	140	260	140	260	140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	—	3.0	—	3.0	—	3.0	ns		
MIIxRXCLK, MIIxTXCLK[3]	Tper_9d	None	39.9	40.0	39.9	40.0	39.9	40.0	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	14.0	26.0	14.0	26.0	14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	—	2.0	—	2.0	—	2.0	ns		
MIIxRXD[3:0], MIIxRXDV, MIIxRXER	Tsu_9e	MIIxRXCLK rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9e		10.0	—	10.0	—	10.0	—	10.0	—	ns		
MIIxTXD[3:0], MIIxTXENP, MIIxTXER	Tdo_9f	MIIxTXCLK rising	0.0	25.0	0.0	25.0	0.0	25.0	0.0	25.0	ns		

Table 9 Ethernet AC Timing Characteristics

1. There are two MII interfaces and the timing is the same for each. "X" represents interface 0 or 1.

2. The values for this symbol were determined by calculation, not by testing.

[3] The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).

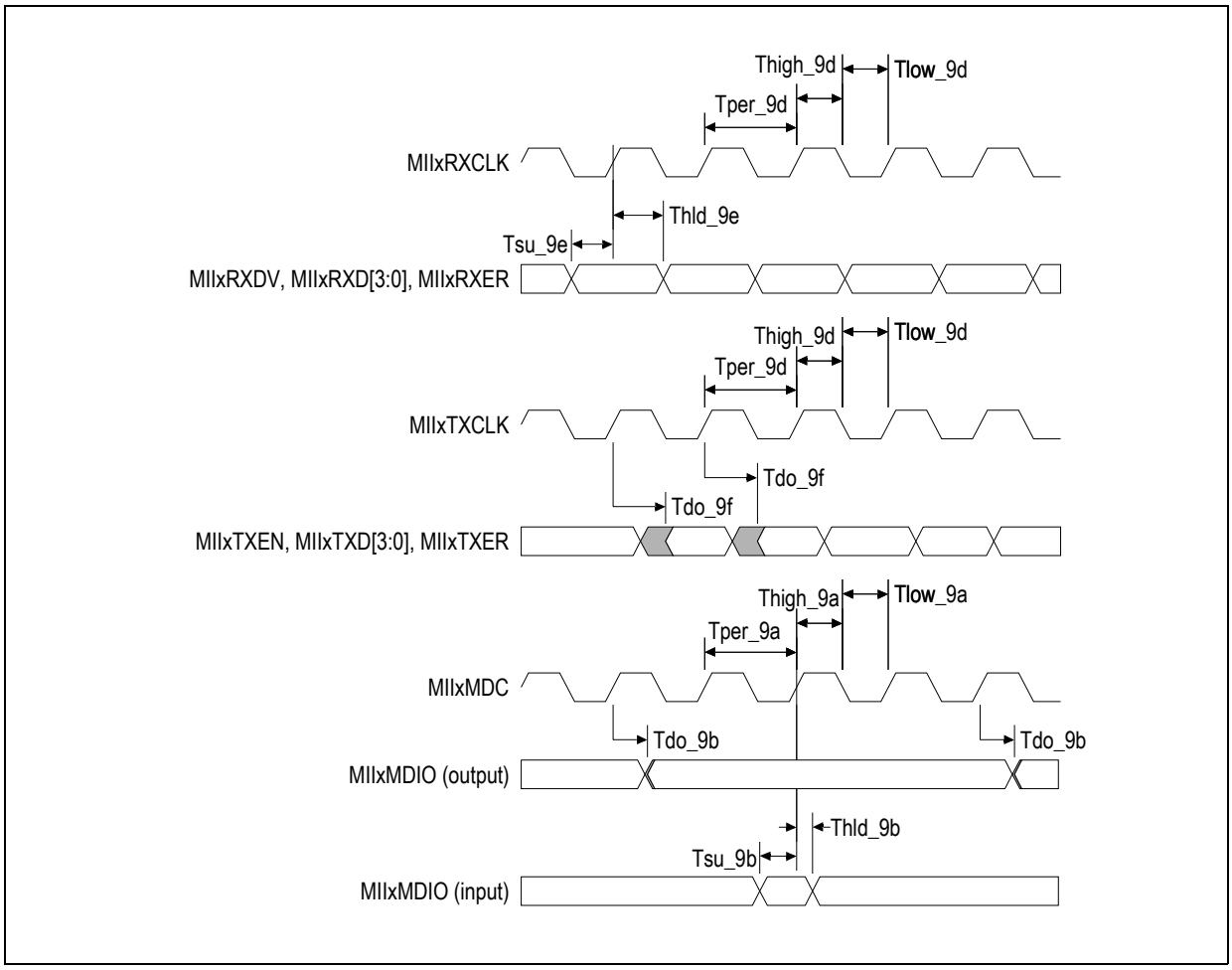


Figure 12 Ethernet AC Timing Waveform

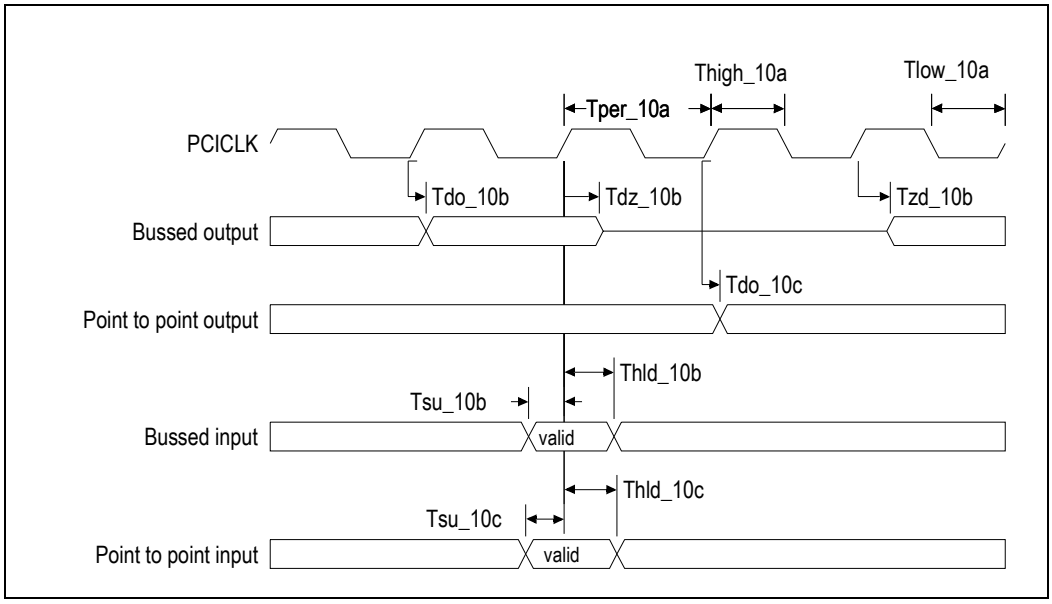


Figure 13 PCI AC Timing Waveform

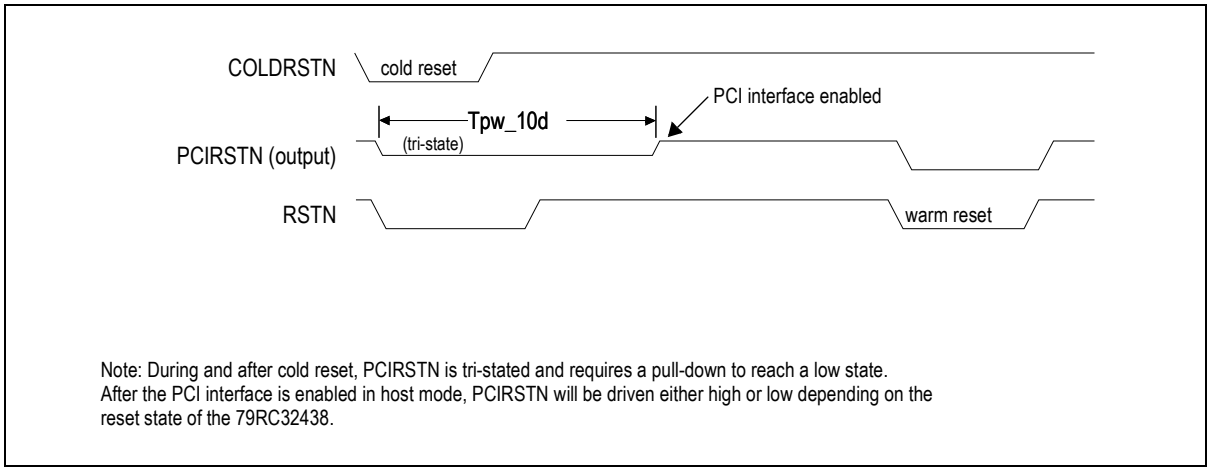


Figure 14 PCI AC Timing Waveform — PCI Reset in Host Mode

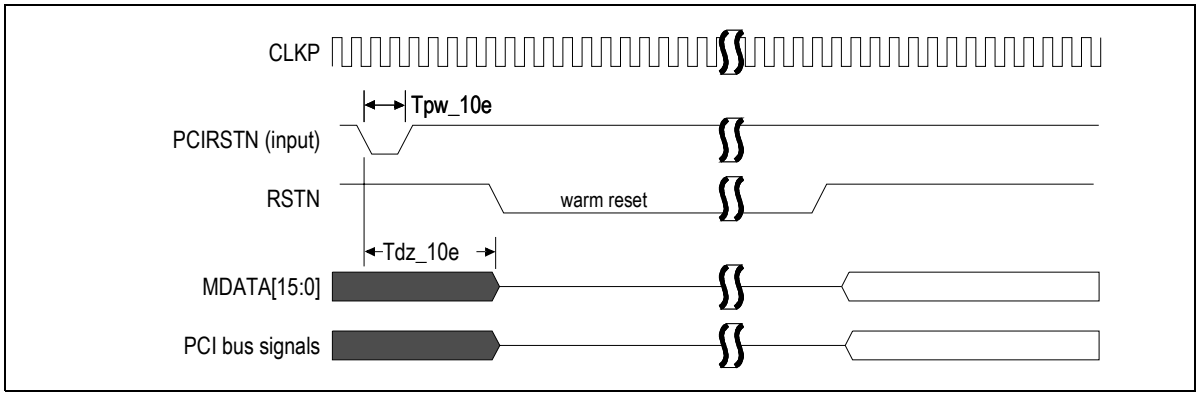


Figure 15 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I^2C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 16.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I^2C AC Timing Characteristics

1. For more information, see the I^2C-Bus specification by Philips Semiconductor.

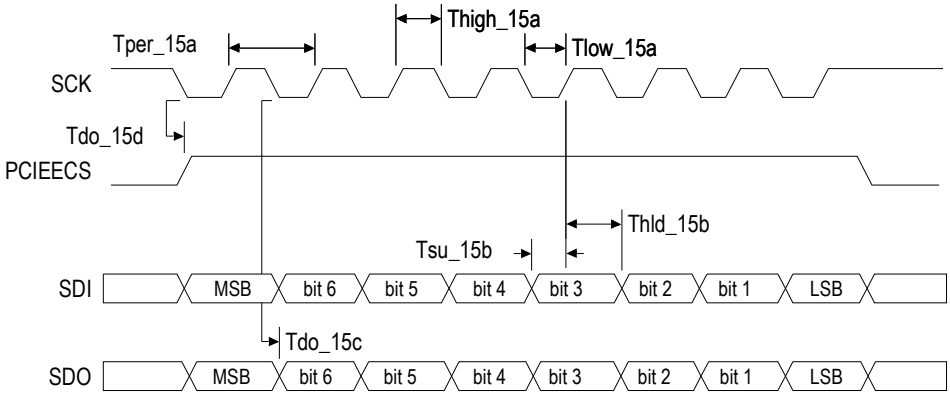
Signal	Symbol	Reference Edge	200MHz		233MHz		266MHz		300MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	—	1920	—	1920	—	1920	—	1920	ns	33 MHz PCI	See Figures 18, 19, 20 and 21.
	Tper_15a		—	960	—	960	—	960	—	960	ns	66 MHz PCI	
	Tper_15a		100	166667	100	166667	100	166667	100	166667	ns	SPI	
	Thigh_15a, Tlow_15a		930	990	930	990	930	990	930	990	ns	33 MHz PCI	
	Thigh_15a, Tlow_15a		465	495	465	495	465	495	465	495	ns	66 MHz PCI	
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI or PCI	
	Thld_15b		60	—	60	—	60	—	60	—	ns		
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI or PCI	
PCIEECS[2]	Tdo_15d	SCK rising or falling	0	60	0	60	0	60	0	60	ns	PCI	
SCK, SDI, SDO[3]	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

2. PCIEECS is the PCI serial EEPROM chip select. It is an alternate function of PCIGNTN[1].

3. In Bit I/O mode, SCK, SDI, and SDO must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.



Loading PCI configuration registers through SPI from an EEPROM.

Figure 18 SPI AC Timing Waveform — PCI Configurations Load

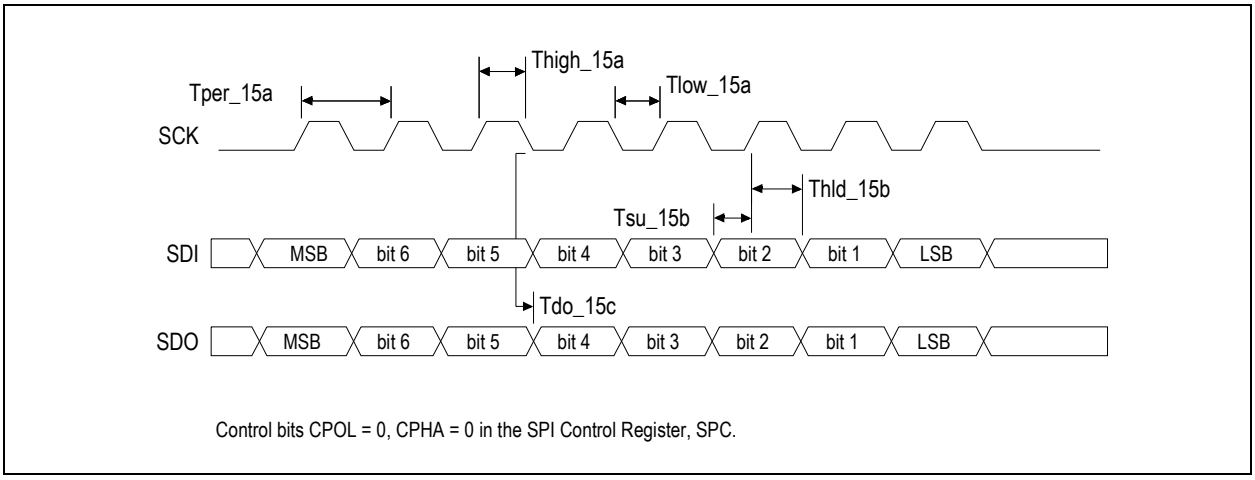


Figure 19 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

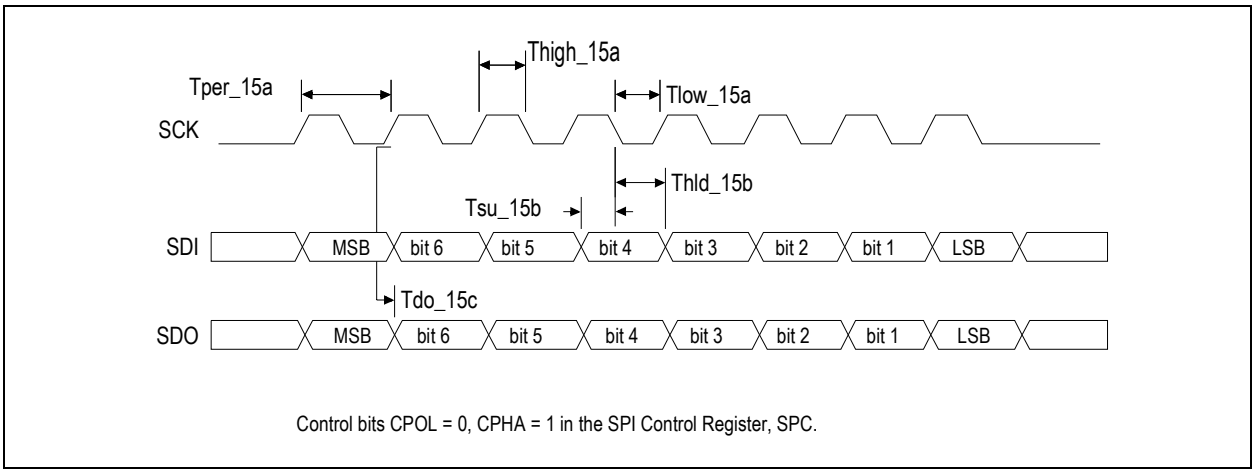


Figure 20 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

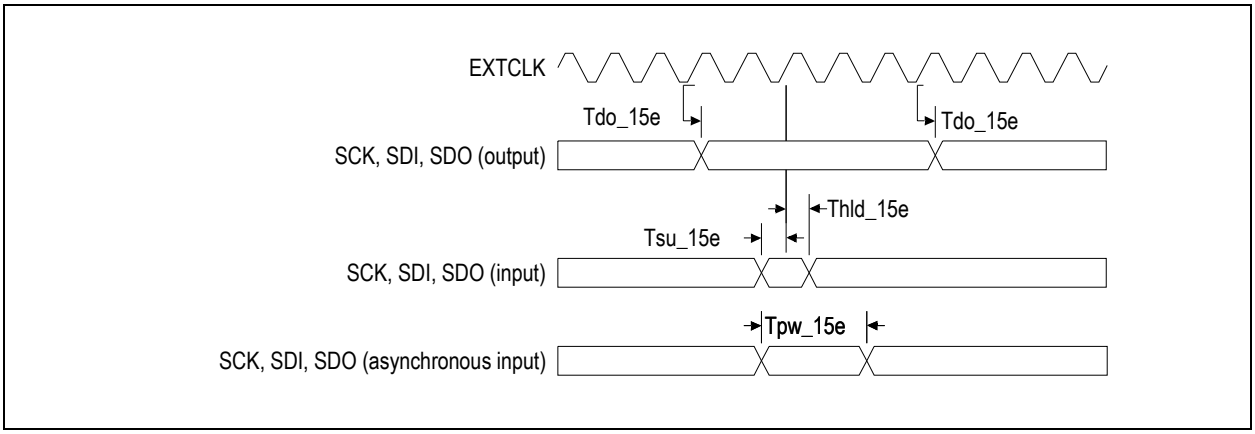


Figure 21 SPI AC Timing Waveform — Bit I/O Mode

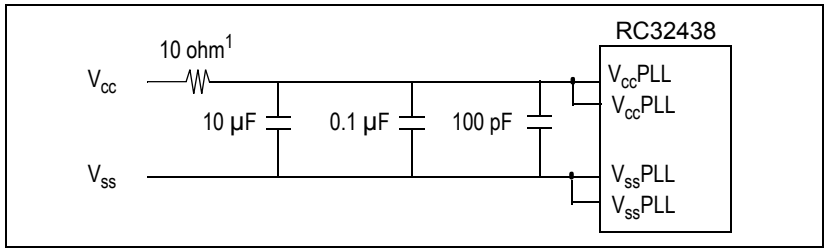


Figure 25 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Clock Speed	Minimum	Typical	Maximum	Unit
V_{ss}	Common ground	All speeds	0	0	0	V
V_{ss}PLL	PLL ground					
V_{cc}I/O	I/O supply except for SSTL_2[1]		3.0	3.3	3.6	V
V_{cc}SI/O	I/O supply for SSTL_2[1]		2.3	2.5	2.7	V
V_{cc}PLL	PLL supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
V_{cc}Core	Internal logic supply	200MHz, 233MHz	1.1	1.2	1.3	V
		266MHz, 300MHz	1.2	1.3	1.4	V
DDRVREF[2]	SSTL_2 input reference voltage	All speeds	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage		DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32438 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.

2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).

3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32438 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32438 IBIS Model on the IDT web site (www.idt.com).

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O	I/O supply for SSTL_2[2]	-0.6	3.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply	-0.6	2.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Package Pin-out — 416-PBGA Signal Pinout for RC32438

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32438 device. Signal names ending with an "_N" or "N" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	MII0CL		D11	V_{ss}		P1	GPIO[00]	1	AC17	V_{ss}	
A2	GPIO[25]	1	D12	V_{ss}		P2	MIIMDIO		AC18	V_{ss}	
A3	GPIO[31]		D13	V_{cc} Core		P3	GPIO[02]	1	AC19	V_{ss}	
A4	CSN[05]		D14	V_{cc} Core		P4	V_{cc} I/O		AC20	V_{cc} I/O	
A5	CSN[02]		D15	V_{cc} Core		P23	V_{cc} CORE		AC21	V_{cc} I/O	
A6	BWEN[01]		D16	V_{ss}		P24	DDRDM[03]		AC22	V_{cc} I/O	
A7	BOEN		D17	V_{ss}		P25	DDRDATA[31]		AC23	Vcc SI/O	
A8	MDATA[15]		D18	V_{ss}		P26	DDRDATA[30]		AC24	Vcc SI/O	
A9	MDATA[14]		D19	V_{ss}		R1	INST		AC25	DDROEN[00]	
A10	MDATA[10]		D20	V_{cc} I/O		R2	EJTAG_TMS		AC26	DDRADDR[00]	
A11	MDATA[07]		D21	Vcc SI/O		R3	V_{ss}		AD1	JTAG_TRST_N	
A12	MDATA[06]		D22	Vcc SI/O		R4	V_{cc} I/O		AD2	JTAG_TMS	
A13	GPIO[29]		D23	Vcc SI/O		R23	Vcc SI/O		AD3	GPIO[15]	1
A14	GPIO[22]	1	D24	Vcc SI/O		R24	DDRDATA[29]		AD4	SDA	
A15	MADDR[21]		D25	DDRDATA[11]		R25	DDRADDR[13]		AD5	GPIO[27]	1
A16	MADDR[19]		D26	DDRDATA[10]		R26	DDRCSN[01]		AD6	PCIAD[30]	
A17	MADDR[16]		E1	MII0TXD[02]		T1	NC		AD7	PCIAD[26]	
A18	MADDR[13]		E2	MII0TXD[00]		T2	GPIO[03]	1	AD8	PCICBEN[03]	
A19	MADDR[10]		E3	MII0TXD[01]		T3	CPU		AD9	PCIAD[21]	
A20	MADDR[07]		E4	V_{ss}		T4	V_{cc} I/O		AD10	PCIAD[18]	
A21	MADDR[05]		E23	Vcc SI/O		T23	Vcc SI/O		AD11	PCIREQN[01]	
A22	MADDR[02]		E24	DDRDATA[09]		T24	DDRCSN[00]		AD12	PCICLK	
A23	RSTN		E25	DDRDATA[12]		T25	DDRADDR[10]		AD13	PCIGNTN[00]	
A24	DDRDATA[02]		E26	DDRDM[01]		T26	DDRADDR[12]		AD14	PCIIRDYN	
A25	DDRDATA[04]		F1	MII0TXER		U1	JTAG_TDI		AD15	PCISTOPN	
A26	DDRDATA[05]		F2	MII0TXD[03]		U2	JTAG_TCK		AD16	PCIPERRN	
B1	MII0CRS		F3	MII0TXENP		U3	JTAG_TDO		AD17	PCIAD[15]	
B2	WAITACKN		F4	V_{ss}		U4	V_{cc} I/O		AD18	PCIAD[11]	
B3	RWN		F23	Vcc SI/O		U23	V_{ss}		AD19	PCIAD[08]	
B4	CSN[04]		F24	DDRDQS[01]		U24	DDRADDR[11]		AD20	PCIAD[06]	
B5	CSN[01]		F25	DDRDATA[15]		U25	DDRWEN		AD21	PCIGNTN[03]	
B6	BWEN[00]		F26	DDRDATA[14]		U26	DDRADDR[09]		AD22	PCIAD[00]	
B7	BGN		G1	MII0RXER		V1	SDO		AD23	PCIAD[04]	
B8	MDATA[13]		G2	MII0RXDV		V2	SDI		AD24	DDRDM[05]	

Table 20 RC32438 416-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C20	MADDR[08]		L26	DDRDATA[22]		AB26	DDRADDR[02]		AF10	PCIAD[20]	
C21	MADDR[04]		M1	MII1TXD[02]		AC1	V_{ss} PLL		AF11	PCIAD[17]	
C22	MADDR[01]		M2	MII1TXD[01]		AC2	GPIO[10]	1	AF12	PCIREQN[03]	
C23	DDRDATA[00]		M3	MIIMDC		AC3	GPIO[12]	1	AF13	PCIREQN[00]	
C24	DDRDATA[03]		M4	V_{cc} Core		AC4	V_{ss}		AF14	PCICBEN[02]	
C25	DDRDATA[08]		M23	V_{cc} Core		AC5	V_{ss}		AF15	PCITRDYN	
C26	DDRDATA[07]		M24	DDRDATA[23]		AC6	V_{ss}		AF16	PCISERRN	
D1	MII0RXD[03]		M25	DDRDATA[27]		AC7	V_{cc} I/O		AF17	PCIPAR	
D2	MII0RXD[01]		M26	DDRDATA[25]		AC8	V_{cc} I/O		AF18	PCIAD[14]	
D3	MII0RXD[02]		N1	MII1TXER		AC9	V_{cc} I/O		AF19	PCIAD[12]	
D4	V_{ss}		N2	MII1TXENP		AC10	V_{ss}		AF20	PCIAD[09]	
D5	V_{ss}		N3	GPIO[01]	1	AC11	V_{ss}		AF21	PCIAD[07]	
D6	V_{ss}		N4	V_{cc} Core		AC12	V_{ss}		AF22	PCIAD[03]	
D7	V_{cc} I/O		N23	V_{cc} Core		AC13	V_{cc} Core		AF23	PCIAD[01]	
D8	V_{cc} I/O		N24	DDRDATA[26]		AC14	V_{cc} Core		AF24	PCIGNTN[02]	
D9	V_{cc} I/O		N25	DDRDATA[28]		AC15	V_{cc} Core		AF25	DDRDM[06]	
D10	V_{ss}		N26	DDRDQS[03]		AC16	V_{ss}		AF26	DDROEN[03]	

Table 20 RC32438 416-pin Signal Pin-Out (Part 3 of 3)

RC32438 Power Pins

V_{cc} I/O	V_{cc} SI/O	V_{cc} Core	V_{cc} PLL
D7	D21	D13	Y2, AA3
D8	D22	D14	
D9	D23	D15	
D20	D24	K4	
P4	E23	L4	
R4	F23	L23	
T4	R23	M4	
U4	T23	M23	
AC7	AB24	N4	
AC8	AC23	N23	
AC9	AC24	P23	
AC20		AC13	
AC21		AC14	
AC22		AC15	

Table 21 RC32438 Power Pins

Signal Name	I/O Type	Location	Signal Category
GPIO[28]	I/O	AF5	General Purpose Input/Output
GPIO[29]	I/O	A13	
GPIO[30]	I/O	AE9	
GPIO[31]	I/O	A3	
INST	O	R1	Debug
JTAG_TCK	I	U2	EJTAG/ICE
JTAG_TDI	I	U1	
JTAG_TDO	O	U3	
JTAG_TMS	I	AD2	
JTAG_TRST_N	I	AD1	
MADDR[00]	O	B22	Memory and Peripheral Bus
MADDR[01]	O	C22	
MADDR[02]	O	A22	
MADDR[03]	O	B21	
MADDR[04]	O	C21	
MADDR[05]	O	A21	
MADDR[06]	O	B20	
MADDR[07]	O	A20	
MADDR[08]	O	C20	
MADDR[09]	O	B19	
MADDR[10]	O	A19	
MADDR[11]	O	C19	
MADDR[12]	O	B18	
MADDR[13]	O	A18	
MADDR[14]	O	B17	
MADDR[15]	O	C18	
MADDR[16]	O	A17	
MADDR[17]	O	B16	
MADDR[18]	O	C17	
MADDR[19]	O	A16	
MADDR[20]	O	B14	
MADDR[21]	O	A15	
MDATA[00]	I/O	C15	
MDATA[01]	I/O	C12	

Table 24 RC32438 Alphabetical Signal List (Part 5 of 9)

Signal Name	I/O Type	Location	Signal Category
PCIAD[21]	I/O	AD9	PCI Bus
PCIAD[22]	I/O	AE10	
PCIAD[23]	I/O	AF9	
PCIAD[24]	I/O	AF8	
PCIAD[25]	I/O	AE8	
PCIAD[26]	I/O	AD7	
PCIAD[27]	I/O	AF7	
PCIAD[28]	I/O	AE7	
PCIAD[29]	I/O	AF6	
PCIAD[30]	I/O	AD6	
PCIAD[31]	I/O	AE6	
PCICBEN[00]	I/O	AE21	
PCICBEN[01]	I/O	AE18	
PCICBEN[02]	I/O	AF14	
PCICBEN[03]	I/O	AD8	
PCICLK	I	AD12	
PCIDEVSELN	I/O	AE16	
PCIFRAMEN	I/O	AE15	
PCIGNTN[00]	I/O	AD13	
PCIGNTN[01]	I/O	AE24	
PCIGNTN[02]	I/O	AF24	
PCIGNTN[03]	I/O	AD21	
PCIIRDYN	I/O	AD14	
PCILOCKN	I/O	AE17	
PCIPAR	I/O	AF17	
PCIPERRN	I/O	AD16	
PCIREQN[00]	I/O	AF13	
PCIREQN[01]	I/O	AD11	
PCIREQN[02]	I/O	AE14	
PCIREQN[03]	I/O	AF12	
PCIRSTN	I/O	AE13	
PCISERRN	I/O	AF16	
PCISTOPN	I/O	AD15	
PCITRDYN	I/O	AF15	
RSTN	I/O	A23	System
RWN	O	B3	Memory and Peripheral Bus

Table 24 RC32438 Alphabetical Signal List (Part 8 of 9)

RC32438 Pinout — Top View