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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	80-PQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc812bsz-reel

PIN FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
DV_{DD}	P	Digital Positive Supply Voltage, 3 V or 5 V Nominal.
AV_{DD}	P	Analog Positive Supply Voltage, 3 V or 5 V Nominal.
C_{REF}	I	Decoupling Input for On-Chip Reference. Connect 0.1 μF between this pin and AGND.
V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V, which appears at the pin. This pin can be overdriven by an external reference.
AGND	G	Analog Ground. Ground reference point for the analog circuitry.
P1.0–P1.7	I	Port 1 is an 8-bit input port only. Unlike other ports, Port 1 defaults to Analog Input mode. To configure any of these Port Pins as a digital input, write a 0 to the port bit. Port 1 pins are multifunctional and share the following functionality.
ADC0–ADC7	I	Analog Inputs. Eight single-ended analog inputs. Channel selection is via ADCCON2 SFR.
T2	I	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
T2EX	I	Digital Input. Capture/Reload trigger for Counter 2; also functions as an Up/Down control input for Counter 2.
$\overline{SS}$	I	Slave Select Input for the SPI Interface.
SDATA	I/O	User selectable, I^2C Compatible or SPI Data Input/Output Pin.
SCLOCK	I/O	Serial Clock Pin for I^2C Compatible or SPI Serial Interface Clock.
MOSI	I/O	SPI Master Output/Slave Input Data I/O Pin for SPI Interface.
MISO	I/O	SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface.
DAC0	O	Voltage Output from DAC0.
DAC1	O	Voltage Output from DAC1.
RESET	I	Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device. External power-on reset (POR) circuity must be implemented to drive the RESET pin as described in the Power-On Reset Operation section.
P3.0–P3.7	I/O	Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors; in that state they can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. Port 3 pins also contain various secondary functions that are described below.
RxD	I/O	Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of Serial (UART) Port
TxD	O	Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of Serial (UART) Port
$\overline{INT0}$	I	Interrupt 0, programmable edge or level triggered Interrupt input, $\overline{INT0}$ can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
$\overline{INT1}$	I	Interrupt 1, programmable edge or level triggered Interrupt input, $\overline{INT1}$ can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
T0	I	Timer/Counter 0 Input.
T1	I	Timer/Counter 1 Input.
$\overline{CONVST}$	I	Active Low Convert Start Logic Input for the ADC Block when the External Convert Start Function is Enabled. A low-to-high transition on this input puts the track-and-hold into its hold mode and starts conversion.
$\overline{WR}$	O	Write Control Signal, Logic Output. Latches the data byte from Port 0 into the external data memory.
$\overline{RD}$	O	Read Control Signal, Logic Output. Enables the external data memory to Port 0.
XTAL2	O	Output of the Inverting Oscillator Amplifier.
XTAL1	I	Input to the Inverting Oscillator Amplifier and to the Internal Clock Generator Circuits.
DGND	G	Digital Ground. Ground reference point for the digital circuitry.
P2.0–P2.7 (A8–A15) (A16–A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors; in that state they can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the external 24-bit external data memory space.

PIN FUNCTION DESCRIPTIONS (continued)

Mnemonic	Type	Function
$\overline{\text{PSEN}}$	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. $\overline{\text{PSEN}}$ can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET.
ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFH. When held low, this input enables the device to fetch all instructions from external program memory.
P0.7–P0.0 (A0–A7)	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pull-ups when emitting 1s.
EP		Exposed Pad. For the LFCSP, the exposed pad must be soldered and left unconnected.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

Full-Scale Error

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal-to-(Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

ARCHITECTURE, MAIN FEATURES

The ADuC812 is a highly integrated, true 12-bit data acquisition system. At its core, the ADuC812 incorporates a high performance 8-bit (8052 compatible) MCU with on-chip reprogrammable nonvolatile Flash program memory controlling a multichannel (eight input channels) 12-bit ADC.

The chip incorporates all secondary functions to fully support the programmable data acquisition core. These secondary functions include User Flash Memory, Watchdog Timer (WDT), Power Supply Monitor (PSM), and various industry-standard parallel and serial interfaces.

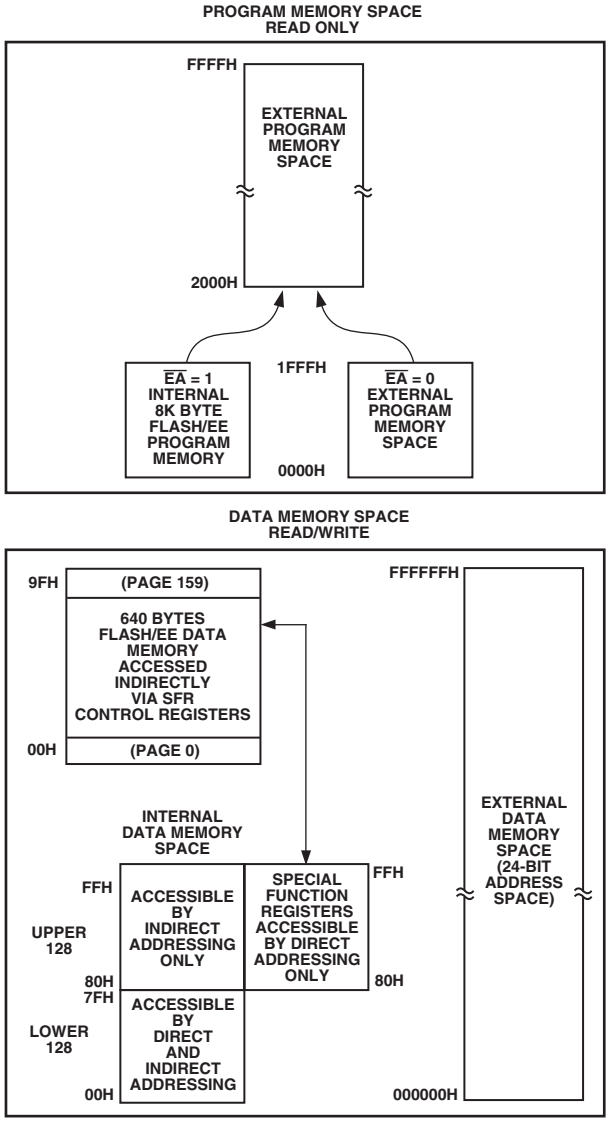


Figure 1. Program and Data Memory Maps

The lower 128 bytes of internal data memory are mapped as shown in Figure 2. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits) above the register banks form a block of bit addressable memory space at bit addresses 00H through 7FH.

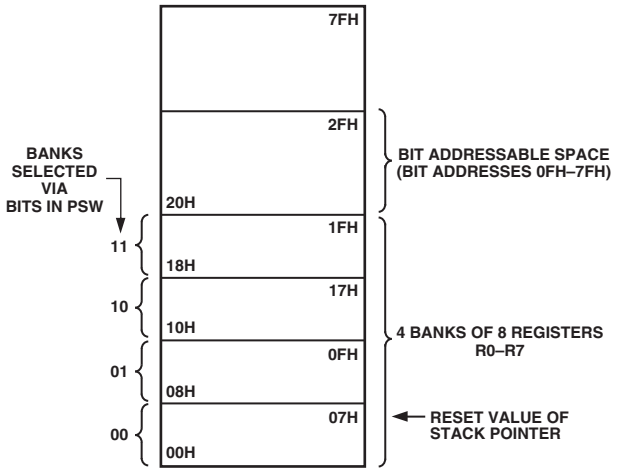


Figure 2. Lower 128 Bytes of Internal RAM

MEMORY ORGANIZATION

As with all 8052 compatible devices, the ADuC812 has separate address spaces for program and data memory as shown in Figure 1. Also as shown in Figure 1, an additional 640 bytes of User Data Flash EEPROM are available to the user. The User Data Flash Memory area is accessed indirectly via a group of control registers mapped in the Special Function Register (SFR) area in the Data Memory Space.

The SFR space is mapped in the upper 128 bytes of internal data memory space. The SFR area is accessed by direct addressing only and provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC812 via the SFR area is shown in Figure 3.

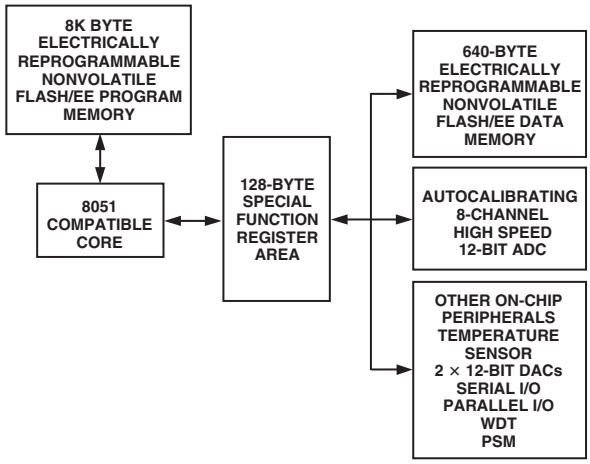


Figure 3. Programming Model

OVERVIEW OF MCU-RELATED SFRs

Accumulator SFR

ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR

The B register is used with the ACC for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratch pad register.

Stack Pointer SFR

The SP register is the stack pointer and is used to hold an internal RAM address that is called the "top of the stack." The SP register is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Data Pointer

The Data Pointer is made up of three 8-bit registers: DPP (page byte), DPH (high byte), and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, and DPL).

Program Status Word SFR

The PSW register is the Program Status Word that contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power-On Default Value	00H
Bit Addressable	Yes

CY	AC	F0	RS1	RS0	OV	F1	P

Table I. PSW SFR Bit Designations

Bit	Name	Description
7	CY	Carry Flag
6	AC	Auxiliary Carry Flag
5	F0	General-Purpose Flag
4	RS1	Register Bank Select Bits
3	RS0	RS1 RS0 Selected Bank 0 0 0 0 1 1 1 0 2 1 1 3
2	OV	Overflow Flag
1	F1	General-Purpose Flag
0	P	Parity Bit

Power Control SFR

The Power Control (PCON) register contains bits for power saving options and general-purpose status flags as shown in Table II.

SFR Address	87H
Power-On Default Value	00H
Bit Addressable	No

SMOD	———	———	ALEOFF	GF1	GF0	PD	IDL

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	———	Reserved
5	———	Reserved
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

SPECIAL FUNCTION REGISTERS

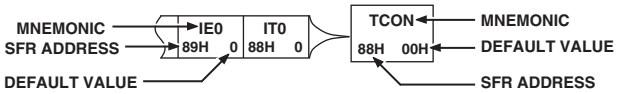
All registers except the program counter and the four general-purpose register banks reside in the special function register (SFR) area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and other on-chip peripherals.

Figure 4 shows a full SFR memory map and SFR contents on reset. Unoccupied SFR locations are shown dark shaded (NOT USED). Unoccupied locations in the SFR address space are not implemented, i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for on-chip testing are shown lighter shaded (RESERVED) and should not be accessed by user software. Sixteen of the SFR locations are also bit addressable and denoted by "1" i.e., the bit addressable SFRs are those whose address ends in 0H or 8H.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 0	SPR1 F9H 0	SPR0 F8H 0	BITS	SPICON[1] F8H 00H
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS	B[1] F0H 00H
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS	I2CCON[1] E8H 00H
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS	ACC[1] E0H 00H
ADCI DFH 0	DMA DEH 0	CCONV DDH 0	SCONV DCH 0	CS3 DBH 0	CS2 DAH 0	CS1 D9H 0	CS0 D8H 0	BITS	ADCCON2[1] D8H 00H
CY D7H 0	AC D6H 0	F0 D5H 0	RS1 D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS	PSW[1] D0H 00H
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS	T2CON[1] C8H 00H
PRE2 C7H 0	PRE1 C6H 0	PRE0 C5H 0	C4H 0	WDR1 C3H 0	WDR2 C2H 0	WDS C1H 0	WDE C0H 0	BITS	WDCON[1] C0H 00H
PSI BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH 0	PT0 B9H 0	PX0 B8H 0	BITS	IP[1] B8H 00H
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS	P3[1] B0H FFH
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS	IE[1] A8H 00H
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS	P2[1] A0H FFH
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	TI 99H 0	RI 98H 0	BITS	SCON[1] 98H 00H
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS	P1[1, 3] 90H FFH
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS	TCON[1] 88H 00H
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS	P0[1] 80H FFH

DAC0L F9H 00H	DAC0H FAH 00H	DAC1L FBH 00H	DAC1H FCH 00H	DACCON FDH 04H	RESERVED	NOT USED		
ADCOFSL[2] F1H 00H	ADCOFSH[2] F2H 20H	ADCGAINL[2] F3H 00H	ADCGAINH[2] F4H 00H	ADCCON3 F5H 00H	RESERVED	SPIDAT F7H 00H		
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADCCON1 EFH 20H		
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		
ADCDATAL D9H 00H	ADCDATAH DAH 00H	RESERVED	RESERVED	RESERVED	RESERVED	PSMCON DFH DEH		
RESERVED	DMAL D2H 00H	DMAH D3H 00H	DMAP D4H 00H	RESERVED	RESERVED	RESERVED		
RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED		
NOT USED	NOT USED	NOT USED	ETIM3 C4H C9H	RESERVED	EDARL C6H 00H	RESERVED		
ECON B9H 00H	ETIM1 BAH 52H	ETIM2 BBH 04H	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED		
IE2 A9H 00H	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED		
SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	NOT USED	NOT USED	NOT USED	NOT USED		
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED		
TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	NOT USED	NOT USED		
SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H		

SFR MAP KEY:



SFR NOTES

[1]SFRs WHOSE ADDRESS ENDS IN 0H OR 8H ARE BIT ADDRESSABLE.
[2]CALIBRATION COEFFICIENTS ARE PRECONFIGURED ON POWER-UP TO FACTORY CALIBRATED VALUES.
[3]THE PRIMARY FUNCTION OF PORT 1 IS AS AN ANALOG INPUT PORT; THEREFORE, TO ENABLE THE DIGITAL SECONDARY FUNCTIONS ON THESE PORT PINS, WRITE A "0" TO THE CORRESPONDING PORT 1 SFR BIT.

Figure 4. Special Function Register Locations and Reset Values

Using the Flash/EE Program Memory

This 8K byte Flash/EE program memory array is mapped into the lower 8K bytes of the 64K bytes program space addressable by the ADuC812 and will be used to hold user code in typical applications.

The program memory array can be programmed in one of two modes:

Serial Downloading (In-Circuit Programming)

As part of its embedded download/debug kernel, the ADuC812 facilitates serial code download via the standard UART serial port. Serial download mode is automatically entered on power-up if the external pin $\overline{\text{PSEN}}$ is pulled low through an external resistor as shown in Figure 15. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC812 QuickStart development system.

The Serial Download protocol is detailed in a MicroConverter Applications Note uC004, available from the ADI MicroConverter website at www.analog.com/microconverter.

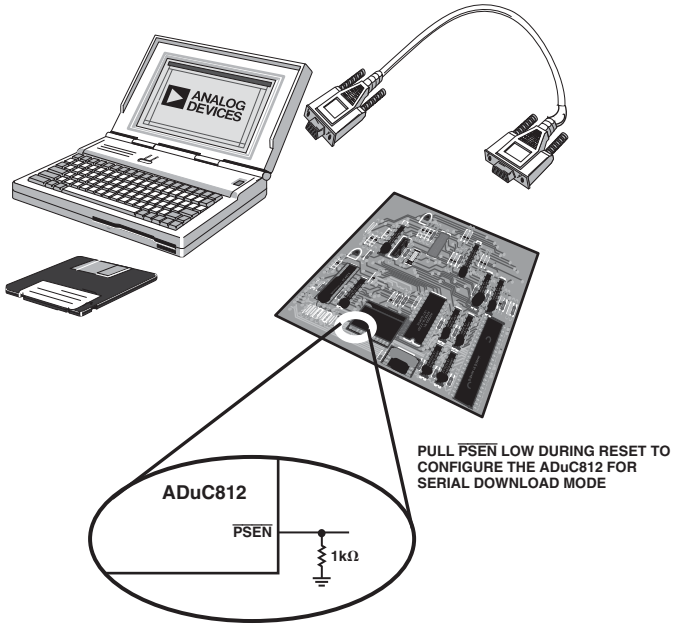


Figure 15. Flash/EE Memory Serial Download Mode Programming

Parallel Programming

The parallel programming mode is fully compatible with conventional third party Flash or EEPROM device programmers. In this mode, Ports P0, P1, and P2 operate as the external data and address bus interface, ALE operates as the Write Enable strobe, and Port P3 is used as a general configuration port that configures the device for various program and erase operations during parallel programming.

The high voltage (12 V) supply required for Flash programming is generated using on-chip charge pumps to supply the high voltage program lines.

The complete parallel programming specification is available on the MicroConverter homepage at www.analog.com/microconverter.

Using the Flash/EE Data Memory

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (Page 00H to Page 9FH) 4-byte pages, as shown in Figure 16.

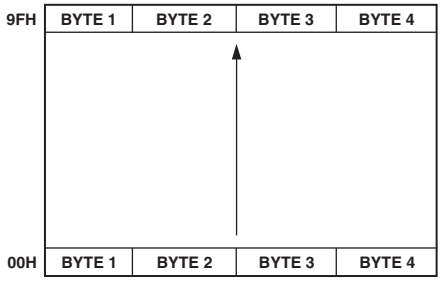


Figure 16. User Flash/EE Memory Configuration

As with other ADuC812 user peripheral circuits, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) is used to hold the 4-byte page being accessed. EADRL is used to hold the 8-bit address of the page being accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to trigger various read, write, erase, and verify functions. These register can be summarized as follows:

ECON:	SFR Address	B9H
	Function	Controls access to 640 bytes Flash/EE data space.
	Default	00H
EADRL:	SFR Address	C6H
	Function	Holds the Flash/EE data page address. 0H through 9FH
	Default	00H
EDATA1–4:		
	SFR Address	BCH to BFH, respectively
	Function	Holds the Flash/EE data memory page write or page read data bytes.
	Default	EDATA1–4→00H

A block diagram of the SFR registered interface to the data Flash/EE memory array is shown in Figure 17.

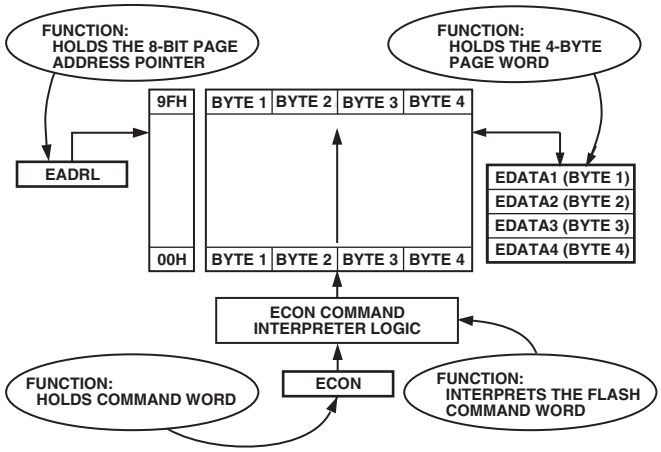


Figure 17. User Flash/EE Memory Control and Configuration

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 18. Details of the actual DAC architecture can be found in U.S. Patent Number 5969657 (www.uspto.gov). Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

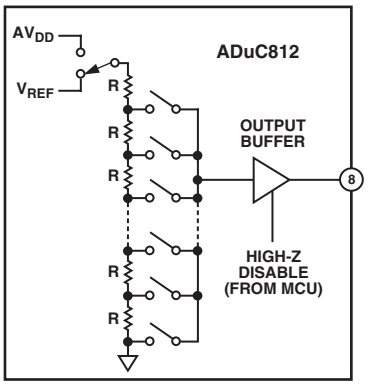


Figure 18. Resistor String DAC Functional Equivalent

As illustrated in Figure 18, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF}, or if an external reference is applied, the voltage at the V_{REF} pin. The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function *except* codes 0 to 48, and, in 0-to-AV_{DD} mode only, codes 3995 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 19. The dotted line in Figure 19 indicates the *ideal* transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 19 represents a transfer function in 0-to-V_{DD} mode only. In 0-to-V_{REF} mode (with $V_{REF} < V_{DD}$) the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the "ideal" line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of endpoint linearity errors.

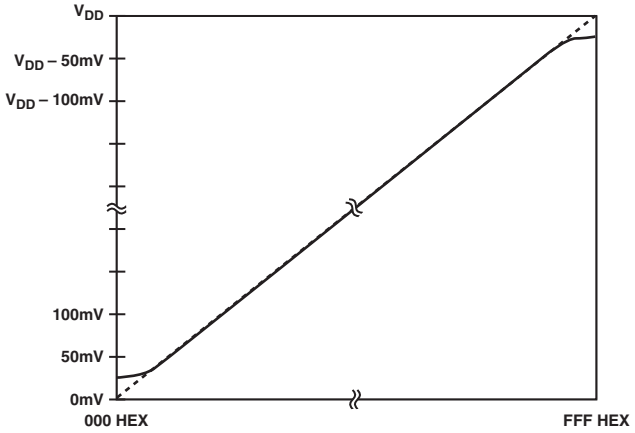


Figure 19. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 19 get worse as a function of output loading. Most of the ADuC812's data sheet specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 19 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 20 and Figure 21 illustrate this behavior. It should be noted that the upper trace in each of these figures is only valid for an output range selection of 0-to-AV_{DD}. In 0-to-V_{REF} mode, DAC loading will not cause high-side voltage drops as long as the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage will not be affected by loads less than 5 mA. But somewhere around 7 mA the upper curve in Figure 21 drops below 2.5 V (V_{REF}), indicating that at these higher currents the output will not be capable of reaching V_{REF}.

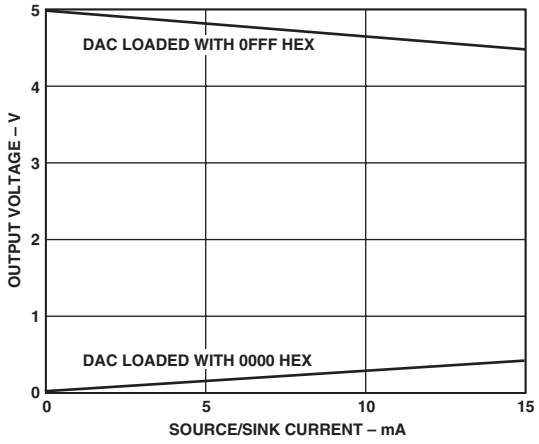


Figure 20. Source and Sink Current Capability with $V_{REF} = V_{DD} = 5$ V

MOSI (Master Out, Slave In Pin)
The MOSI (master out, slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin)
The master serial clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table XI). In slave mode, the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important therefore that the CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin)
The Slave Select ($\overline{SS}$) input pin is shared with the ADC5 input. To configure this pin as a digital input, the bit must be cleared, e.g., CLR P1.5.

This line is active low. Data is only received or transmitted in slave mode when the $\overline{SS}$ pin is low, allowing the ADuC812 to be used in single master, multislave SPI configurations. If CPHA = 1, then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte wide transmission or reception, and return high again after the last bit in that byte wide transmission or reception. In SPI Slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR. The following SFR registers are used to control the SPI interface.

SPICON	**SPI Control Register**
SFR Address	F8H
Power-On Default Value	OOH
Bit Addressable	Yes

ISPI	WCOL	SPE	SPIM	CPOL	CPHA	SPR1	SPR0

Table XI. SPICON SFR Bit Designations

Bit	Name	Description
7	ISPI	SPI Interrupt Bit. Set by MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user to enable the SPI interface. Cleared by user to enable I^2C interface.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user to enable Master mode operation (SCLOCK is an output). Cleared by user to enable Slave mode operation (SCLOCK is an input).
3	CPOL*	Clock Polarity Select Bit. Set by user if SCLOCK idles high. Cleared by user if SCLOCK idles low.
2	CPHA*	Clock Phase Select Bit. Set by user if leading SCLOCK edge is to transmit data. Cleared by user if trailing SCLOCK edge is to transmit data.
1	SPR1	SPI Bit Rate Select Bits.
0	SPR0	These bits select the SCLOCK rate (bit rate) in Master mode as follows: SPR1 SPR0 Selected Bit Rate 0 0 $f_{OSC}/4$ 0 1 $f_{OSC}/8$ 1 0 $f_{OSC}/32$ 1 1 $f_{OSC}/64$ In SPI Slave mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit.

*The CPOL and CPHA bits should both contain the same values for master and slave devices.

	Timer/Counter 2
T2CON	**Control Register**
SFR Address	C8H
Power-On Default Value	00H
Bit Addressable	Yes

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CNT2	CAP2

Table XVII. T2CON SFR Bit Designations

Bit	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 will not be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by user to start Timer 2. Cleared by user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and timer capture/reload registers.

TH2 and TL2

Timer 2, data high byte and low byte.
SFR Address = CDH, CCH, respectively.

RCAP2H and RCAP2L

Timer 2, Capture/Reload high byte and low byte.
SFR Address = CBH, CAH, respectively.

Timer/Counter Operation Modes

The following paragraphs describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table XVIII.

Table XVIII. TIMECON SFR Bit Designations

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In Autoreload mode, there are two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to reload with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1 then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The Autoreload mode is illustrated in Figure 30.

16-Bit Capture Mode

In the Capture mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, that can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture mode is illustrated in Figure 31.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag will not occur. Therefore Timer 2 interrupts will not occur, so they do not have to be disabled. In this mode however, the EXF2 flag can still cause interrupts and this can be used as a third external interrupt.

Baud rate generation will be described as part of the UART serial port operation in the following pages.

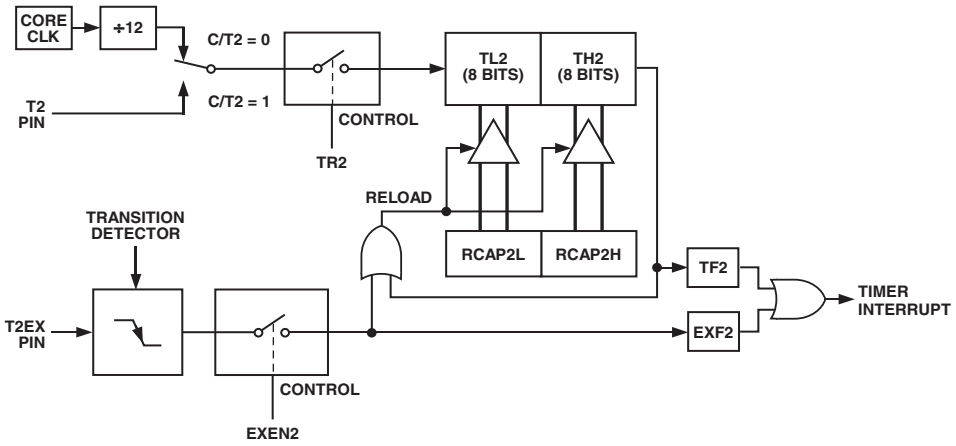


Figure 30. Timer/Counter 2, 16-Bit Autoreload Mode

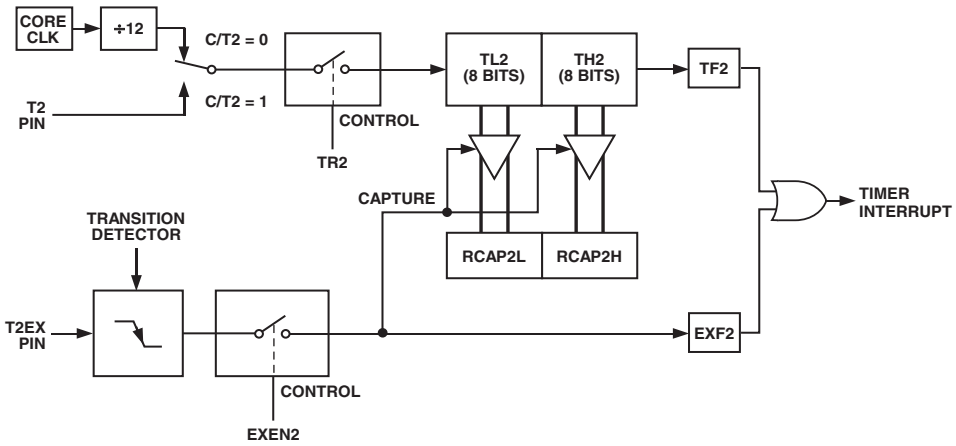


Figure 31. Timer/Counter 2, 16-Bit Capture Mode

INTERRUPT SYSTEM

The ADuC812 provides a total of nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt related SFRs.

IE	Interrupt Enable Register
IP	Interrupt Priority Register
IE2	Secondary Interrupt Enable Register

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default Value	00H
Bit Addressable	Yes

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Table XXII. IE SFR Bit Designations

Bit	Name	Description
7	EA	Written by user to enable "1" or disable "0" all interrupt sources.
6	EADC	Written by user to enable "1" or disable "0" ADC interrupt.
5	ET2	Written by user to enable "1" or disable "0" Timer 2 interrupt.
4	ES	Written by user to enable "1" or disable "0" UART serial port interrupt.
3	ET1	Written by user to enable "1" or disable "0" Timer 1 interrupt.
2	EX1	Written by user to enable "1" or disable "0" External Interrupt 1.
1	ET0	Written by user to enable "1" or disable "0" Timer 0 interrupt.
0	EX0	Written by user to enable "1" or disable "0" External Interrupt 0.

IP	**Interrupt Priority Register**
SFR Address	B8H
Power-On Default Value	00H
Bit Addressable	Yes

PSI	PADC	PT2	PS	PT1	PX1	PT0	PX0

Table XXIII. IP SFR Bit Designations

Bit	Name	Description
7	PSI	Written by user to select I^2C/SPI priority ("1" = High; "0" = Low).
6	PADC	Written by user to select ADC interrupt priority ("1" = High; "0" = Low).
5	PT2	Written by user to select Timer 2 interrupt priority ("1" = High; "0" = Low).
4	PS	Written by user to select UART serial port interrupt priority ("1" = High; "0" = Low).
3	PT1	Written by user to select Timer 1 interrupt priority ("1" = High; "0" = Low).
2	PX1	Written by user to select External Interrupt 1 priority ("1" = High; "0" = Low).
1	PT0	Written by user to select Timer 0 interrupt priority ("1" = High; "0" = Low).
0	PX0	Written by user to select External Interrupt 0 priority ("1" = High; "0" = Low).

IE2 **Secondary Interrupt Enable Register**
SFR Address A9H
Power-On Default Value 00H
Bit Addressable No

—	—	—	—	—	—	EPSMI	ESI

Table XXIV. IE2 SFR Bit Designations

Bit	Name	Description
7	—	Reserved for future use.
6	—	Reserved for future use.
5	—	Reserved for future use.
4	—	Reserved for future use.
3	—	Reserved for future use.
2	—	Reserved for future use.
1	EPSMI	Written by user to Enable "1" or Disable "0" power supply monitor interrupt.
0	ESI	Written by user to Enable "1" or Disable "0" I^2C/SPI serial port interrupt.

Interrupt Priority
The Interrupt Enable registers are written by the user to enable individual interrupt sources, while the Interrupt Priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of high priority may interrupt the service routine of a low priority interrupt. If two interrupts of different priorities occur at the same time, the higher level interrupt will be served first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed, as shown in Table XXV.

Table XXV. Priority within an Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
IE0	2	External Interrupt 0
ADCI	3	ADC Interrupt
TF0	4	Timer/Counter 0 Interrupt
IE1	5	External Interrupt 1
TF1	6	Timer/Counter 1 Interrupt
I2CI + ISPI	7	I^2C/SPI Interrupt
RI + TI	8	Serial Interrupt
TF2 + EXF2	9 (Lowest)	Timer/Counter 2 Interrupt

Interrupt Vectors
When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in the Table XXVI.

Table XXVI. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
ADCI	0033H
I2CI + ISPI	003BH
PSMI	0043H

If access to more than 64K bytes of RAM is desired, a feature unique to the ADuC812 allows addressing up to 16 MBytes of external RAM simply by adding an additional latch as illustrated in Figure 39.

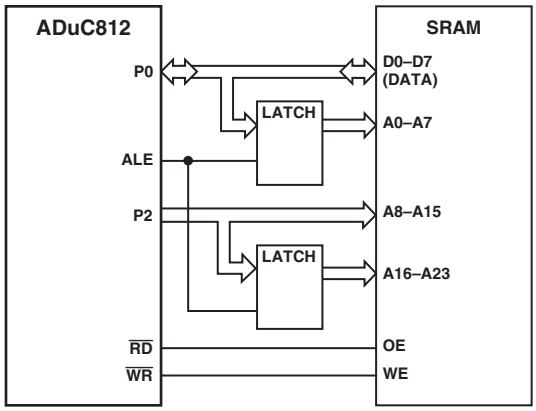


Figure 39. External Data Memory Interface (16 M Bytes Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC812 (write operation) or the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM and the 8051 standard of 64K byte external data memory access is maintained.

Detailed timing diagrams of external program and data memory read and write access can be found in the Timing Specification sections.

Power-On Reset Operation

External POR (power-on reset) circuitry must be implemented to drive the RESET pin of the ADuC812. The circuit must hold the RESET pin asserted (high) whenever the power supply (DV_{DD}) is below 2.5 V. Furthermore, V_{DD} must remain above 2.5 V for at least 10 ms before the RESET signal is deasserted (low), by which time the power supply must have reached at least a 2.7 V level. The external POR circuit must be operational down to 1.2 V or less. The timing diagram in Figure 40 illustrates this functionality under three separate events: power-up, brownout, and power-down. Notice that when RESET is asserted (high), it tracks the voltage on DV_{DD}. These recommendations must be adhered to through the manufacturing flow of your ADuC812 based system as well as during its normal power-on operation. Failure to adhere to these recommendations can result in permanent damage to device functionality.

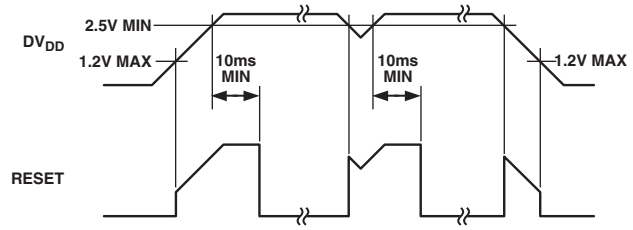


Figure 40. External POR Timing

The best way to implement an external POR function to meet the above requirements involves the use of a dedicated POR chip, such as the ADM809/ADM810 SOT-23 packaged PORs from Analog Devices. Recommended connection diagrams for both active high ADM810 and active low ADM809 PORs are shown in Figure 41 and Figure 42, respectively.

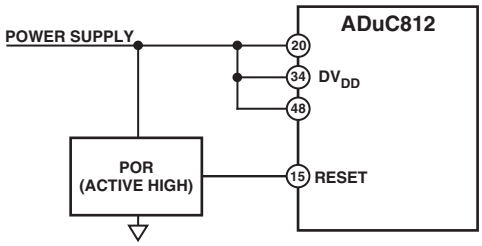


Figure 41. External Active High POR Circuit

Some active-low POR chips, such as the ADM809, can be used with a manual push-button as an additional reset source as illustrated by the dashed line connection in Figure 42.

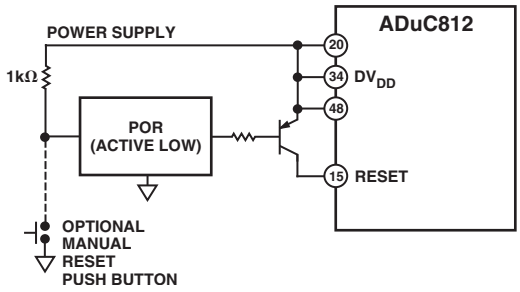


Figure 42. External Active Low POR Circuit

Power Supplies

The ADuC812's operational power supply voltage range is 2.7 V to 5.25 V. Although the guaranteed data sheet specifications are given only for power supplies within 2.7 V to 3.6 V or ±10% of the nominal 5 V level, the chip will function equally well at any power supply level between 2.7 V and 5.5 V.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system DV_{DD} line. However, though you can power AV_{DD} and DV_{DD} from two separate supplies if desired, you must ensure that they remain within ±0.3 V of one another at all times in order to avoid damaging the chip (as per the Absolute Maximum Ratings section). Therefore it is recommended that unless AV_{DD} and DV_{DD} are connected directly together, you connect back-to-back Schottky diodes between them as shown in Figure 43.

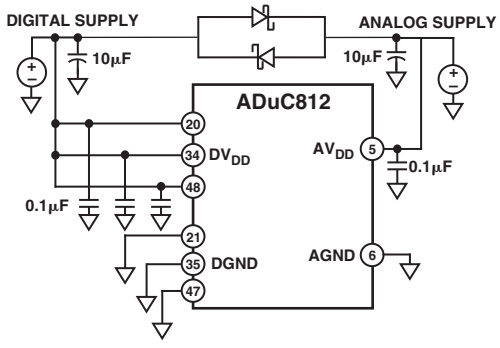


Figure 43. External Dual-Supply Connections

As an alternative to providing two separate power supplies, the user can help keep AV_{DD} quiet by placing a small series resistor and/or ferrite bead between it and DV_{DD}, and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 44. With this configuration, other analog circuitry (such as op amps, voltage reference, and so on) can be powered from the AV_{DD} supply line as well. The user will still want to include back-to-back Schottky diodes between AV_{DD} and DV_{DD} in order to protect from power-up and power-down transient conditions that could separate the two supply voltages momentarily.

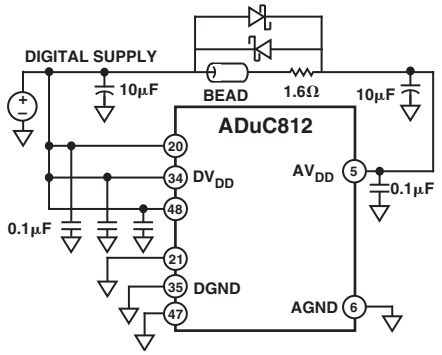


Figure 44. External Single-Supply Connections

Notice that in both Figure 43 and Figure 44, a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local small value (0.1 µF) capacitors are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors, and ensure the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should also be noted that, at all times, the analog and digital ground pins on the ADuC812 must be referenced to the same system ground reference point.

Power Consumption

The currents consumed by the various sections of the ADuC812 are shown in Table XXVII. The CORE values given represent the current drawn by DV_{DD}, while the rest (ADC, DAC, Voltage Reference) are pulled by the AV_{DD} pin and can be disabled in software when not in use. The other on-chip peripherals (watchdog timer, power supply monitor, and so on) consume negligible current and are therefore lumped in with the CORE operating current here. Of course, the user must add any currents sourced by the DAC or the parallel and serial I/O pins, in order to determine the total current needed at the ADuC812's supply pins. Also, current drawn from the DV_{DD} supply will increase by approximately 10 mA during Flash/EE erase and program cycles.

Table XXVII. Typical I_{DD} of Core and Peripherals

	V_{DD} = 5 V	V_{DD} = 3 V
CORE (Normal Mode)	(1.6 nAs × MCLK) + 6 mA	(0.8 nAs × MCLK) + 3 mA
CORE (Idle Mode)	(0.75 nAs × MCLK) + 5 mA	(0.25 nAs × MCLK) + 3 mA
ADC	1.3 mA	1.0 mA
DAC (Each)	250 µA	200 µA
Voltage Ref	200 µA	150 µA

Since operating DV_{DD} current is primarily a function of clock speed, the expressions for CORE supply current in Table XXVII are given as functions of MCLK, the oscillator frequency. Plug in a value for MCLK in hertz to determine the current consumed by the core at that oscillator frequency. Since the ADC and DACs can be enabled or disabled in software, add only the currents from the peripherals you expect to use. The internal voltage reference is automatically enabled whenever either the ADC or at least one DAC is enabled. And again, do not forget to include current sourced by I/O pins, serial port pins, DAC outputs, and so forth, plus the additional current drawn during Flash/EE erase and program cycles.

A software switch allows the chip to be switched from normal mode into idle mode, and also into full power-down mode. Below are brief descriptions of power-down and idle modes.

In idle mode, the oscillator continues to run but is gated off to the core only. The on-chip peripherals continue to receive the clock, and remain functional. Port pins and DAC output pins retain their states in this mode. The chip will recover from idle mode upon receiving any enabled interrupt, or upon receiving a hardware reset.

In full power-down mode, the on-chip oscillator stops, and all on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state). The chip will only recover from power-down mode upon receiving a hardware reset or when power is cycled. During full power-down mode, the ADuC812 consumes a total of approximately 5 µA.

Parameter		12 MHz Min	12 MHz Max	Variable Clock Min	Variable Clock Max	Unit
EXTERNAL PROGRAM MEMORY READ CYCLE						
t_{LHLL}	ALE Pulsewidth	127		$2t_{CK} - 40$		ns
t_{AVLL}	Address Valid to ALE Low	43		$t_{CK} - 40$		ns
t_{LLAX}	Address Hold after ALE Low	53		$t_{CK} - 30$		ns
t_{LLIV}	ALE Low to Valid Instruction In		234		$4t_{CK} - 100$	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	53		$t_{CK} - 30$		ns
t_{PLPH}	$\overline{PSEN}$ Pulsewidth	205		$3t_{CK} - 45$		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CK} - 105$	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		59		$t_{CK} - 25$	ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CK} - 105$	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		25		25	ns
t_{PHAX}	Address Hold after $\overline{PSEN}$ High	0		0		ns

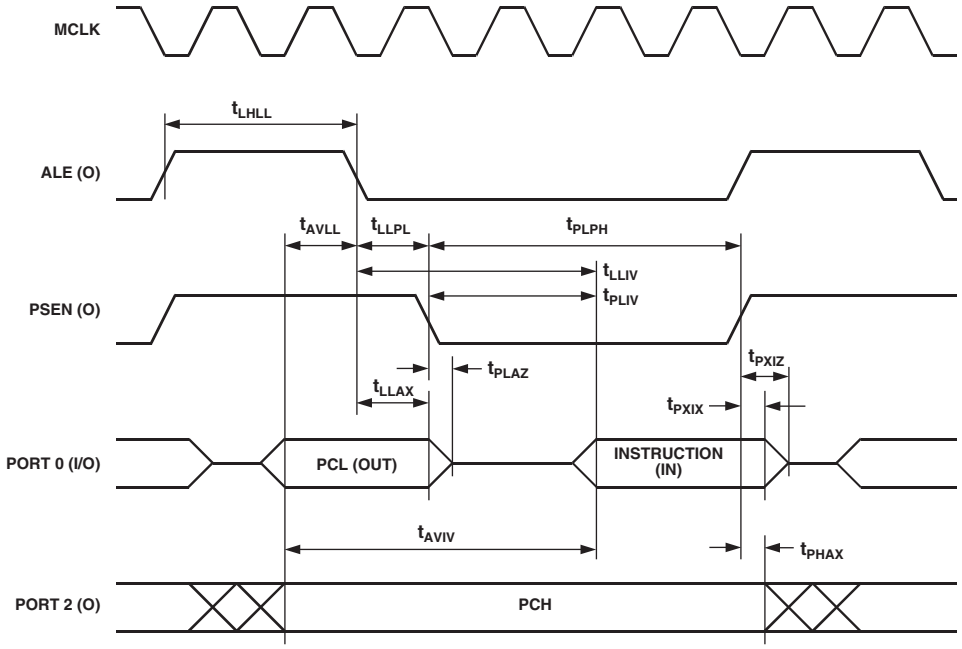


Figure 51. External Program Memory Read Cycle

Parameter		12 MHz Min	12 MHz Typ	12 MHz Max	Variable Clock Min	Variable Clock Typ	Variable Clock Max	Unit
UART TIMING (Shift Register Mode)								
t_{XLXL}	Serial Port Clock Cycle Time		1.0			$12t_{CK}$		μs
t_{QVXH}	Output Data Setup to Clock	700			$10t_{CK} - 133$			ns
t_{DVXH}	Input Data Setup to Clock	300			$2t_{CK} + 133$			ns
t_{XHDX}	Input Data Hold after Clock	0			0			ns
t_{XHQX}	Output Data Hold after Clock	50			$2t_{CK} - 117$			ns

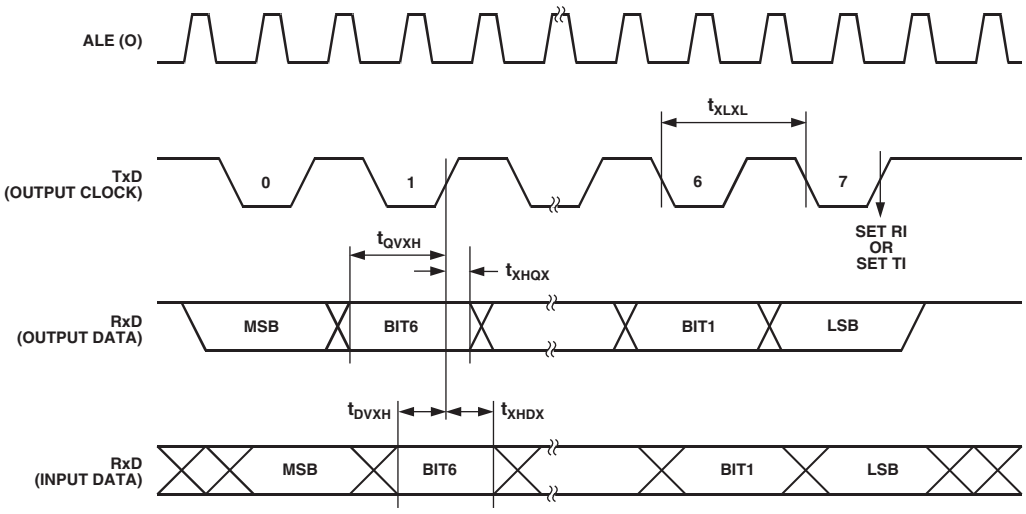


Figure 54. UART Timing in Shift Register Mode

Parameter		Min	Max	Unit
I^2C COMPATIBLE INTERFACE TIMING				
t_{LOW}	SCLOCK Low Pulsewidth	1.3		μs
t_{HIGH}	SCLOCK High Pulsewidth	0.6		μs
$t_{HD;\ STA}$	Start Condition Hold Time	0.6		μs
$t_{SU;\ DAT}$	Data Setup Time	100		μs
$t_{HD;\ DAT}$	Data Hold time	0	0.9	μs
$t_{SU;\ STA}$	Setup time for Repeated Start	0.6		μs
$t_{SU;\ STO}$	Stop Condition Setup Time	0.6		μs
t_{BUF}	Bus Free Time between a STOP Condition and a START Condition	1.3		μs
t_R	Rise Time for Both SCLOCK and SDATA		300	ns
t_F	Fall Time for Both SCLOCK and SDATA		300	ns
t_{SUP}[1]	Pulsewidth of Spike Suppressed		50	ns

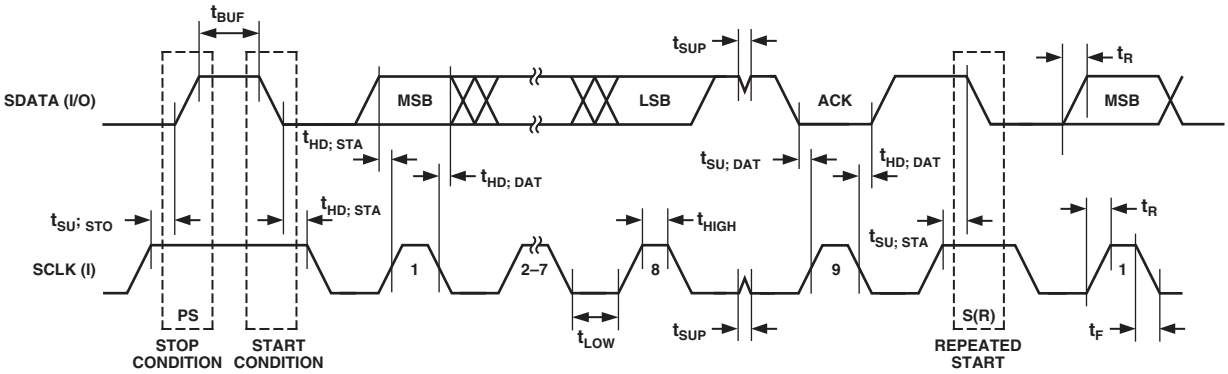


Figure 55. I^2C Compatible Interface Timing

Parameter		Min	Typ	Max	Unit
SPI SLAVE MODE TIMING (CPHA = 1)					
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulsewidth		330		ns
t_{SH}	SCLOCK High Pulsewidth		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

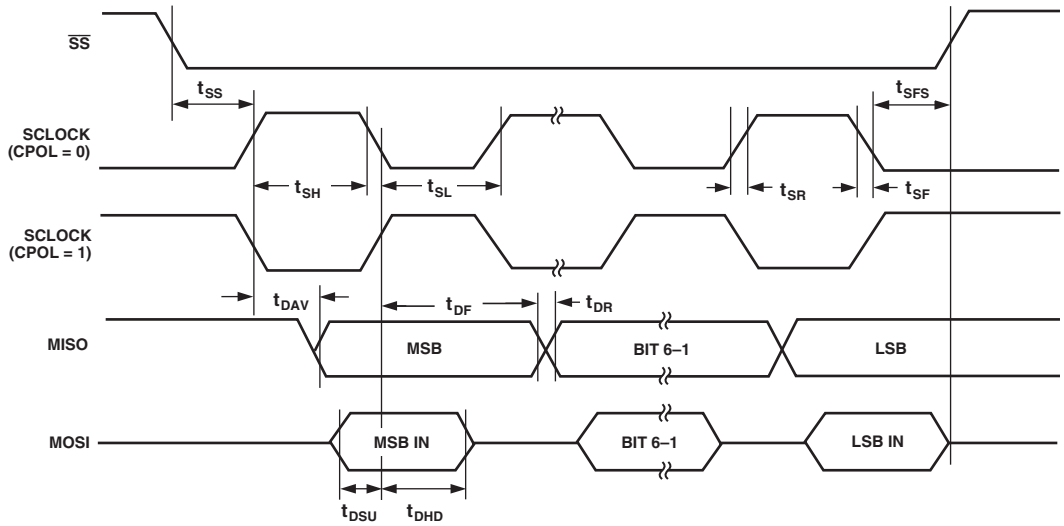


Figure 58. SPI Slave Mode Timing (CPHA = 1)

Parameter		Min	Typ	Max	Unit
SPI SLAVE MODE TIMING (CPHA = 0)					
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulsewidth		330		ns
t_{SH}	SCLOCK High Pulsewidth		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{DOSS}	Data Output Valid after $\overline{SS}$ Edge			20	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

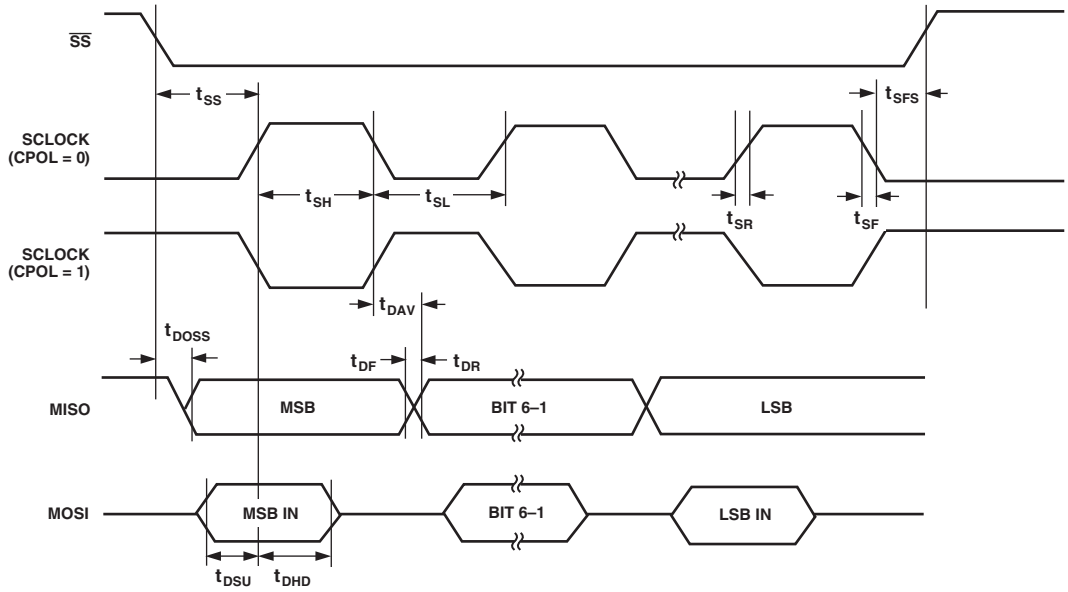
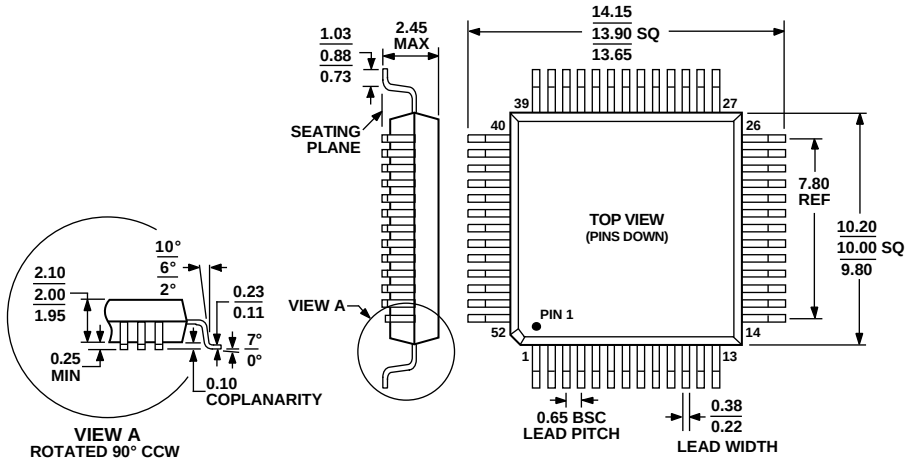


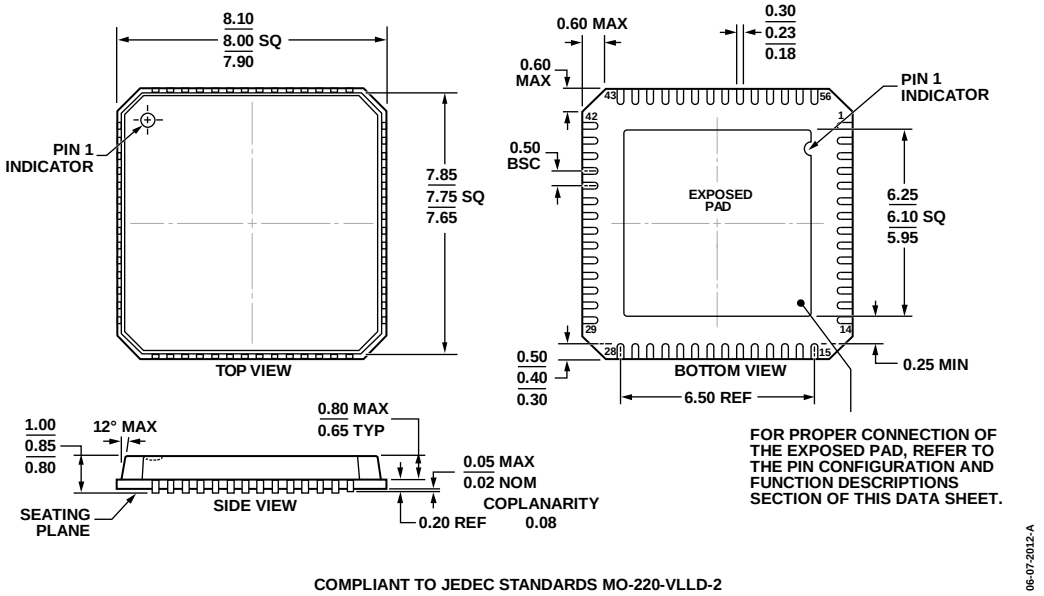
Figure 59. SPI Slave Mode Timing (CPHA = 0)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-112-AC-1

Figure 60. 52-Lead Metric Quad Flat Package [MQFP]
(S-52-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 61. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 x 8 mm Body, Very Thin Quad
(CP-56-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADuC812BSZ	–40°C to +85°C	52-Lead Metric Quad Flat Package [MQFP]	S-52-2
ADuC812BSZ-REEL	–40°C to +85°C	52-Lead Metric Quad Flat Package [MQFP]	S-52-2
EVAL-ADuC812QSZ		QuickStart Development System	

[1] Z = RoHS Compliant Part.